Future Prediction of Self-heating in Short Intra-block Wires

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Abstract

This paper predicts self-heating effect in a short intra-block wire will arise as a design issue with technology scaling. The short intra-block wires are close to the substrate and thought to have good thermal radiation characteristic, however, we reveal that the self-heating of short wires will be more significantly than that of global wires, and it can cause a reliability and performance degradation in the future. The max temperature rise from the ambient temperature becomes 27.3°C in a 14 nm process. Our attribution analysis also clarifies that shrinking wire cross-sectional area as well as low-k material and increased power dissipation deteriorates self-heating. Experimental results also reveal that the self-heating of local wires will be getting worse than repeater-inserted global wires.

1. Introduction

Recently, thermal integrity is becoming a principal design issue, since reliability such as electromigration [1, 2] and leakage current are strong functions of temperature, and increased power consumption makes the thermal problem more serious. To solve this problem, thermal analysis of a whole chip and temperature-aware design from architectural level [3] to physical design level [4] are a hot topic both in academia and industry.

From a micro point of view, on the other hand, self-heating problem of global wires has been comprehensively studied [5–11]. Self-heating effect is a phenomenon that the energy dissipated by wire resistance generates heat inside the wire, which results in an increase in temperature. An overheated wire causes [11]: (1) deterioration of signal propagation delay because of the electric resistance increase, and (2) reliability degradation such as electromigration. As for global wires, the self-heating problem has been discussed intensively, because the self-heating problem is thought to be more significant in global wires due to the following reasons [11]: (1) global wires are distantly routed from the substrate, and the generated heat is difficult to diffuse, and (2) large current usually flows in global wires, and generates a large amount of heat inside the wire.

In contrast, local and intermediate wires have been less paid attention to, because the wires are close to the substrate that has an excellent thermal conductivity, and the temperature increase is not significant. However, process scaling brings the following factors that may intensify the self-heating problem: (1) remarkable elevation of local clock frequency, which is higher than global clock, (2) thermal resistance increase by shrinking wire cross-sectional area, (3) introducing low-k materials for insulator. Thus, it is not sure whether the self-heating effect in short intra-block wires will be negligible or will cause a serious problem in the future.

This paper predicts that the self-heating effect arises in short intra-block wire in the future, and its temperature increase is compared with the increase in global wires that has been mainly discussed so far. The previous work [11] assumes an extreme configuration of current flowing in an global interconnect to clearly point out the self-heating problem. However, the impact of self-heating in a practical design, e.g. with buffer insertion, is still unclear. To evaluate the self-heating problem of signal wires from the viewpoint of practical circuit design, this work assumes a clock distribution, which is one of the practical worst-case, because the switching probability is one. As for global wiring, buffer insertion is considered to remove excessively long wire configurations.

The contribution of this work is to reveal that the wire self-heating problem arises not only in global wires but also in short intra-block wires in the future, and the temperature increases would be comparable, or rather the short wires will face severer self-heating. Our prediction will give a message to the future design guideline and contribute to improve reliability and performance.

The rest of the paper is organized as follows. Section 2 explains the motivation of this work. Section 3 describes the wire and chip models that are used for the prediction. Section 4 shows prediction results of the temperature in-

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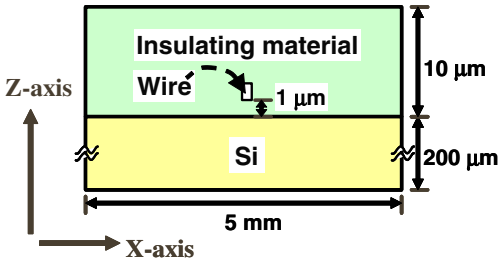

Figure 1. 2D chip model.

crease, and demonstrates an attribution analysis that examines which scaling parameter greatly influences the temperature rise. After that, we compare the self-heating of local wires with that of optimized global wires. Finally, we conclude the paper in Section 5.

2 Motivation

To explain the motivation why this work focuses on and examines the self-heating problem in short intra-block wires, we here show a simple example that the cross-sectional area reduction deteriorates the thermal problem. Let us suppose a simplified 2D chip model shown in Figure 1. The center rectangle represents a Cu wire, and the lower rectangle corresponds to the Si substrate. The upper large rectangle area is FSG (Fluorinated Silicate Glass), the insulating material. We assume that 10 μW is consumed per 1 μm-long wire, where this value is similar to that used in the experiment in Section 4 based on ITRS prediction. The cross-sectional area is scaled according to ITRS 2005 [12], which will be explained in detail in the next section. To clearly see the effect of scaled wire cross-sectional area, the distance from the substrate to the wire is constant of 1 μm in this example. The power dissipation and the insulating material are also assumed to be the same in every technology. The ambient temperature is 27°C.

Figure 2 shows the temperature rises of intermediate wire in the future process. ΔT here is the temperature rise from the ambient temperature and ΔT_{max} is maximum ΔT. The temperature increase comes from the shrink of the cross sectional area, because other parameters are unchanged. The distribution of the temperature rise from the ambient temperature in 2020 (Tech. node: 14 nm) is depicted in Figure 3. This observation gives an insight that smaller cross-section makes the heat dispersion difficult and the temperature increases very locally nearby the wire.

3 Wire and chip models for predicting self-heating problem

This section describes the wire and chip models used for the future prediction of the self-heating problem.

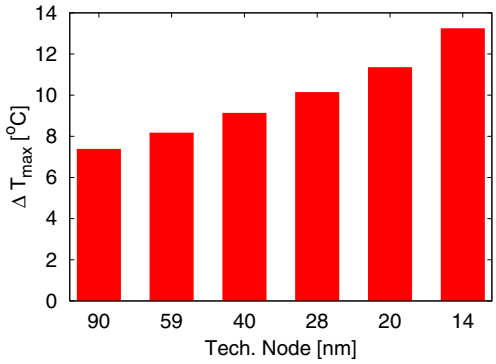

Figure 2. Prediction result of temperature rise from the ambient, ΔT_{max} (2D chip model).

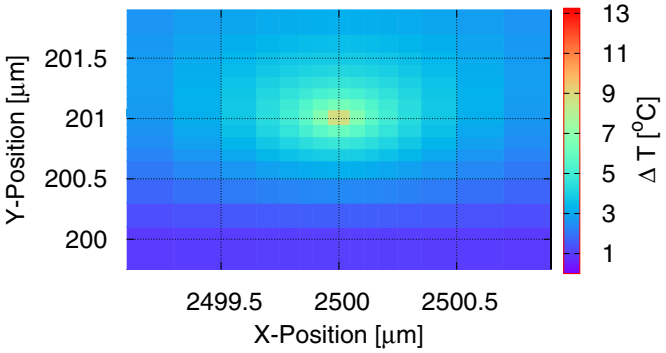

Figure 3. Distribution of ΔT in 2020 (2D chip model). The axes are indicated in Figure 1.

3.1. Device parameters in the future processes

The parameter set used for the evaluation of short intra-block wires is listed in Table 1 (see Appendix). The parameters are compatible with ITRS 2005 [12] except the three columns in the bottom, metal insulator, thermal conductivity of the metal insulator, and interconnect length L. These three parameters are determined by the following policies:

- selecting an insulating material that satisfies the effective dielectric constant predicted in ITRS and whose thermal conductivity is as high as possible. The relative permittivity and thermal conductivity of Porous Silica depend on its porosity, and we convert the effective dielectric constant into the porosity and then calculate the thermal conductivity [13, 14].
- the wire length L is chosen, assuming the intra-block clock distribution. L is short enough as a short intra-block wire. The detail will be explained later in Section 3.2.

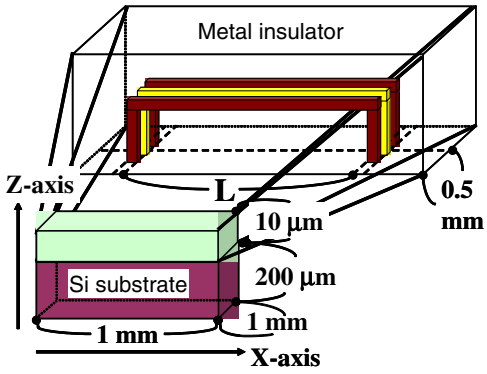

Figure 4. Wire model for self-heating prediction.

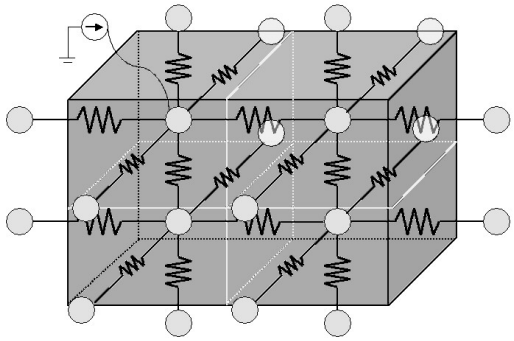

Figure 5. An example of heat diffusion model.

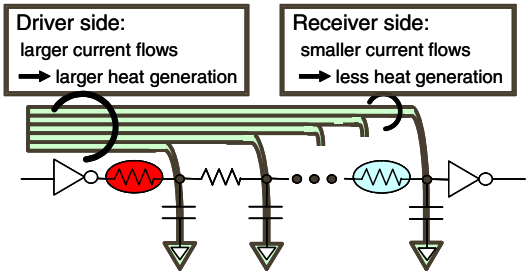

Figure 6. Nonuniform heating in a wire.

3.2. Wire and chip models

The wire and chip models used for the evaluation are depicted in Figure 4. The intra-block clock distribution on a 1 mm square chip is assumed. This paper analyzes the very local heat diffusion, and hence 1mm square chip is large enough to accurately estimate the self-heating effect. The upper cuboid is magnified in the upper figure, and there are three wires inside it. Three wires are placed on M5 layer in a 6-layer wiring structure. Our prediction evaluates ΔT, which is the temperature rise from the ambient temperature. We evaluate the temperature of the center wire in Figure 4, and it is driven by a 16x buffer whose output resistance is 50 Ω, and a 64x buffer (16x inverter + 64x inverter) is connected to the sink as a receiver in all technologies. The current flow in the wire is evaluated by circuit simulation with a predictive transistor model developed based on ITRS [15]. The other wires are placed as shielding wires and the spacing is equal to the wire width.

The heat radiation performance of the chip roughly corresponds to a package for 0.4 W/mm^2 chip. The side surface is heat insulated (θ = 1 [W/m^2·K]), and the upper/bottom surfaces are covered by the package of θ = 1500 [W/m^2·K] and θ = 4500 [W/m^2·K] respectively. The ambient temperature is 27°C.

The frequency of the injected clock signal comes from the local clock frequency in ITRS, and the input transition time is set to 10% of the clock cycle. At each technology node, the maximum wire length L is selected so that the receiver can receive the signal whose transition time is less than one-seventh of the clock cycle, where one-seventh is an empirical parameter often used in actual designs.

3.3. Thermal analysis technique

In our analysis, we use a finite-difference approach [4, 16] to solve the heat diffusion equation based on electrical-thermal analogy [7]. A chip is divided into cuboids. The thermal resistance is connected between adjacent nodes, where nodes are placed at the center of each cuboid. The consumed power is injected into the corresponding node from ground. For a simple example, when a chip is evenly divided by each lengthwise and crosswise direction, the model becomes like Figure 5.

When a CMOS gate is switching, larger current flows in the wire of driver side than the receiver side, as shown in Figure 6. Thus, larger heat is generated near the driver. We therefore analyze the self-heating effect in consideration of the nonuniform heating in a wire.

4. Prediction results and discussion

We here discuss the prediction results. In Section 4.1 and Section 4.2, we evaluate the short intra-block wires. Section 4.1 demonstrates prediction results of self-heating. Section 4.2 examines which scaling parameter dominantly determines the trend of the temperature increase.

Our prediction evaluates ΔT, which is the temperature rise from the ambient temperature. The prediction result of global wires is compared with that of the short intra-block wire in Section 4.3.

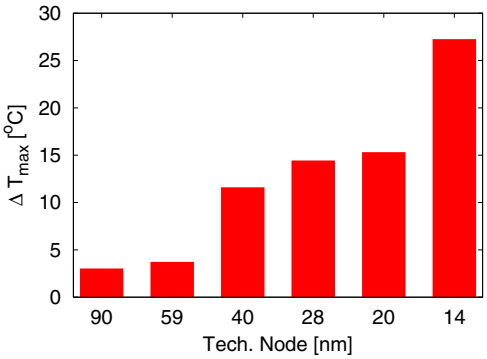

Figure 7. Prediction result of temperature rise from the ambient, ΔT_{max} (short intra-block wire).

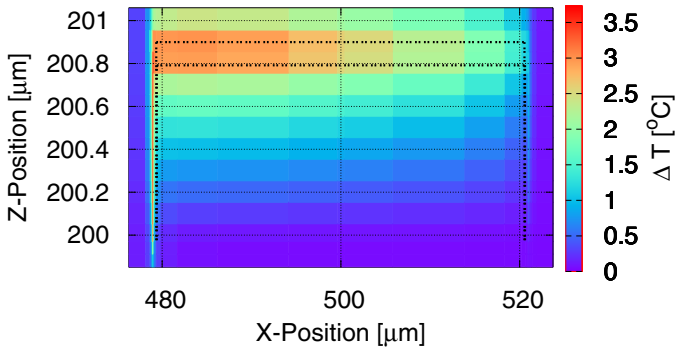

Figure 8. Distribution of ΔT in 2008 (short intra-block wire). The region surrounded with dotted lines corresponds to the wire, and the axes are indicated in Figure 4.

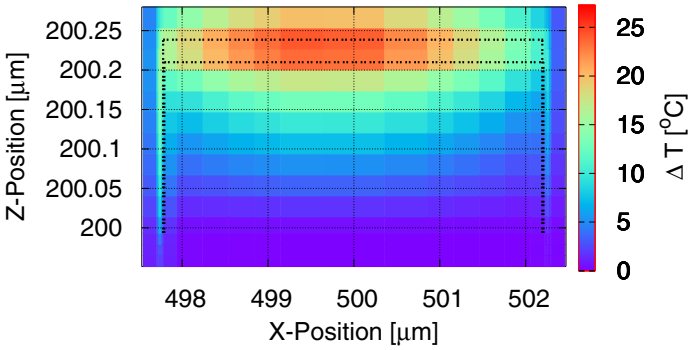

Figure 9. Distribution of ΔT in 2020 (short intra-block wire). The region surrounded with dotted lines corresponds to the wire, and the axes are indicated in Figure 4.

4.1. Temperature rise with scaling

Figure 7 shows the increasing trend of ΔT_{max} with process scaling, where ΔT_{max} is the maximum temperature difference between the ambient and the hottest point in the wire. The prediction result indicates that the self-heating in short intra-block wires will be significant as technology advances. ΔT_{max} becomes up to 27.3°C at 14 nm, whereas it is 3.0°C at 90 nm. It is quite reasonable that self-heating of short intra-block wires has not been considered so far, however, in the future, self-heating of short wires also must be taken into consideration in terms of performance and reliability.

ΔT distributions in 2008 (Tech. node: 59 nm) and 2020 (Tech. node: 14 nm) are depicted in Figure 8 and Figure 9, respectively. We see that a part of a wire which is close to the driver in the left side has the higher temperature rise in Figure 8, because larger current flows at the driving point as explained in Figure 6.

These figures indicate that the generated heat diffuses through not only the vertical metal (via) but also the interlevel metal insulator. Even for the short wires, the heat diffusion characteristics through the insulator are important. We think that the increase in thermal resistance due to smaller wire cross-sectional area also causes the temperature rise, as introduced in Figure 2. Further analysis is performed in the next section.

4.2. Attribution analysis of temperature rise

This section examines which process parameter dominantly influences the self-heating effect. The factors to examine are:

(a) distance from substrate,
(b) insulating material,
(c) power consumption,
(d) wire cross-sectional area,

where the other parameters are fixed to those in the 14 nm process.

Figure 10 shows the temperature trends. Y-axis represents "*Contribution*" defined in Equation (1), which means how much each parameter contributes to the temperature rise/fall.

$$Contribution\ [^{\circ}\mathrm{C}] = \Delta T_{max} - \Delta T_{max}(90nm). \quad (1)$$

As Figure 10 indicates, ΔT_{max} lowers with (a); scaling distance from substrate, and goes up with (b) - (d); insulating material, power consumption, and wire cross-sectional area. Considering all the factors together, we find that the effect of the temperature rise is larger than that of the temperature fall, which results in the temperature rise predicted in Section 4.1. A similar experiment is also conducted in terms of wire length L, however, *Contribution* is vanishingly small compared to the others. It is notably interesting that cross-sectional area affects the self-heating as much as insulating material and power consumption. Although the poor ther-

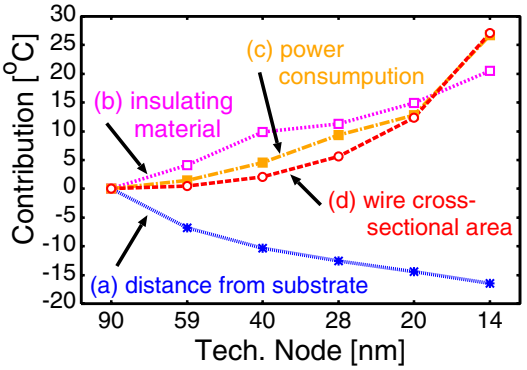

Figure 10. Result of attribution analysis on ΔT_{max}.

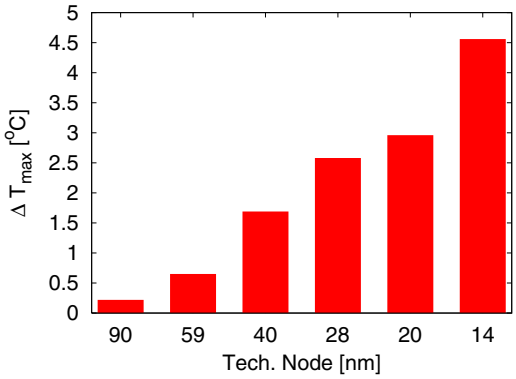

Figure 11. Prediction result of temperature rise from the ambient, ΔT_{max} (global wire).

mal conductance of the future insulating materials has been discussed in literatures [11, 14], the influence of smaller cross-sectional area on self-heating, which is pointed out in our work, has not been paid attention to. A small geometry of wires degrades thermal conductivity (heat diffusion to substrate) as well as electrical conductivity.

4.3. Temperature rise with scaling in global wire

We here predict the self-heating effect of global wires, and the result is compared with that of short intra-block wires. The wire model used for the experiment is same as Figure 4. The center of the three wires is the global wire to examine. The wire is placed on M11 layer in a 11-layer wiring chip.

The parameter set used for the evaluation is listed in Table 2 (see Appendix). The parameters are compatible with ITRS 2005 except the two rows in the bottom, buffer size and wire length L. These two parameters are an optimal solution of repeater insertion for minimizing the propagation delay [17, 18]. Compared with the case of the short intra-block wire, L is much larger. The wire width is set to one-second of "Minimum global wiring pitch". The gate output resistance and the gate input capacitance comply with ITRS 2005.

The global clock frequency is assumed to be one-fourth of the local clock, since the higher global clock is prevented by the large interconnect delay and difficult to realize. When the global clock could be the same as the local clock, the temperature rise would be multiplied by 4, because the thermal analysis is done with the linear circuit. The other conditions are similar to the case in the short intra-block wire (see Section 3.2).

The trend of ΔT_{max} is shown Figure 11. Figure 12 presents ΔT distribution of 2020 (Tech. node: 14 nm) . From this result, the self-heating effect of the global wire

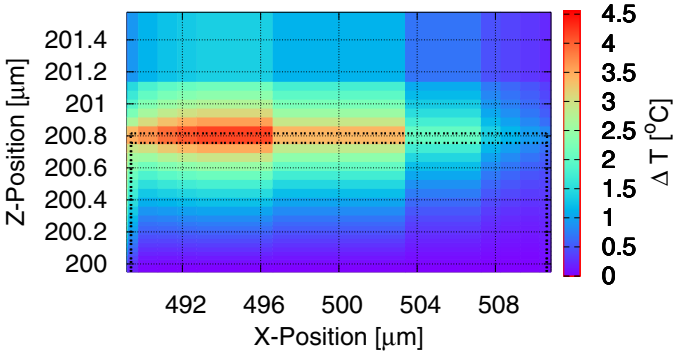

Figure 12. Distribution of ΔT in 2020 (global wire). The region surrounded with dotted lines corresponds to the wire, and the axes are indicated in Figure 4.

will be very small in the design which minimizes the propagation delay. The temperature of the short intra-block wire is, on the other hand, growing more drastically than that of the global wire. Our prediction results point out that we should pay more attention to self-heating in local wires, not to global wires.

5. Conclusion

The self-heating effect is predicted to arise in short intra-block wire with process scaling. The maximum temperature rise from the ambient becomes 27.3°C at the 14 nm process. We reveal that the cross-sectional area of a wire affects self-heating as significantly as the insulating material and power consumption. We compare the self-heating of the global wire with that of the short intra-block wire. From the experimental result, the temperature of the short intra-block wire is growing more drastically than that of the global wire as

technology advances. In the future, self-heating of short intra-block wires can be a threat of the electric resistance increase and the reliability deterioration.

6. Acknowledgement

This work is supported in part by NEDO.

Appendix

Table 1. Parameter set for local wire analysis.

	Year (Tech. node [nm])					
	2005 (90)	2008 (59)	2011 (40)	2014 (28)	2017 (20)	2020 (14)
Metal 1 A/R	1.7	1.8	1.9	1.9	2.0	2.0
Intermediate A/R (Wire)	1.7	1.8	1.9	1.9	2.0	2.0
Intermediate A/R (Via)	1.5	1.6	1.6	1.7	1.8	1.8
V_{dd} [V]	1.1	1.0	1.0	0.9	0.7	0.7
Local Clk [GHz]	5.204	10.972	17.658	28.356	45.535	73.122
Effective dielectric constant	3.1	2.7	2.5	2.4	1.9	1.6
Interlevel metal insulator	FSG	SiOC	Porous Silica			
Thermal conductivity [W/m·K]	0.89	0.39	0.231	0.207	0.162	0.115
L [μm]	108	42	18	11	5	4.5

Table 2. Parameter set for global wire analysis.

	Year (Tech. node [nm])					
	2005 (90)	2008 (59)	2011 (40)	2014 (28)	2017 (20)	2020 (14)
Minimum global wiring pitch [nm]	300	177	120	84	60	42
Global A/R (Wire)	2.2	2.3	2.4	2.5	2.6	2.8
Global A/R (Via)	2	2.1	2.2	2.3	2.4	2.5
$I_{d,sat}$ (NMOS) [μA/μm]	1020	1570	2490	2290	2533	2981
$I_{d,sat}$ (PMOS) [μA/μm]	408	628	996	916	1013.2	1192.4
$C_{g,total}$ [fF/μm]	0.813	0.847	0.859	0.542	0.487	0.362
Buffer size	7.71	5.06	3.98	5.04	4.11	2.76
L [μm]	341.306	171.694	97.629	55.183	35.427	21.645

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