

A Frequency-Dependent Target Impedance Method Fulfilling Both Average and Dynamic Voltage Drop Constraints

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Abstract—Target impedance has been playing a critical role in guiding robust power delivery network (PDN) design. However, traditional methodology has difficulty in associating time domain behavior, such as current profile and voltage drop, with frequency domain PDN impedance. Also, average voltage drop is not explicitly considered in the methodology. These two problems may cause under- or over-designed PDN. This paper proposes a novel frequency-dependent target impedance methodology. The proposed methodology first determines the target impedance shape from the given constraints of average and dynamic voltage drops and exploits a concept of magnitude equivalent frequency (MEF) to bridge the time domain behavior and frequency domain target impedance. Experiment results show that the proposed frequency-dependent target impedance tightly satisfies the given constraints of average and dynamic voltage drops.

Index Terms—target impedance, frequency dependent, average voltage drop, dynamic voltage drop, magnitude equivalent frequency

I. INTRODUCTION

High-quality low-noise power delivery network (PDN) is demanded by every design to ensure its performance. Target impedance methodology is a common practice to guide PDN design. Traditionally, target impedance Z_{target} is defined as:

$$Z_{target} = V_{max_drop}/I, \quad (1)$$

where V_{max_drop} is the maximum allowable voltage drop, and I is the current requirement [1]. Z_{target} is given as a target value for all the frequency range, which could often result in over-designed PDN. On the other hand, existing efforts on frequency dependent target impedance could result in over- or under-designed PDN because of the following two problems.

The first problem is the missing link between time domain and frequency domain. Actual PDN impedance is defined in frequency domain while current profile and voltage drop constraint are given in time domain. Although the current spectrum tells us that dynamic power noise distributes within a certain frequency range, how to determine detailed frequency-dependent target impedance remains an open problem. Refs. [2], [3] try to address this problem by approximating the time domain current profile as triangles. However, such approximation methods suffer from the fact that real current waveform may not be easily simplified to the triangle shape. Ref. [4] suggests to use current spectrum for deriving target impedance. However, the constraint of the worst voltage drop, which is defined in time domain, is difficult to convert into frequency domain.

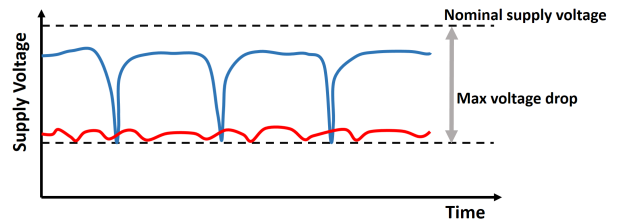


Fig. 1. Two voltage profiles with same max voltage drop.

Secondly, the average voltage drop constraint is not well handled in traditional methodology while Refs. [5], [6] report that average drop has a greater impact on chip performance than dynamic noise. Let us take the voltage profiles in Fig. 1 as an example. Here, given a load current profile, suppose two PDNs having different target impedances that satisfy the same maximum voltage drop constraint. Two voltage profiles corresponding to the different PDNs are depicted in red and blue. The red profile has lower average voltage and smaller ripple, which means chip performance is lower and the PDN for the red profile is over-designed in high-frequency range but under-designed in low-frequency range.

The main contribution of this paper is to propose a new frequency-dependent target impedance methodology, which considers the constraints of both average and dynamic voltage drops. To bridge the design gap between frequency and time domain, a concept of magnitude equivalent frequency (MEF) is proposed to simplify frequency-dependent target impedance design. The proposed methodology is experimentally validated with various current loads.

II. FREQUENCY-DEPENDENT TARGET IMPEDANCE

This section describes how to derive frequency-dependent target impedance under voltage drop constraints for a given load current profile. As discussed with Fig. 1, target impedance should consider the constraints of both average and dynamic voltage drops, which means the target impedance value could vary depending on the frequency. Here, it should be noted that a number of frequency-dependent target impedances exist since the degree of freedom is much larger than the number of the given constraints. Among them, we need to provide a simple frequency-dependent target impedance that has fewer parameters yet satisfies the constraints and has compatibility with PDN design.

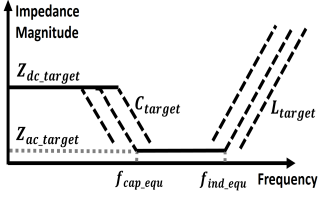


Fig. 2. RLC target impedance.

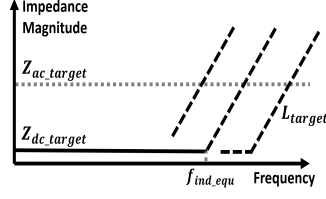


Fig. 3. RL target impedance.

Motivated by this, we propose a frequency-dependent target impedance with four parameters of Z_{ac_target} , Z_{dc_target} , C_{target} , and L_{target} . Z_{ac_target} and Z_{dc_target} denote the target impedance magnitudes at middle frequency range and DC, respectively. Fig 2 shows an example of frequency-dependent target impedance, in which $Z_{dc_target} > Z_{ac_target}$. To minimize PDN design cost, we need to find the minimum required capacitance, which is specified by target capacitance C_{target} , and maximum allowable inductance, which is target inductance L_{target} .

A. Overall Flow and Basic Shapes

As the first step, PDN designers shall determine, or be given, the maximum allowable average and dynamic voltage drops, V_{avg_allow} and V_{dyn_allow} , as PDN design constraints. These constraints determine the basic target impedance shape in frequency domain.

Supposing the average load current is I_{avg} , the target impedance in low frequency range including DC is:

$$Z_{dc_target} = V_{avg_allow}/I_{avg}. \quad (2)$$

As for the dynamic voltage drop constraint, we first define the magnitude of load current $I(t)$ and voltage $V(t)$ as:

$$\begin{aligned} \text{Mag}(I(t)) &= I_{max} - I_{avg}, \\ \text{Mag}(V(t)) &= V_{avg} - V_{min}, \end{aligned} \quad (3)$$

where I_{max} is the maximum value of $I(t)$, I_{avg} is the average value of $I(t)$, V_{avg} is the average load voltage, and V_{min} is the minimum load voltage. The target impedance in the middle frequency range is:

$$Z_{ac_target} = V_{dyn_allow}/\text{Mag}(I(t)). \quad (4)$$

Z_{ac_target} can be either larger or smaller than Z_{dc_target} , and then two types of target impedance shape exist.

Fig. 2 shows the target impedance shape in case of $Z_{dc_target} > Z_{ac_target}$, which is called RLC type. In this case, mitigating dynamic voltage drop is the main PDN design challenge. The PDN design goal is to find the minimum of required target capacitance C_{target} and the maximum of allowable target inductance L_{target} so that Z_{ac_target} can be met with the minimal design resource.

Fig. 3 corresponds to the case of $Z_{dc_target} < Z_{ac_target}$, where the average voltage drop is the severer constraint than the dynamic voltage drop. This shape is called RL type. The goal is to find L_{target} , so that Z_{ac_target} can be met with the minimal design resource. Another special case of $Z_{dc_target} = Z_{ac_target}$ is treated as a corner case of RL-type target impedance. Fig. 4

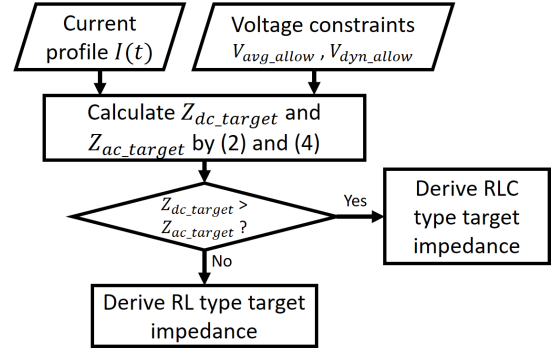


Fig. 4. Overall flow of frequency-dependent target impedance methodology.

shows the overall flow of target impedance derivation, where current profile $I(t)$ and voltage constraints of V_{avg_allow} and V_{dyn_allow} are given to the flow. The following explains how to derive C_{target} and L_{target} using a concept of MEF.

B. Magnitude Equivalent Frequency (MEF)

The key idea of MEF is, instead of analyzing the detailed current waveform, we use a sine waveform current to reproduce the same magnitude of the voltage noise. The frequency of this sine waveform is defined as MEF. Once MEF is obtained for capacitance dominant impedance, we can use MEF as the corner frequency f_{cap_equ} to C_{target} in Fig. 2. Similarly, MEF for inductance dominant impedance is denoted as f_{ind_equ} , which is used as the corner frequency to derive L_{target} . The derivation of C_{target} and L_{target} will be discussed in the next subsection. The remaining of this subsection proves the existence of such MEFs and discusses the property of MEF.

For capacitance dominant impedance, supposing the magnitudes of original load current $I(t)$ and voltage $V(t)$ are bounded, which is always hold in actual PDNs, we necessarily have a sine waveform current $I_s(t)$ that has the same magnitude, i.e. $\text{Mag}(I_s(t)) = \text{Mag}(I(t))$. Then, $\text{Mag}(V_s(t))$ becomes a function of frequency for capacitance C dominant impedance:

$$\text{Mag}(V_s(t)) = \text{Mag}(I_s(t))/(2\pi C f_{cap_equ}). \quad (5)$$

Therefore, we can find the frequency of sine waveform f_{cap_equ} that achieves $\text{Mag}(V_s(t)) = \text{Mag}(V(t))$. Hereafter, we denote f_{cap_equ} as capacitance MEF of load current. The existence of this capacitance MEF can be summarized by:

Theorem 1. Let $I(t)$ be load current profile and $V(t)$ be corresponding PDN voltage profile. If $V(t)$ and $I(t)$ are bounded, $\text{Mag}(V(t))$ across capacitance dominant impedance can be reproduced by current $I_s(t) = \text{Mag}(I(t)) \cdot \sin(2\pi f_{cap_equ} \cdot t)$.

Hereafter, such $I_s(t)$ is called magnitude equivalent current (MEC). Similarly, for inductance dominant impedance, inductance MEF f_{ind_equ} also exists.

Theorem 2. Let $I(t)$ be load current profile, $V(t)$ be corresponding PDN voltage profile. If $I(t)$ and $V(t)$ are bounded, $\text{Mag}(V(t))$ across inductance dominant impedance can be reproduced by MEC $I_s(t) = \text{Mag}(I(t)) \cdot \sin(2\pi f_{ind_equ} \cdot t)$.

Furthermore, MEF value is independent of capacitance or inductance value. That is:

Theorem 3. Let $V(t)$ be the voltage profile for the original current profile, and $V_s(t)$ be the voltage profile for the MEC to the original current profile. Then, for all the capacitance and inductance dominant impedances, $\text{Mag}(V_s(t)) = \text{Mag}(V(t))$ hold.

With the definition of (3), the magnitudes of current and voltage satisfy the properties below, where N_A and N_B are arbitrary positive real numbers:

$$\begin{aligned} \text{Mag}(N_A \cdot I(t)) &= N_A \cdot \text{Mag}(I(t)), \\ \text{Mag}(N_B \cdot V(t)) &= N_B \cdot \text{Mag}(V(t)). \end{aligned} \quad (6)$$

Supposing a sine MEC current $I_s(t)$ at MEF, then $\text{Mag}(I_s(t)) = \text{Mag}(I(t))$ and $\text{Mag}(V_s(t)) = \text{Mag}(V(t))$ are satisfied for capacitance C dominant impedance. Then for another capacitance C' ($= N_C \cdot C$, where $N_C > 0$) dominant impedance, the corresponding voltage magnitude for $I_s(t)$ is:

$$\text{Mag}(V'_s(t)) = \frac{\text{Mag}(I_s(t))}{C' \cdot 2\pi f_{cap_equ}} = \frac{\text{Mag}(V_s(t))}{N_C}. \quad (7)$$

Also, $\text{Mag}(V(t))$ is inversely proportional to C , which can be explained using Fourier series of $V(t)$ and $V'(t)$, where $V'(t)$ is the voltage profile for C' . The coefficient for the same trigonometric function is N_C times different. Combining this relation with (6), $\text{Mag}(V'(t))$ becomes

$$\text{Mag}(V'(t)) = \text{Mag}\left(\frac{V(t)}{N_C}\right) = \frac{\text{Mag}(V(t))}{N_C} = \frac{\text{Mag}(V_s(t))}{N_C}. \quad (8)$$

Since the rightmost terms of (7) and (8) are identical, $\text{Mag}(V'_s(t)) = \text{Mag}(V'(t))$ still holds for different capacitances with the same MEC. We can draw similar conclusion for inductance dominant impedance, and then Theorem 3 is proved.

We have proved MEFs exist for capacitance and inductance dominant impedances, and MEFs are independent of capacitance and inductance value.

C. Derive target inductance and target capacitance

This section explains how to derive MEF and obtain target inductance and target capacitance.

MEF can be derived for any capacitance and inductance, as suggested in Theorem 3, and then we prepare a characterization circuit for capacitance MEF f_{cap_equ} in Fig. 5 and the circuit for inductance MEF f_{ind_equ} in Fig. 6, where the values of R , C_{test} , and L_{test} can be arbitrarily set by you. Given the load current profile $I(t)$, the output voltage $V_{C_{test}}(t)$, $V_{L_{test}}(t)$, and their magnitudes $\text{Mag}(I(t))$, $\text{Mag}(V_{C_{test}}(t))$ and $\text{Mag}(V_{L_{test}}(t))$ are obtained by simulation. Note that although the values of C_{test} and L_{test} do not impact MEF thanks to Theorem 3, we still need to select sufficiently large capacitance and inductance to ensure the circuit impedance is dominated by capacitance or inductance.

When the impedance of RC characterization circuit is capacitance C_{test} dominant, f_{cap_equ} is derived as:

$$f_{cap_equ} = \frac{\text{Mag}(I(t))}{\text{Mag}(V_{C_{test}}(t)) 2\pi C_{test}}. \quad (9)$$

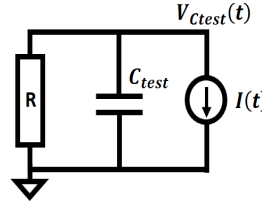


Fig. 5. RC test circuit.

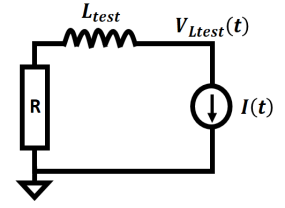


Fig. 6. RL test circuit.

Algorithm 1 Derive target inductance and target capacitance

Input: $I(t)$

Main Routine :

- 1: **if** $\text{Mag}(V_{C_{test}}(t)) < \alpha \cdot \text{Mag}(V(t))_{\text{ref}}$ **then**
 - 2: Derive capacitance MEF f_{cap_equ} by (9)
 - 3: Derive target capacitance C_{target} by (11)
 - 4: **else**
 - 5: Abort with a message “Select larger C_{test} ”.
 - 6: **end if**
 - 7: **if** $\text{Mag}(V_{L_{test}}(t)) > (1/\alpha) \cdot \text{Mag}(V(t))_{\text{ref}}$ **then**
 - 8: Derive inductance MEF f_{ind_equ} by (10)
 - 9: Derive target inductance L_{target} by (12)
 - 10: **else**
 - 11: Abort with a message “Select larger L_{test} ”.
 - 12: **end if**
-

Similarly, when the RL characterization circuit is dominated by inductance L_{test} , f_{ind_equ} is derived as:

$$f_{ind_equ} = \frac{\text{Mag}(V_{L_{test}}(t))}{\text{Mag}(I(t)) 2\pi L_{test}}. \quad (10)$$

For RLC-type target impedance in Fig. 2, target impedance at middle frequency Z_{ac_target} should be met between capacitance MEF f_{cap_equ} and inductance MEF f_{ind_equ} . For RL type-target impedance in Fig. 3, target impedance at middle frequency Z_{ac_target} should be satisfied between DC and inductance MEF f_{ind_equ} . The corresponding target capacitance and target inductance are

$$C_{target} = \frac{1}{2\pi f_{cap_equ} Z_{ac_target}}, \quad (11)$$

$$L_{target} = \frac{Z_{ac_target}}{2\pi f_{ind_equ}}. \quad (12)$$

The derivation of target inductance L_{target} and target capacitance C_{target} can be summarized as Algorithm 1. Now, we can derive all the parameters to define the proposed frequency-dependent target impedance, which are C_{target} in (11), L_{target} in (12), Z_{ac_target} in (4), and Z_{dc_target} in (2).

III. EXPERIMENT RESULTS

This section verifies whether the proposed target impedance can satisfy the constraints of average and dynamic voltage drops. For this evaluation, we need a simulatable PDN that traces the frequency-dependent target impedance. On the other hand, the derived target impedance is a piecewise curve in frequency domain, and the exact PDN realization is difficult.

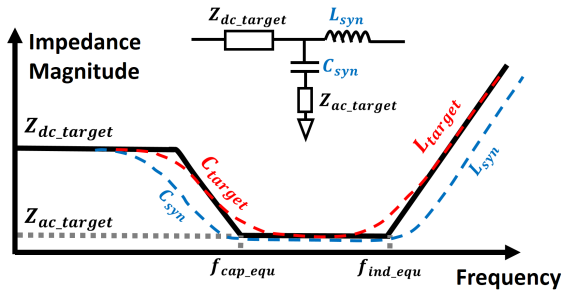


Fig. 7. RLC-type target impedance synthesis.

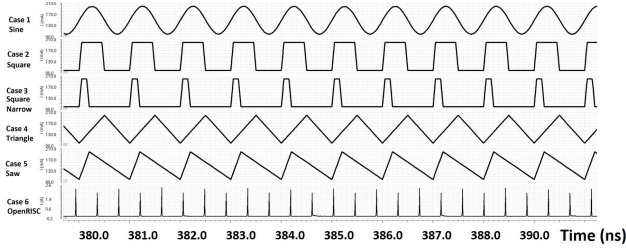


Fig. 8. Load current profiles at 1 GHz for experiments. From top to bottom: Sine, Square, Narrow square, Triangle, Sawtooth, and OpenRISC.

Instead, we synthesize a T-shape RLC circuit in Fig. 7 that tightly tracks the piecewise target impedance. When L_{target} and C_{target} are used for the T-shape circuit, the voltage drop constraints can be violated because the impedance of the T-shape circuit is larger at the corner frequencies than the piecewise target impedance, which is depicted as the red dashed line in Fig. 7. To avoid this violation, we use larger capacitance $C_{syn} = 10 \cdot C_{target}$, and smaller inductance $L_{syn} = 0.1 \cdot L_{target}$ in this paper. This minor modification can ensure the actual impedance is close to Z_{ac_target} at the corner frequencies, which is plotted as the blue dashed line. It should be noted that this circuit synthesis is just one method and various approaches could be adopted in actual PDN design.

For evaluating the applicability of the proposed methodology to various waveforms, we prepared six load current profiles in Fig. 8. Cases 1-5 are artificial load waveforms. Cases 1-5 suppose 1 GHz operation, and their fluctuations range 100 mA to 200 mA. Case 6 is obtained from 32-bit OpenRISC core logic operation.

For case 1 of sine waveform, we confirmed that the inductance MEF and capacitance MEF are 1.0 GHz as we expected. In cases 2 and 3, square waveforms with different widths of 400 ps and 100 ps are used to mimic sudden and short-duration module activations. In cases 4 and 5, triangle waveforms with different rising times of 500 ps and 200 ps aim to mimic typical digital circuit load. In our experiments, we set the constraints of maximum allowable voltage drop as $V_{avg_allow}=70$ mV and $V_{dyn_allow}=10$ mV. Given the nominal voltage as 800 mV, the minimal allowable voltage is 720 mV¹. Table I lists the derived values of Z_{dc_target} , Z_{ac_target} , C_{target} and L_{target} , where these four parameters define the proposed frequency-dependent target impedance. In the last two columns, the load minimal voltage V_{min} is obtained from

¹Here, only RLC-type impedance case is presented due to page limitation.

TABLE I
DERIVED TARGET IMPEDANCE PARAMETERS, AND AVERAGE AND MINIMAL VOLTAGES.

| | Z_{dc_target} (m Ω) | Z_{ac_target} (m Ω) | C_{target} (nF) | L_{target} (pH) | V_{avg} (mV) | V_{min} (mV) |
|-----------|-----------------------------------|-----------------------------------|----------------------|----------------------|-------------------|-------------------|
| Case 1 | 466.6 | 200.0 | 0.8 | 31.8 | 730.0 | 722.5 |
| Case 2 | 482.7 | 181.8 | 1.2 | 5.0 | 730.0 | 722.2 |
| Case 3 | 608.7 | 117.6 | 0.7 | 5.0 | 729.9 | 720.9 |
| Case 4 | 466.6 | 200.0 | 0.6 | 24.7 | 730.0 | 722.5 |
| Case 5 | 466.6 | 200.0 | 0.5 | 19.8 | 730.0 | 722.5 |
| Avg. Err. | - | - | - | - | 0.0003% | 0.3% |
| Case 6 | 251.9 | 12.5 | 0.35 | 0.01 | 790.2 | 760.6 |
| Err. | - | - | - | - | 0.02% | 0.07% |

the simulation with the synthesized T-shape RLC circuit. The average error of V_{avg} and V_{min} are 0.0003% and 0.3%, which indicates the PDNs that satisfy the frequency-dependent target impedance meet the given constraint of average and maximum voltage drops.

For OpenRISC case of 6, the load design is synthesized with NanGate 15 nm Open Cell Library at 1.2 GHz. The nominal voltage is 800 mV, and the constraints of $V_{avg_allow}=10$ mV and $V_{dyn_allow}=30$ mV are given. Then, the minimum allowable voltage is 760 mV. RLC-type target impedance is derived based on Z_{dc_target} , Z_{ac_target} , C_{target} , and L_{target} , which is listed in Table I. We synthesize this target impedance circuit as a T-shape RLC circuit in Fig. 7, and run the simulation. The measured $V_{min}=760.6$ mV, and $V_{avg}=790.2$ mV. These results indicate that the proposed frequency-dependent target impedance works well for actual processor workload including various frequency components.

IV. CONCLUSION

In this paper, we have proposed a new frequency-dependent target impedance methodology that satisfies the constraints of both average and dynamic voltage drops. Given the voltage drop constraints and load current profile, frequency-dependent target impedance is derived. We experimentally confirmed that the synthesized target impedance satisfied the constraints with less than 0.1% error in actual processor load case.

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