Negative and Positive Muon-induced SEU Cross Sections in 28-nm and 65-nm Planar Bulk CMOS SRAMs

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Abstract—In this paper, we compare the negative and positive muon-induced SEU event cross sections of 28-nm and 65-nm planar bulk CMOS SRAMs. Our measurement results show a 3.6 X increase in muon-induced SEU event cross section from 65-nm to 28-nm technology, and negative muon-induced SEU event cross section is 3.3 X larger compared to positive muons at 28-nm technology. This result is consistent with the previous works reporting muon-induced SEU event cross section increases with technology scaling. The measured result also suggests the contribution of direct ionization to the total SEU event cross section is 54.1 % at 28-nm node with operating voltage of 0.6 V while it is 1.8 % at 65-nm node with 0.9 V.

Index Terms—single event upset, SRAMs, muons, direct ionization, muon capture, technology scaling

I. INTRODUCTION

Secondary cosmic ray is the main source of soft error in a terrestrial environment, and then lots of efforts have been devoted to neutron-induced soft errors for estimation and mitigation. On the other hand, in the nano-scale technology era, muons are drawing attention as a potential source of soft error [1].

One of the major concerns about muon-induced soft errors is whether the SEU (Single Event Upset) cross section will raise with technology scaling [2]. Sierawski et al. measured and compared positive muon-induced SEU cross sections in 55-nm, 45-nm, and 40-nm bulk CMOS SRAMs and showed a growing tendency with technology scaling [3]. With simulation, [3] also discussed the possibility of further increase in muon-induced SEU cross section. Seifert et al. conducted positive muon irradiation on 32-nm planar, 22-nm FinFET, 14-nm FinFET SRAMs [4]. Although they showed a decrease from 32-nm planar to 22-nm FinFET devices, within the same structure of FinFET, SEU cross section seems to increase slightly from 22-nm to 14-nm FinFET.

On the other hand, negative muons should be investigated with the technology scaling since they have a larger cross section of the events depositing large charge compared to positive muons. Fig. 1 illustrates the difference in charge deposition mechanism between negative and positive muons. Both positive and negative muons deposit charge due to direct ionization. Also, a capture reaction of low-energy negative muon generates secondary ions, and they deposit larger charge

than direct ionization. We conducted negative muon irradiation experiments for 65-nm bulk SRAMs [5], [6] and showed the SEU bit cross section [1] of negative muons is larger than that of positive muons, especially in bulk devices, where at least 6.2 X difference was observed between the SEU bit cross sections of negative and positive muons. However, the cross section of negative muon-induced SEU is reported only at a single node of 65-nm, and the trend for technology scaling cannot be discussed with experimental data even though it is highly desired.

Also, the proportions of muon capture and direct ionization to the SEU cross section are interesting and worth investigating. In 65-nm technology, the muon capture is dominant since the negative muon-induced SEU cross section is much higher than that of positive muon [3] as mentioned above, but the contribution of direct ionization to the total cross section is expected to increase in finer technologies due to a decrease in critical charge. For this purpose, we need to evaluate SEU cross sections at more advanced technology nodes both for positive and negative muon. These comparisons will be useful
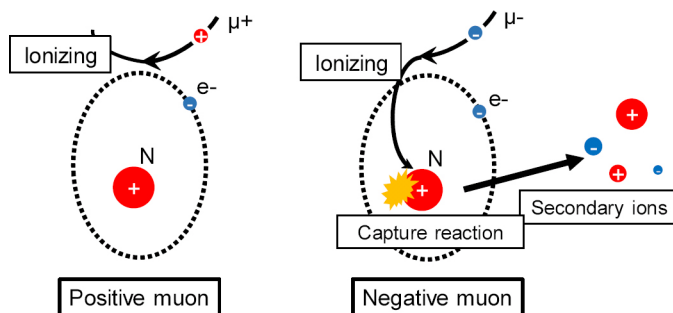

Fig. 1: Both positive and negative muons could deposit charge by ionizing. However, only negative muons can deposit charge by capture reaction when their energy is low enough. Capture reaction releases ions that deposit larger energy than direct ionization deposits.

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[1]In this paper, we define two cross sections: the first one is based on the number of error bits, which is hereafter called bit cross section, and the latter is based on the number of events and called event cross section.

for the better understanding of secondary cosmic rays-induced SER (Soft Error Rate) at the terrestrial environment since muons take more than 60 % in proportion of fluxes in the total cosmic rays.

In this paper, we compare the negative, positive, and total muon-induced SEU cross sections of 28-nm and 65-nm planar bulk CMOS SRAMs. First, we newly measure the SEU cross section of 28-nm SRAM in the irradiation experiment with monoenergetic negative muon source. For comparison, the SEU cross sections in 65-nm SRAMs are imported from [5] and compared with the measured cross sections in 28-nm SRAMs. The comparison result shows an increase in both negative muon- and direct ionization-induced SEU cross sections with technology scaling.

The rest of this paper is organized as follows. Section II presents measurement results of muon-induced SEU cross section of 28-nm SRAM, and Section III compares the cross sections of 28-nm and 65-nm SRAMs and discusses the contributions of direct ionization and muon capture to the total SEU cross section. Finally, concluding remarks are given in Section IV.

II. EXPERIMENT OF NEGATIVE AND POSITIVE MUON IRRADIATION ON 28-NM SRAMS

For technology comparison, we conducted negative and positive muon irradiation experiments for 28-nm planar bulk 1-MB SRAM whose half cells are in Deep N-Well (DNW), and other half cells are not. We write a checkerboard pattern to the SRAMs and hold the data until reading. All the bits on the chips are written and read every 20 seconds. Due to a relatively short period of read and write operations, the test is regarded as a static test. The beam facility of MUSE (MUon SciEnce facility) in MLF (Material and Life science experimental Facility) at J-PARC (Japan Proton Accelerator Research Complex) [7], [8] provides both negative and positive monoenergetic muons with 5 % energy deviation. To make a fair comparison between 28-nm and 65-nm technology nodes, it should be clarified that the beam facility and irradiation setup are the same with the 65-nm SRAM test in [5]. The energy of muon should be adjusted to make most of the muons stop near the transistor similar to the 65-nm experiment, which makes LET (Linear Energy Transfer) and the possibility of negative muon being captured maximum. This energy adjustment is performed such that the SEU cross section becomes maximum. Consequently, we can collect as many errors as possible within the limited beam time. Note that this SRAM chip is mounted on a ceramic package and is irradiated from BEOL side without a cover. A vacuum chamber is not applied.

Fig. 2 shows the result of energy scanning, where the x-axis is the energy of negative muon and the y-axis is the measured SEU bit cross section at 0.6 V. Each error bar represents one standard deviation. The irradiation time for each energy is around 15 minutes. From this figure, we observe that the SEU bit cross section reaches the maximum at 2.07 MeV, which indicates more muons stop near the transistors inside the chip compared with other energies.
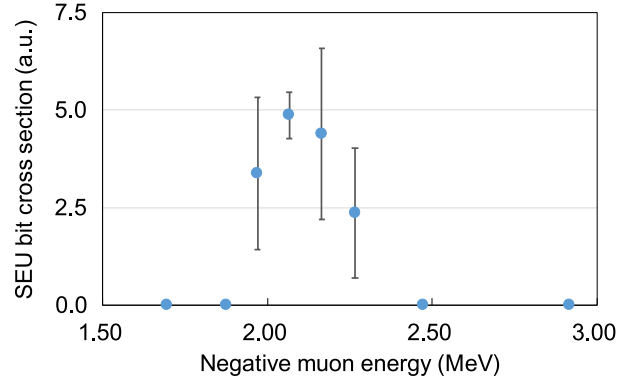

Fig. 2: Result of energy scanning to find the energy at which muon stops near the transistor. Negative muon source is utilized. The SRAM operation voltage is 0.6 V.

In our experiment, the stopping energy was scanned with the negative muon beam due to its relatively large cross section compared with the positive muon. Though Refs. [9], [10] point out that negative muons have a slightly longer flight length than positive muons with the same energy, our previous work [5] has not observed a distinct peak difference between positive and negative muons, which is probably attributed to the 5 % energy deviation of the muon beam concealing the difference of flight length. Due to the longer time necessary to collect statistically enough errors to identify the stopping energy of positive muon, we chose the stopping energy of positive muon as the same as that of negative muon and executed a long-time run.

The total upset events observed in the irradiation experiment are shown in Table I. We distinguish the SBUs (Single Bit Upset) with MCUs (Multiple Cells Upsets) by the locations of the upset bits in the bit map. When the adjacent bits upset at the same read and write cycle, an MCU is supposed to be observed. However, the adjacent upsets might be induced by multiple muons, which are referred to as pseudo MCUs here. To show the reliability of the data set, the maximum percentage of two-bit pseudo MCUs is calculated in the following. The probability of SBU is calculated as

$$P_{SBU} = \frac{N_{SBU}}{N_{TotalBits}}, \tag{1}$$

where N_{SBU} represents the number of SBUs in a period of irradiation, and $N_{TotalBits}$ stands for the total number of bits under test. Here, we consider all the upsets as SBUs to maximize P_{SBU} and consequently the probability of pseudo MCU. Then, the probability of pseudo MCU is calculated as follows.

$$P_{pseudoMCU} = {}_8C_1 \cdot P_{SBU}^2, \tag{2}$$

where ${}_8C_1 = 8$ stands for eight possible positions next to the bit cell of interest in either horizontal, vertical or diagonal direction. The maximum number of MCU is calculated as the product of $N_{TotalBits}$ and $P_{pseudoMCU}$, and then the

TABLE I: Total number of SBUs and MCUs observed in the irradiation experiments. A noticeable point is that MCUs are observed at both 0.6 V and 1.5 V.

	Voltage (V)	Energy (MeV)	Test time (a.u.)	# of SBUs	# of MCUs
	0.6	2.07	230	41	8
	0.6	2.16	15	1	1
	0.6	2.26	14	1	1
Negative muon	0.6	2.47	14	0	0
	0.6	2.91	14	0	0
	0.6	1.97	15	3	0
	0.6	1.88	15	0	0
	0.6	1.69	15	0	0
	1.5	2.07	20	0	1
	1.0	2.07	15	0	0
Positive muon	0.6	2.07	103	7	0

maximum percentage of pseudo MCU over the number of measured MCUs N_{MCU} is

$$\frac{N_{TotalBits} \cdot P_{pseudoMCU}}{N_{MCU}}. \qquad (3)$$

The calculated percentages of pseudo two-bit MCU at 0.6 V is 9.25×10^{-7} %. We also notice that even at 1.5 V, a 4-bit MCU is still observed and its probability of being a pseudo MCU is 3.39×10^{-8}. On the other hand, due to the small SRAM capacity and limited beam time, we could not observe enough number of MCUs to analyze the spatial patterns.

III. DISCUSSION

With the data of 65-nm SRAMs in [5], we compare the negative and positive muon-induced SEU event cross sections for 28-nm and 65-nm planar bulk SRAMs. For mitigating statistical uncertainties, the two technologies are compared with the conditions having the largest numbers of errors, which are operating voltage of 0.9 V and muon energy of 6.62 MeV (stopping energy for this device) for 65-nm and 0.6 V and 2.07 MeV for 28-nm. Here, it should be noted that this stopping energy difference comes from the package setup, not from the technology difference. Due to 65-nm SRAMs being fabricated with DNW, only the upsets in 28-nm SRAM cells with DNW are used for comparison. Fig. 3 shows the result of a comparison between 65-nm and 28-nm. Each error bar represents one standard deviation.

A. Comparison result: negative v.s. positive muons, and 28-nm v.s. 65-nm

We first compare negative and positive muons for each node in Fig. 3. We observe negative muon-induced SEU event cross section is 2.3 X larger at 0.6 V in 28-nm node and 104.3 X larger at 0.9 V in 65-nm node than positive muon-induced ones. It is confirmed that negative muon has higher error-inducing ability than positive muon at both 28-nm and 65-nm nodes.

As for technology comparison, Fig. 3 shows that the negative muon-induced SEU event cross section increases 2.8 X from 65-nm to 28-nm. Meanwhile, the increase in positive
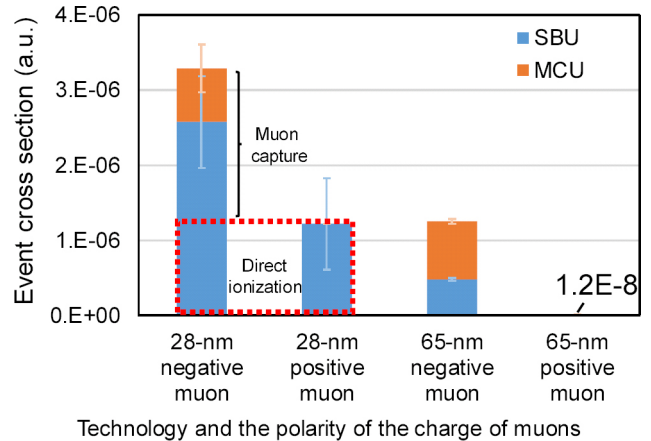

Fig. 3: Comparison of SEU event cross sections in 28-nm and 65-nm SRAMs. The error bar stands for one standard deviation. The negative muon-induced SEU event cross section in 28-nm SRAMs is 2.8 X, and the total event cross section is 3.6 X larger than those in 65-nm SRAMs. Due to 65-nm SRAMs being fabricated with DNW option, only the data upsets in 28-nm SRAM cells with DNW are utilized for comparison. The event cross section difference of negative and positive muon is supposed to be due to capture reaction. Thus, the contributions of direct ionization and muon capture could be decomposed.

muon-induced cross section would be 101.5 X and the total increase including negative and positive muon-induced SEU event cross sections would be 3.6 X from 65-nm to 28-nm technology nodes. The event cross section difference of negative and positive muon is supposed to be due to capture reaction since positive muons are thought to be able to induce SEUs only by direct ionization. Therefore, the larger increasing rate of positive muon-induced SEU cross section from 65-nm to 28-nm node suggests that direct ionization could deposit charge large enough to cause upsets. This observation will be discussed in the next subsection.

As for MCU and SBU, we observe that the SBU event cross section increases while the MCU event cross section decreases from 65-nm to 28-nm technology. In 65-nm technology, we observed almost all the errors in the cells sharing the same P-well [5], and our analysis suggests a large possibility of PBA (Parasitic Bipolar Action)-induced MCUs. However, for 28-nm technology, we do not obtain the specific information on well and well tap placement. But fortunately, half of SRAM cells are located in DNW in the 28-nm SRAM. This option is thought to activate PBA and lead to a larger scale MCUs. To evaluate the MCU scales, we counted the bit cross sections and separated them into cells with or without DNW as shown in Fig. 4. From this figure, we observe a slight increase in MCU bit cross section in the cells with DNW, and it may suggest a possibility of PBA while it is still within the range of one standard deviation. The analysis of MCU pattern and mechanism induced by negative muon in 28-nm SRAMs is
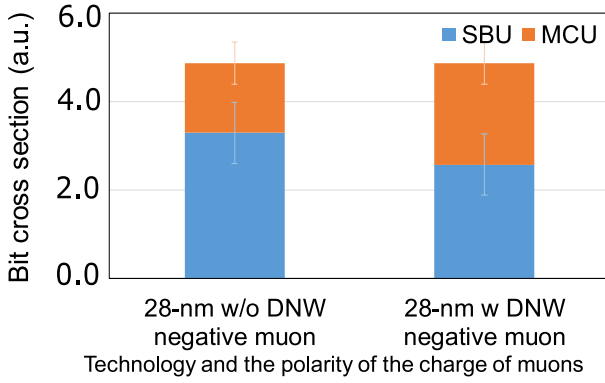
Fig. 4: Comparison of bit cross sections with and without DNW. A slight increase in MCU bit cross section in cells with DNW is observed, which may suggest the existence of PBA in 28-nm bulk SRAM.

included in our future work.

B. Analyzing the comparison results with deposited charge

To explain the reason why direct ionization-induced SEUs increase with technology scaling, the analysis of deposited charge is provided. Fig. 5 shows the accumulated probabilities of the amount of charge deposited by positive and negative muons, σ_{acP} and σ_{acN}, which were obtained by particle and heavy ion transport code system (PHITS, Particles and Heavy Ions Transport code System) with the structure of 65-nm transistor [5]. It indicates that negative muon has a higher probability of large charge deposit than positive muon while negative and positive muons have a similar probability of low charge deposit, which is consistent with our measurement results that under positive muon irradiation, no MCU was observed in either 28-nm or 65-nm nodes.

In this case, as the critical charge Q_c decreases with technology scaling [11], the ratio of the accumulated probability of negative muon to that of positive muon, which is $\sigma_{acN}(Q_c)/\sigma_{acP}(Q_c)$, becomes smaller. This tendency explains why the difference of SEU event cross section between negative and positive muons is smaller at 28-nm in Fig. 3 since the 28-nm SRAM at 0.6 V has smaller critical charge than the 65-nm SRAM at 0.9 V.

Supposing the direct ionization-induced SEU event cross sections for positive and negative muons are the same, we can estimate the contributions of direct ionization and muon capture as marked in Fig. 3. We notice that both direct ionization and muon capture cause soft errors in 28-nm SRAM while muon capture induces most of the errors in 65-nm SRAM. The ratio of direct ionization-induced SEU to the total SEU taking into account both positive and negative muon is 54.1 % at 28-nm and 1.8 % at 65-nm. This result suggests that the charge deposited by muon direct ionization contributes to more upsets in 28-nm than that in 65-nm and this tendency could be more significant in 20-nm technology.
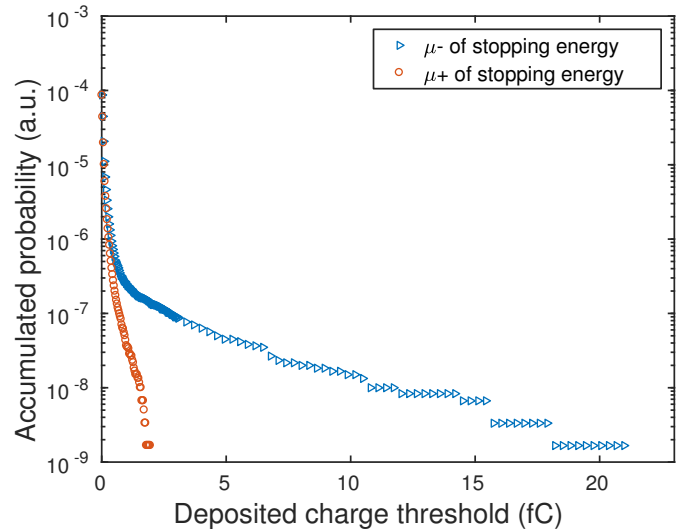

Fig. 5: Accumulated probability of event is shown with the threshold charge. The y-axis shows the possibility of a muon-induced event depositing the charge which is larger than the corresponding value at x-axis. The possibility is calculated with PHITS supposing the muons with stopping energy are injected into the silicon. The volume for charge calculation is $0.52 \times 0.08 \times 0.40 \mu m^3$ supposing 65-nm node.

IV. CONCLUSION

We confirm that with technology scaling, both negative and positive muon-induced SEU event cross sections increase, and the total increasing rate is 3.6 X from 65-nm to 28-nm bulk SRAM. The comparison between positive and negative muon-induced SEU event cross sections suggests the 54.1 % and 1.8 % of SEU is caused by direct ionization at 28-nm and 65-nm technology, respectively. At both 0.6 V and 1.5 V, negative muon-induced MCUs are observed in the 28-nm SRAM.

ACKNOWLEDGMENT

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