IEICE TRANS. ELECTRON., VOL.E102–C, NO.4 APRIL 2019

PAPER Special Section on Solid-State Circuit Design — Architecture, Circuit, Device and Design Methodology

Analyzing Impacts of SRAM, FF and Combinational Circuit on Chip-Level Neutron-Induced Soft Error Rate

Wang LIAO[†a)], ***Nonmember and*** **Masanori HASHIMOTO**[†b)], ***Member***

SUMMARY Soft error jeopardizes the reliability of semiconductor devices, especially those working at low voltage. In recent years, silicon-on-thin-box (SOTB), which is a FD-SOI device, is drawing attention since it is suitable for ultra-low-voltage operation. This work evaluates the contributions of SRAM, FF and combinational circuit to chip-level soft error rate (SER) based on irradiation test results. For this evaluation, this work performed neutron irradiation test for characterizing single event transient (SET) rate of SOTB and bulk circuits at 0.5 V. Using the SBU and MCU data in SRAMs from previous work, we calculated the MBU rate with/without error correcting code (ECC) and with 1/2/4-col MUX interleaving. Combining FF error rates reported in literature, we estimated chip-level SER and each contribution to chip-level SER for embedded and high-performance processors. For both the processors, without ECC, 95% errors occur at SRAM in both SOTB and bulk chips at 0.5 V and 1.0 V, and the overall chip-level SERs of the assumed SOTB chip at 0.5 V is at least 10 x lower than that of bulk chip. On the other hand, when ECC is applied to SRAM in the SOTB chip, SEUs occurring at FFs are dominant in the high-performance processor while MBUs at SRAMs are not negligible in the bulk embedded chips.

key words: *soft error rate, chip-level, SRAMs, flip flops, combinational circuits*

1. Introduction

In recent decade, with the trend of reducing power dissipation, transistors that are suitable for low voltage operation are shifted to mass production. While improving the conventional bulk CMOS transistors to fit low voltage operation, the transistors of a new structure of fully depleted silicon-on-insulator (FD-SOI) is one of those promising devices [1]. Moreover, silicon-on-thin-box (SOTB), which is a FD-SOI device with thinner BOX (buried oxide) and SOI layers of 10 nm and 12 nm, respectively, was proposed to improve controllability of ultra-low voltage (0.6 V and below) operation [5]. On the other hand, the lower operation power makes soft error occur more easily due to lower critical charge [2]. But compared to conventional bulk devices, SOTB devices have better immunity to soft errors thanks to the insulator layer between the substrate and SOI layer [3], [4]. For covering a wide range of reliability demand, the soft error immunity of SOTB chips needs to be evaluated and compared with that of conventional bulk chips, especially at low operation voltage.

For assessing the soft error immunity of devices under low operation voltage, Kobayashi *et al.* measured the soft error rate (SER) of flip flop (FF) of bulk and SOTB circuits at the supply voltage between 0.6 V to 1.2 V [6]. Hirokawa *et al.* measured single bit upset (SBU) and multiple cell upsets (MCU) in SOTB and bulk SRAM at 0.4 V to 1.0 V [7]. Furuta *et al.* measured single event transient (SET) in SOTB and bulk circuits at 1.2 V [8].

To provide a comprehensive understanding of soft error immunity in low operation voltage, this paper evaluates the chip-level neutron-induced SER of SOTB and bulk circuits at 0.5 V and 1.0 V and investigates the contributions of SRAM, FF and combinational circuit to the chip-level SER. For achieving this, we fabricated SOTB and bulk test chips and measured SET rate of SOTB and bulk combinational circuits at 0.5 V due to lack of SET rate at ultra low voltage. Combining with previously reported SERs of FF and SRAM [6], [7], chip-level SER of processors designed with SOTB and bulk CMOS is calculated. We compare the composition of chip-level SER between embedded and high-performance processors with and without ECC. A preliminary analysis result is presented in [9]. This paper newly calculates the rate of multiple bits upsets (MBUs) without or with error correcting code (ECC) using the previous data of MCU to evaluate the influence of soft errors in SRAM to data path in practical systems. Moreover, MBU rates are estimated with 1/2/4-col MUX bit interleaving. Then, the chip-level SER and the composition analysis is updated with the MBU rates to provide with a better understanding of the necessity of ECC for SRAM and reliability-demanding systems.

The rest of this paper is organized as follows. Section 2 explains test chips for irradiation test and shows measurement results. Section 3 discusses multiple bit upsets in the SRAM devices with and without ECC. Section 4 estimates chip-level SER of SOTB and bulk processors and discusses the contributions of SRAM, FF and combinational circuit to the chip-level SER of embedded and high-performance processors.

2. SET Rate Measurement

2.1 Test Chip Design for SET Measurement

We designed and fabricated test chips to evaluate the number of SET occurrence in SOTB and bulk circuits. Figure 1 shows a test group for SET measurement. In the SET measurement mode, SEL1 and SEL2 are set to low to compose

Manuscript received July 31, 2018.
Manuscript revised November 30, 2018.
[†]The authors are with the Department of Information Systems Engieering, Osaka University, Suita-shi, 565–0871 Japan.
a) E-mail: wang.liao@ist.osaka-u.ac.jp
b) E-mail: hasimoto@ist.osaka-u.ac.jp
DOI: 10.1587/transele.2018CDP0004

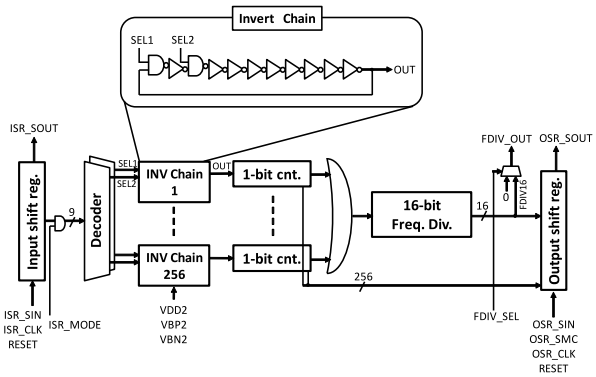

Fig. 1 One test group for SET measurement.

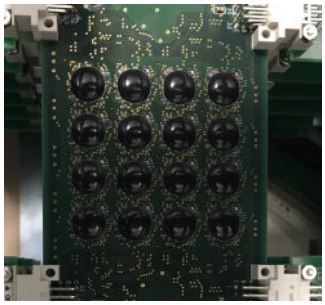

Fig. 2 Chip board used in test. ©[2018] IEEE. Reprinted, with permission, from [9].

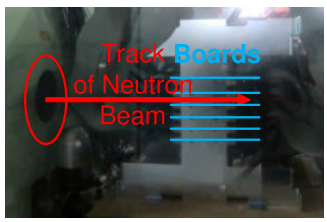

Fig. 3 Experiment setup ©[2018] IEEE. Reprinted, with permission, from [9].

inverter chains. There are 256 inverter chains, and they are target circuits for SET. The cell area of an inverter in the chains is $1.80\mu\text{m} \times 0.52\mu\text{m}$. For obtaining more SET events, more inverters in a chain are preferred since we can allocate more silicon area to the target circuit, i.e. inverters. However, too many inverters may diminish an SET pulse during the propagation in the chain since the chain could gradually reduce the pulse width due to the imbalance between rise and fall delays [10]. As a compromise, we chose the 9-stage inverter chain, strictly speaking, consisting of eight inverters and one NAND gate for this study.

Although the SET rate depends on the logic types, size, etc, characterizing the SET rate for each logic type and size with a statistically meaningful data is not practically possible. Thus, we chose an inverter as the target for SET rate characterization since the inverter is a popular cell in digital circuits and logical masking effect, which prevents an SET from propagating a gate due to the blocking logic values of its side inputs, can be eliminated. Meanwhile all the SETs with a width larger than a certain threshold are captured by FFs in the measurement, which means temporal masking originating from the timing difference between SET and clock is not considered. Due to these, this work measures the raw SET rate that are not affected by logical and temporal maskings.

An SET pulse occurred in a target circuit is given to an asynchronous 1-bit counter, where the 1-bit counter is triplicated and the output is voted for SEU masking. During irradiation experiment, the FF values are scanned out to know how many SETs occurred. Besides, even if the counters and frequency divider are triplicated, errors can accumulate in FFs during the test. For preventing such error accumulation, we periodically reset FFs in the counters and frequency divider.

The test chip includes 60 test groups. Therefore, there are 138,240 target cells in a single test chip. The test chip was fabricated from the same Graphic Data System (GDS) with 65 nm SOTB and bulk technologies with eight metal layers from the same GDS data. A major difference between SOTB and bulk devices is the existence of BOX layer under the channel region.

We mounted 16 test chips on a board as shown in Fig. 2, and six boards, four of which include SOTB chips and two of which include bulk chips, were placed on the neutron beam track as shown in Fig. 3. A pattern generator and logic analyzer were used for generating the input signal and recording the output signal of the chips. In the irradiation test, 48 of 64 SOTB chips and 16 of 32 bulk CMOS chips were measured. The logic analyzer and the PCB boards, each of which gathers the outputs of the chips, are connected with highly-dense contact connectors. The contact patters on the PCB boards were worn out and the secure contact could not be achieved for some connectors despite many trials. Therefore, these chip outputs were not recorded. The supply voltage was set to 0.5 V. The data of the chips were read every 30 minutes.

The neutron beam in Research Center for Nuclear Physics (RCNP) at Osaka University, whose spectrum is similar to that at the terrestrial environment, was irradiated to the test chips. The average flux density of neutrons was $2.46 \times 10^9\,\text{cm}^{-2}\text{h}^{-1}$. Reference [11] reported neutron flux of Tokyo City at sea-level is about $12\ \text{cm}^{-2}\text{h}^{-1}$, and hence the acceleration rate was 2.05×10^8. The test chips were irradiated in 12.9 hours in total with an incident angle of 90 degree.

2.2 Test Result

During the irradiation test, 39 SETs were observed in 16 bulk chips while no SET in 48 SOTB chips. The number of SETs and its SER are listed in Table 1. The location of SET occurrence in the bulk chips was analyzed. The distribution of SET occurrence within test group is shown in Fig. 4, and the distribution within chip is shown in Fig. 5. We can see the SET occurrence is random in space as we expected.

Table 1 Number of measured SETs.

	# of SETs	Irradiation time	# of target cells
SOTB	0	12.9h	6,635,520
Bulk	39	12.9h	2,211,840

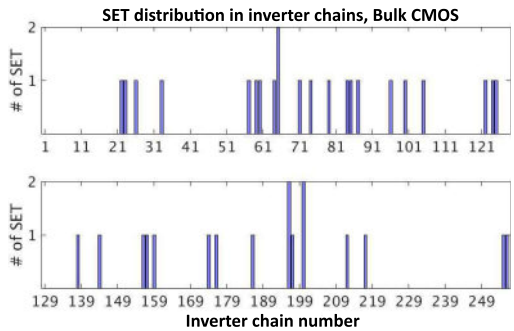

Fig. 4 Distribution of SET occurrence within a test group. Each bar corresponds to an inverter chain.

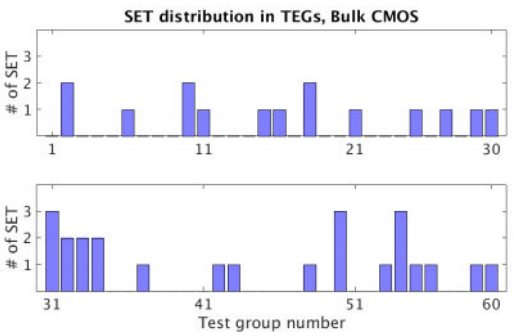

Fig. 5 Distribution of SET occurrence within chip. Each bar corresponds to a test group ©[2018] IEEE. Reprinted, with permission, from [9].

From the result, we could observe that bulk suffers more SETs although it has 2 x less target cells than those in SOTB devices. This indicates that SOTB devices have a stronger immunity to neutron radiation compared to bulk devices. The reason could be attributed to the less charge collection since the insulator layer of the SOTB device prevents the charge deposited in the substrate and well from being collected to the drain.

2.3 Credibility of SET Data

In this irradiation test, the number of SETs was small. For making sure the measured SETs are true SETs instead of pseudo SETs that are caused by SEUs in 1-bit counters, we estimated prospective count of the pseudo SETs. The 1-bit counter consists of 3 FFs and a voter. A pseudo SET occurs when two FFs have upset during the reset interval, and hence the probability of pseudo SET occurrence during reset interval T_{reset}, P_{pSET}, is expressed as

$$P_{pSET} = 3 \cdot P_{FF}^2 \cdot (1 - P_{FF}) + 1 \cdot P_{FF}^3, \quad (1)$$

where P_{FF} is the probability of SEU occurrence during

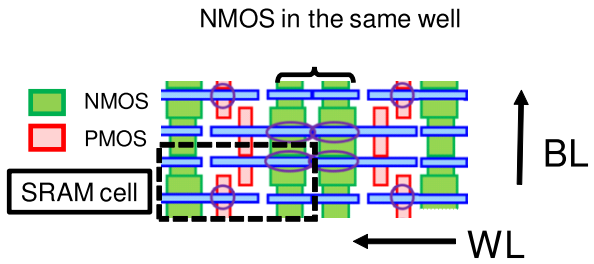

Fig. 6 Layout of SRAM cells ©[2018] IEEE. Reprinted, with permission, from [9].

T_{reset}, and it is expressed as the product of T_{reset} and SER_{FF}, SER of a FF.

Considering the total irradiation time T_{total} and the number of counters in the measured chips $N_{counter}$, the expected number of the pseudo SETs E_{pSET} is calculated as

$$E_{pSET} = P_{pSET} \times N_{counter} \times \frac{T_{total}}{T_{reset}}. \quad (2)$$

In our irradiation experiment, N_{count} was 24,576, and T_{reset} was 3 hours. Using the SER_{FF}, which will be explained in the next section, the expected number of pseudo SET was 2.1. The pseudo SETs were expected to be 5% of the measured SETs. Therefore, we conclude that the measured SETs can be treated as true SETs in the following analysis.

3. MBU Rate Calculation with/without ECC and Interleaving

The SRAM SERs were measured in our previous work [7]. In the measurement, soft errors in SRAMs were classified into SBUs and MCUs. Different from MCUs being counted as long as the upset cells are adjacent, MBU means multiple bits upset inside a single word originating from a single event. This feature makes MBU difficult to be corrected by ECC, especially in high-speed cache in which powerful ECCs cannot be adopted due to its delay overhead [12]. In this section, we calculated the MBU rate for the chip-level SER evaluation. In addition, MBU rates were compared without or with ECC having 1/2/4-col MUX interleaving. By analysis of MBU rates, the reduction due to ECC with interleaving is quantified to show the benefit

3.1 MCU Pattern

Figure 6 illustrates the layout of SRAM cells in the measured chips. The bit lines (BLs) and word lines (WL) are shown in this figure. The cells in the same word are placed along the WL. The number of upsets along the same WL in a single MCU event are the primary index to be observed. Referring to the MCU pattern classification in [13] and counting the upset numbers along the same WL, we define the MCU pattern as,

$$C\_N_1\_N_2\_N_3, \quad (3)$$

where C is category consisting of b/w/c. Here, categories b,

Table 2 MCU pattern classification. Percentage of each pattern is calculated to the total # of MCU events.

		B (%)	W (%)			C (%)					Total MCUs #
		B_x_1_1	W_1_2_2	W_1_3_3	W_1_4_4	C_x_x_1	C_x_x_2	C_x_x_3	C_x_x_4	C_x_x_5	
Bulk	0.4 V	16.01	10.40	0.02	6.92×10^{-3}	6.15	66.91	0.34	0.15	6.92×10^{-3}	14457
	1.0 V	15.65	3.61	–	–	2.04	78.60	0.08	8.34×10^{-3}	–	11986
SOTB	0.4 V	57.69	15.38	3.85	–	11.54	11.38	–	–	–	26
	1.0 V	25.00	25.00	–	–	25.00	25.00	–	–	–	4

w and c stand for a single line along BL, a single line along WL and cluster, where cluster represents an MCU that has two or more bits along with both BL and WL directions. N_1 is the width in the BL direction, N_2 is the width in the WL direction and N_3 is the maximum upset number along the same WL in a single MCU event. With this definition, we categorized the MCUs. Table 2 shows the result. We can see that the type of cluster MCU is the majority in bulk SRAMs and it occupies at least 70%. Comparing bit-line and word-line MCUs, the bit-line ones are slightly more than word-line ones at 0.4 V but the bit-line ones largely exceed the word-line ones at 1.0 V. For SOTB, the trends of MCUs in BL and WL are opposite, and the bit-line MCUs are dominant at 0.4 V. Based on this table, we consider the word organization for ECC and interleaving to calculate the rate of MBU in the corresponding situations.

3.2 MBU Rate with/without ECC and Interleaving

In this subsection, we calculate the MBU rate with and without application of ECC and interleaving. For ECC application, we consider the most popular code of single bit correction double error detection (SECDED). SECDED means a 1-bit error along the WL is assumed to be mitigated whatever the number of upsets in at the BL. This also means SBUs will be mitigated together as well as MCUs only in BLs. For interleaving, 1-col (no interleaving), 2-col (2-bit interval) and 4-col (4-bit interval) MUX are considered. By applying interleaving w/ ECC, even if a successive 2-bit upset along the WL, they are assumed to be corrected separately due to being in the different words.

Taking into account the error correction, an MBU occurs for those $N_3 > 1$ if only ECC is applied, $N_3 > 2$ if ECC and 2-col MUX interleaving are applied, and $N_3 > 4$ if ECC and 4-col MUX interleaving are applied. Then, the MBU rate are calculated using the corresponding percentage of MCU patterns leading to MBU under the assumed combination of ECC and interleaving. The MBU rate is listed in Table 3. From this table, we observe that with ECC and interleaving the MBU rate decreases as we expected compared to that without ECC. Another observation is that sole application of ECC is effective (2 x decrease) but a combination of ECC and small 2-col MUX interleaving achieves around 200 x and 1,000 x reduction in bulk device at 0.4 V and 1.0 V, respectively.

Here, we cannot show the overhead of the 2/4-col MUX interleaving quantitatively since the SRAM array itself was not designed by ourselves. References [12], [19], [20], on the other hand, report an increase in power consumption with the increase in interval distance. This is mainly due to 'half selected' transistors of different words in the same word line [19]. Reference [12] shows an increase in access power of around 30% and 110% from 1-col to 2-col and 4-col MUX interleaving, respectively, for a 4-MB 8-bank cache. Meanwhile, larger MUX interleaving also costs extra area and delay due to larger MUX, but their concrete numbers were not found as far as we investigated. Taking into account the overheads of the larger interleaving to system, we refer the rate under the circumstance of 2-col MUX with ECC in the following chip-level SER estimation.

Table 3 MBU rate in SRAM chips [FIT/Mbit].

	Bulk		SOTB	
	0.4 V	1.0 V	0.4 V	1.0 V
w/o ECC 1-col	737.33	611.30	0.62	0.09
w/ ECC 1-col	573.92	503.13	0.19	0.05
w/ ECC 2-col	3.88	0.56	0.02	–
w/ ECC 4-col	0.05	–	–	–

4. Discussion on Chip-Level SER

4.1 Data Preparation

This section prepares the necessary SER data for estimating chip-level SER. The FF SER in the same SOTB and bulk technologies was measured by Kobayashi et al., and the data in [6] is used. The data used in the chip-level SER estimation is listed in Tables 4 and 5.

In this work, we estimate chip-level SER at 0.5 V and 1.0 V, and some data is missing. References [14]–[17] utilize an exponential function for regression analysis of SER dependency on supply voltage. Referring to these works, we carried out curve fitting to obtain missing data assuming $SER = a\cdot\exp(b\cdot V)$, where a and b are fitting parameters and V is the supply voltage. We confirm that the R-square values of the fitted regression lines for each data set are higher than 0.945, where a value closer to 1 indicates a better fit of the model to the data set. Using the obtained functions, we derived the data at 0.5 V. Such derived data is listed with parenthesis in Tables 4 and 5. As for SOTB SET rate, we calculated it supposing that an error was observed in the irradiation experiment. Unfortunately, we have the SET SER at 0.5 V only, and hence we cannot use curve fitting. We

Table 4 SER data for SOTB circuits.

Voltage [V]	0.4	0.5	0.6	0.8	1.0	1.2
SET [FIT/Mbit]		(0.06)			(0.06)	
SBU [FIT/Mbit]	375	(314)			128	
MBU [FIT/Mbit]	0.6	(0.45)			0.1	
FF [FIT/Mbit]	29.5	(26.8)	26.2	16.2	(14.0)	11.0

Table 5 SER data for bulk circuits.

Voltage [V]	0.4	0.5	0.6	0.8	1.0	1.2
SET [FIT/Mbit]		7.02			(7.02)	
SBU [FIT/Mbit]	1817	(1464)			498	
MBU [FIT/Mbit]	737	(715)			611	
FF [FIT/Mbit]		(1400)	1150	650	620	360

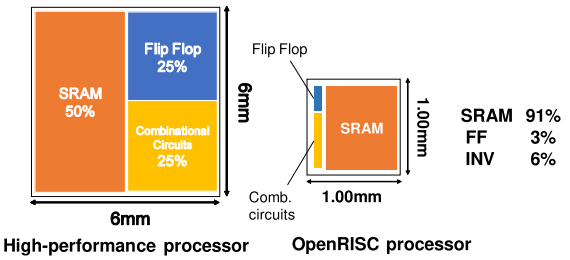

Fig. 7 Structure of high-performance and OpenRISC processor ©[2018] IEEE. Reprinted, with permission, from [9].

thus assumed the SET rates at 0.5 V and 1.0 V were the same. Measuring the SET voltage dependence is one of our future works.

In addition, for chip-level SER estimation, the cell numbers of an assumed high-performance processor and a representative embedded processor, OpenRISC 1200, were considered as the evaluation target in this paper. Figure 7 shows the structure of high-performance processor with large amount of cache memory, larger register files and deeper pipelines, where 50% core area is occupied by SRAM, 25% is occupied by FF and the remaining 25% is occupied by combinational circuit. The core area is 36 mm^2. In our calculation, the sizes of 6T SRAM and FF cell were 0.56μm $\times$ 2.00μm and 1.80μm $\times$ 7.80μm, respectively, and they are consistent with and [7] and [6]. The combination circuit was assumed to be filled of inverters, where the area of an inverter is 1.80μm $\times$ 0.52μm and it is the same as our experiment. The capacity of SRAM is 11.79 Mbit, and the numbers of FFs and inverters are 0.61 M and 5.02 M, respectively. As for OpenRISC 1200, the SRAM size for cache is 0.56 Mbit. To estimate the number of cells, we synthesized the RTL files with a standard cell library. The number of FFs is 24 k and the number combinational cells is 1.10 M. The chip size and area portions of OpenRISC 1200 are also shown in Fig. 7.

Chip-level SER SER_{chip} is calculated as

$$SER_{chip} = (SER_{SBU} + SER_{MBU}) \times N_{SRAM} + SER_{SEU} \times N_{FF} + SER_{SET} \times N_{INV}, \quad (4)$$

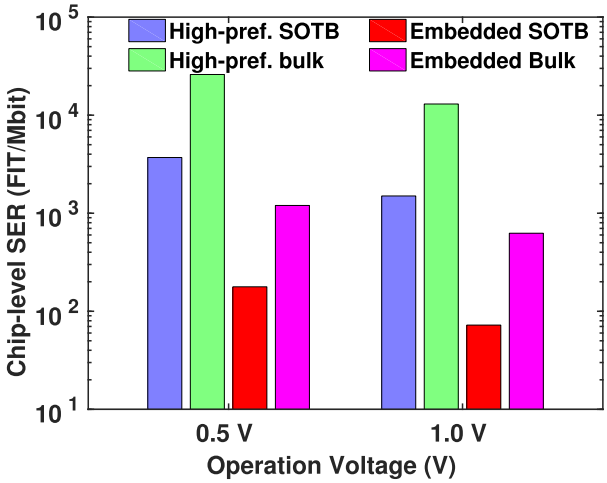

Fig. 8 Chip-level SER without ECC [FIT/Chip].

Table 6 Contributions of SRAM, FF and combinational circuit to chip-level SER without ECC.

		SRAM		Comb.	FF
		MBU	SBU	SET	SEU
high-perf. processor	SOTB@0.5V	0.14%	99.40%	0.02%	0.44%
	SOTB@1.0V	0.51%	98.97%	<0.04%	0.49%
	Bulk@0.5V	31.71%	64.96%	0.12%	3.21%
	Bulk@1.0V	53.82%	43.81%	< 0.24%	2.13%
embedded processor	SOTB@0.5V	0.14%	99.82%	0.00%	0.04%
	SOTB@1.0V	0.07%	99.87%	< 0.01%	0.05%
	Bulk@0.5V	32.70%	67.01%	0.02%	0.27%
	Bulk@1.0V	55.01%	44.78%	< 0.03%	0.18%

where N_{SRAM} is the number of SRAM bits in a chip, and N_{FF} and N_{INV} are the number of FFs and inverters in a chip. To estimate the maximum contribution of SET to chip-level SER, logical, temporal and electrical masking are not considered in this calculation

4.2 Estimation Result and Discussion

The calculated chip-level SER without ECC is shown in Fig. 8. The overall SERs of SOTB chip are 6.0 x and 7.7 x lower than those of bulk chip at 0.5 V and 1.0 V, respectively. Table 6 and Fig. 9 also show a common tendency for both processors that soft error in SRAM dominates in the total chip-level SER. In SOTB chip, more than 99% errors occur in SRAM, and other FF SEU and SET are negligible. Similarly, more than 95% errors occur in SRAM in bulk chip.

Next, we apply ECC to SRAM. In this case, the MBU rates with ECC and 2-col interleaving calculated in the previous section are used. The chip-level SER with ECC is shown in Fig. 10. In high-performance processor of SOTB, the chip-level SER is reduced by two orders magnitude while it is reduced by one order of magnitude in bulk chip. This is because the MBU rate is much lower than the SBU rate in SOTB chip. Consequently, the SERs of SOTB chip

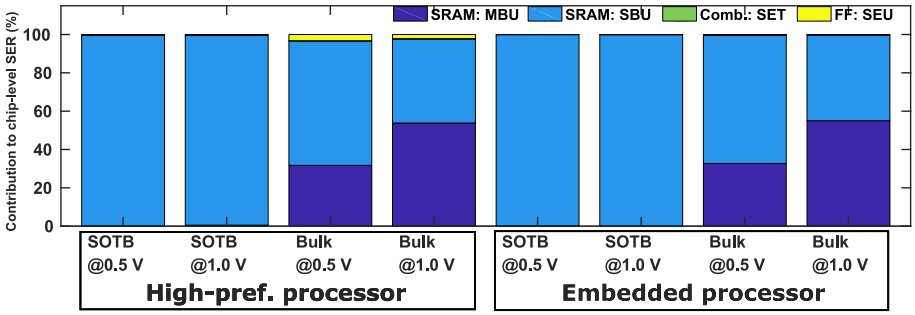

Fig. 9 Contributions of SRAM, FF and combinational circuit to chip-level SER without ECC. This figure is essentially equivalent with Table 6.

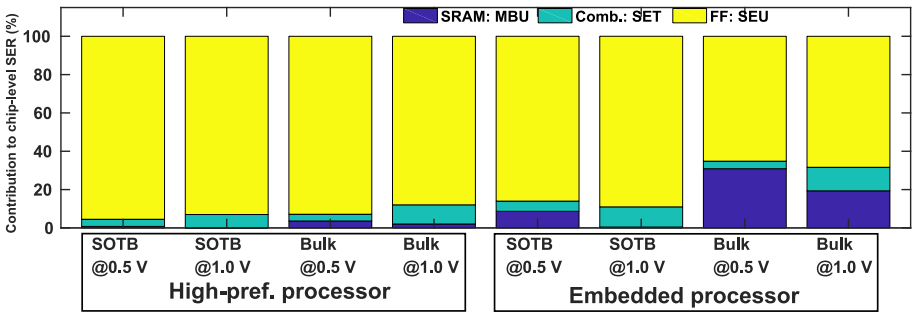

Fig. 11 Contributions of SRAM, FF and combinational circuit to chip-level SER with ECC and 2-col interleaving. This figure is essentially equivalent with Table 7.

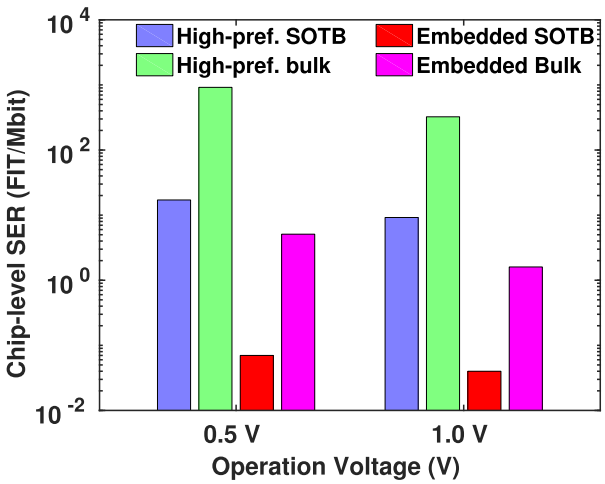

Fig. 10 Chip-level SER with ECC and 2-col interleaving [FIT/Chip]. Note that the range of Y-axis is different from that of Fig. 8.

are 53 x and 34 x lower than those of bulk chip at 0.5 V and 1.0 V, respectively. ECC provides more powerful mitigation to embedded processors.

Table 7 and Fig. 11 show the decomposition of chip-level SER. With ECC, the proportion of FF becomes dominant in all the embedded and high-performance processors of SOTB and bulk while MBU in SRAMs still take around 20% in bulk embedded processors. In high-performance processor of SOTB, the contribution of FF reaches 95% at 0.5 V while that in embedded processors also contributes to

Table 7 Contributions of SRAM, FF and combinational circuit to chip-level SER with ECC and 2-col interleaving.

		SRAM		Comb.	FF
		MBU	SBU	SET	SEU
high-perf. processor	SOTB@0.5V	0.77%	–	3.74%	95.48%
	SOTB@1.0V	0.04%	–	< 6.95%	93.01%
	Bulk@0.5V	3.60%	–	3.53%	92.86%
	Bulk@1.0V	2.04%	–	< 10.00%	87.96%
embedded processor	SOTB@0.5V	8.65%	–	5.33%	86.02%
	SOTB@1.0V	0.45%	–	<10.53%	89.03%
	Bulk@0.5V	30.90%	–	3.92%	65.17%
	Bulk@1.0V	19.35%	–	< 12.29%	68.35%

60% at least. On the other hand, the SET contribution ranges from 4.55% to 16.67%. Considering that temporal and logical masking are ignored for upper bound estimation, we can conclude that SET cannot be a primary concern for both the high-performance and embedded processors. This result is consistent with the simulation based result showing a maximum ratio of 2% in [21].

5. Conclusion

In this paper, the chip-level neutron-induced SER of SOTB and bulk circuits at 0.5 V and 1.0 V and the contributions of SRAM, FF and combinational circuit to the chip-level SER were investigated. Combining the measured SET rate with previously reported SERs, chip-level SER of processors made of SOTB and bulk CMOS were calculated. With-

out ECC, at least 95% errors occur in SRAM in both SOTB and bulk chips and in both embedded and high-performance processors. With ECC, MBU rate is reduced and then chip-level SER of SOTB devices decreasesd 162 x at least, while the reduction for bulk devices was 25 x. The contribution of FF in SOTB high-performance processor became 95% at 1.0 V, whereas the contribution of FF also reached 65%. Therefore, radiation-hard FF SEU is helpful to further reduce chip-level SER.

Acknowledgements

This work was partially done in "Ultra-Low Voltage Device Project" of LEAP funded and supported by METI and NEDO. This work is supported by JST OPERA program.

References

[1] H.-K. Lim and J.G. Fossum, "Threshold voltage of thin-film Silicon-on-Insulator (SOI) MOSFET's," IEEE Trans. Electron Devices, vol.30, no.10, pp.1244–1251, 1983.
[2] N. Seifert, P. Slankard, M. Kirsch, B. Narasimham, V. Zia, C. Brookreson, A. Vo, S. Mitra, B. Gill, and J. Maiz, "Radiation-induced soft error rates of advanced CMOS bulk devices," Proc. Int. Reliab. Phys. Symp., pp.217–225, 2006.
[3] P. Roche, G. Gasiot, K. Forbes, V. O'Sullivan, and V. Ferlet, "Comparisons of soft error rate for SRAMs in commercial SOI and bulk below the 130-nm technology node," IEEE Trans. Nucl. Sci., vol.50, no.6, pp.2046–2054, 2003.
[4] J.R. Schwank, V. Ferlet-Cavrois, M.R. Shaneyfelt, P. Paillet, and P.E. Dodd, "Radiation effects in SOI technologies," IEEE Trans. Nucl. Sci., vol.50, no.3, pp.522–538, 2003.
[5] Y. Yamamoto, H. Makiyama, H. Shinohara, T. Iwamatsu, H. Oda, S. Kamohara, N. Sugii, Y. Yamaguchi, T. Mizutani, and T. Hiramoto, "Ultralow-voltage operation of Silicon-on-Thin-BOX (SOTB) 2Mbit SRAM down to 0.37 V utilizing adaptive back bias," Proc. Symposium on VLSI Circuits, pp.T212–T213, 2013.
[6] J. Yamaguchi, J. Furuta and K. Kobayashi, "A radiation-hardened non-redundant flip-flop, stacked leveling critical charge flip-flop in a 65 nm thin BOX FD-SOI process," Proc. European Conference on Radiation and Its Effects on Components and Systems (RADECS), pp.1–4, 2015.
[7] S. Hirokawa, R. Harada, K. Sakuta, Y. Watanabe, and M. Hashimoto, "Multiple sensitive volume based soft error rate estimation with machine learning," Proc. European Conference on Radiation and Its Effects on Components and Systems (RADECS), pp.1–4, 2016.
[8] J. Furuta, E. Sonezaki, and K. Kobayashi, "Radiation hardness evaluations of 65 nm fully depleted silicon on insulator and bulk processes by measuring single event transient pulse widths and single event upset rates," Japanese Journal of Applied Physics, vol.54, no.4S, pp.04DC15–1–6, March 2015.
[9] W. Liao, S. Hirokawa, R. Harada, and M. Hashimoto, "Contributions of SRAM, FF and combinational circuit to chip-level neutron-induced soft error Rate — Bulk vs. FD-SOI at 0.5 and 1.0V," Proc. International NEWCAS Conference, pp.33–37, 2017.
[10] V. Ferlet-Cavrois, L.W. Massengill, and P. Gouker, "Single event transients in digital CMOS — A review," IEEE Trans. Nucl. Sci., vol.60, no.3, pp.1767–1790, 2013.
[11] J.F. Ziegler, "Terrestrial cosmic rays," IBM Journal of Research and Development, vol.40, no.1, pp.19–39, Jan. 1996.
[12] J. Kim, N. Hardavellas, K. Mai, B. Falsafi, and J. Hoe, "Multi-bit error tolerant caches using two-dimensional error coding," Proc. Annu. Int. Symp. Microarchitecture, MICRO, pp.197–209, 2007.
[13] E. Ibe, H. Taniguchi, Y. Yahagi, K.-I. Shimbo, and T. Toba, "Impact of scaling on neutron-induced soft error in SRAMs from a 250 nm to a 22 nm design rule," IEEE Trans. Electron Devices, vol.57, no.7, pp.1527–1538, 2010.
[14] A. Dixit and A. Wood, "The impact of new technology on soft error rates," Proc. Int. Reliab. Phys. Symp., pp.5B.4.1–5B.4.7, 2011.
[15] H. Fuketa, R. Harada, M. Hashimoto, and T. Onoye, "Measurement and analysis of alpha-particle-induced soft errors and multiple-cell upsets in 10T subthreshold SRAM," IEEE Trans. Device Mater. Rel., vol.14, no.1, pp.463–470, 2014.
[16] B. Narasimham, S. Gupta, D. Reed, J.K. Wang, N. Hendrickson, and H. Taufique, "Scaling trends and bias dependence of the soft error rate of 16 nm and 7 nm FinFET SRAMs," Proc. Int. Reliab. Phys. Symp., pp.4C.11–4C.14, 2018.
[17] B. Narasimham, S. Hatami, A. Anvar, D.M. Harris, A. Lin, J.K. Wang, I. Chatterjee, K. Ni, B.L. Bhuva, R.D. Schrimpf, R.A. Reed, and M.W. McCurdy, "Bias dependence of single-event upsets in 16 nm FinFET D-flip-flops," IEEE Trans. Nucl. Sci., vol.62, no.6, pp.2578–2584, Dec. 2015.
[18] P. Hazucha and C. Svensson, "Impact of CMOS technology scaling on the atmospheric neutron soft error rate," IEEE Trans. Nucl. Sci., vol.47, no.6, pp.2586–2594, Dec. 2000.
[19] S. Kim and M.R. Guthaus, "Low-power multiple-bit upset tolerant memory optimization," Proc. 2011 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp.577–581, 2011.
[20] S. Baeg, S. Wen, and R. Wong, "SRAM interleaving distance selection with a soft error failure model," IEEE Trans. Nucl. Sci., vol.56, no.4, pp.2111–2118, 2009.
[21] B. Gill, N. Seifert, and V. Zia, "Comparison of alpha-particle and neutron-induced combinational and sequential logic error rates at the 32nm technology node," Proc. Int. Reliab. Phys. Symp., pp.199–205, 2009.

Wang Liao received the B.S. in Shenyang University of Technology in 2013 and M.S. degrees in Northeastern University in 2015, respectively. He is now a currently Ph.D. candidate in Osaka University, Department of Information Systems Engineering. His research interest is radiation effect in electronics.

Masanori Hashimoto received the B.E., M.E. and Ph.D. degrees in Communications and Computer Engineering from Kyoto University, Kyoto, Japan, in 1997, 1999, and 2001, respectively. Since 2016, he has been a Professor in Department of Information Systems Engineering, Graduate School of Information Science and Technology, Osaka University. His research interest includes computer-aided design for digital integrated circuits, and high speed circuit design. Dr. Hashimoto served on the technical program committees for international conferences including DAC, ICCAD, ITC, Symposium on VLSI Circuits, ASP-DAC, DATE, ISPD and ICCD. He is a member of IEEE, ACM, and IPSJ.