Characterizing soft error rates of 65-nm SOTB and bulk SRAMs with muon and neutron beams

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***Abstract*—This paper comparatively discusses soft error immunity of silicon on thin BOX (SOTB) SRAM and conventional bulk SRAM presenting neutron- and muon-induced soft error rates (SER) in 65-nm 6T SRAM over a wide range of supply voltages. The results show that the neutron-induced multiple cell upset (MCU) rates of SOTB at 0.4 V and 1.0 V are 0.01 times and 0.003 times lower than those of bulk at 0.4 V and 1.0 V, respectively. In advanced bulk low-voltage SRAM, protons can be dominant secondary particles, which brings drastic SER elevation, but this will not arise in SOTB SRAM due to its thin SOI layer. We also characterized the immunity to positive and negative muons. We observed negative muon induced more upsets due to muon capture process. We also confirmed that SOTB SRAM was more robust to muon than bulk SRAM.**

I. Introduction

Soft error occurring inside VLSIs in the terrestrial environment has been recognized as a major threat for electronics at ground level [1]. Radiation-induced soft error is represented as a transient malfunction in VLSIs due to single event upsets (SEUs), which are caused by energetic ionizing radiation and destroy the information stored in memory elements.

Fully depleted silicon on insulator (FD-SOI) is suitable for lower-voltage operation compared to conventional bulk devices. Silicon on thin buried oxide (SOTB) device, which is an FD-SOI device, has better threshold voltage controllability with body biasing by thinning the insulator layer (buried oxide; BOX) under the channel region [2].

This paper discusses the SRAM SER, which is the most sensitive component in VLSIs. The presented results cover conventional bulk transistor, which continues to be used for cost-effective IoT applications, and SOTB transistor. Furthermore, muon-induced soft error is also discussed as a future reliability concern.

II. MCU mechanism and its countermeasure

Multiple cell upsets (MCUs) induced by a single neutron are becoming a serious concern. MCUs can be mostly mitigated by interleaving and ECC (error correction code). On the other hand, as the number of upsets for an event becomes larger, MCU patterns which cannot be eliminated by interleaving and ECC are more likely to arise. There are four possible mechanisms of MCU; (1) successive hits of an ion, (2) multi hits by multiple ions, (3) charge drift/diffusion (charge sharing), and (4) parasitic bipolar action.

In bulk SRAM, (3) charge sharing and (4) parasitic bipolar action are major mechanisms. Charge sharing causes MCU due to charge diffusion to multiple cells. Parasitic bipolar action triggered by changing well potential flips multiple cells in a well.

In SOTB SRAM, on the other hand, MCUs due to (3) charge sharing and (4) parasitic bipolar action do not occur since SOTB transistors do not share a well. Therefore, the remaining (1) successive hits of an ion and (2) multi hits by multiple ions cause MCUs in SOTB SRAM. Consequently, the MCU rate is expected to be lower and large-bit MCUs are less probable to occur in SOTB SRAM.

III. Neutron-induced soft error

Two SRAM test chips of SOTB and bulk devices were fabricated in a 65-nm CMOS technology from the same Graphic Data System (GDS) data. Both the test chips include 24 SRAM macros, and each SRAM macro consists of nine memory arrays of 512WL×64BL=32k bits, which includes traditional 6T SRAM cells, read/write circuitry, control unit, and data/address shift registers. Then, each chip contains 6,912 kbits. In both SOTB and bulk SRAMs, the SRAM area is covered by a deep N-well.

Neutron irradiation test was carried out at RCNP of Osaka University. Four SOTB SRAM boards and two bulk SRAM boards, on each of them 16 chips are mounted, were irradiated, where the boards were aligned to be perpendicular (0 °) to or in parallel (90 °) to the beam track.

Fig. 1 shows the measurement results of the accelerated neutron test with voltage scaling. The number of measured SEUs on the SOTB SRAM at 0.4 V supply voltage was 4.4 times larger than that at 1.0 V supply voltage, while the number of SEUs on the SOTB SRAM at 0.4 V was 0.08 times smaller than that on the bulk SRAM at 0.4 V supply voltage. The number of SEUs on the SOTB SRAM at 0.4 V operation was roughly equivalent to that on the bulk device at 1.0 V. On the other hand, the numbers of measured MCUs on the SOTB SRAM was 0.01X and 0.003X smaller than those on the bulk SRAM at 0.4V and 1.0V, respectively. Therefore, roughly speaking, SOTB SRAM is expected to achieve two to three orders of magnitude lower SER when ECC and interleaving are applied.

Fig. 2 shows the MCU rates for each number of simultaneous bit flips in the SOTB and bulk SRAMs at the incident angle of 0°. As the number of bit flips increases, the number of measured MCUs quickly decreases in the SOTB SRAM, while it slowly decreases in the bulk SRAM. Even the MCU rate of

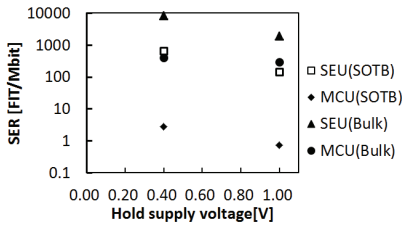

Fig. 1: Measured neutron-induced SEU and MCU rates (0°) [3].

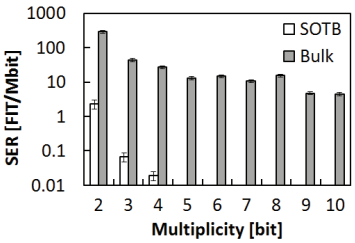

Fig. 2: Measured neutron-induced MCU rate (0.4V, 0°) [3].

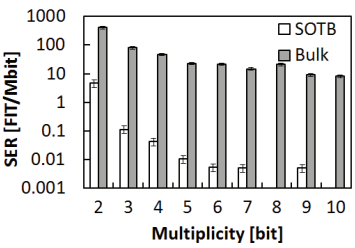

Fig. 3: Measured neutron-induced MCU rate (0.4V, 90°) [3].

simultaneous 10-bit flips in the bulk SRAM is higher than the MCU rate of 2-bit flips in the SOTB SRAM. Regarding MCU, SOTB is superior to bulk since MOS transistors do not share a well in SOTB and charge sharing and parasitic bipolar action do not occur, as discussed in Section II.

Fig. 3 shows the result at the incident angle of 90°. In this case, 9-bit MCU occurred even in the SOTB SRAM, while its rate was more than three orders of magnitude lower than that of the bulk SRAM. This result is explained by the fact that secondary ions contributing to MCU tend to be emitted forward and pass through multiple memory cells along the neutron beam. When the incident angle is 90°, the secondary ions emitted forward by nuclear reaction travel parallel to the chip surface, and more likely pass through multiple sensitive volumes for upsets. Hence, larger MCUs were observed at the incident angle of 90°. This angular dependency of MCU in bulk ultra-low-voltage SRAM is reported in [4].

IV. Muon-induced soft error

Recent literature (e.g., [5]) points out that muons are a potential source of soft error in the terrestrial environment. Muons are the majority particle on the ground, and hence muon-induced soft error is drawing attention in the research community of single event effects. On the one hand, available muon beamlines for irradiation experiments are limited, and hence, while several accelerator-based irradiation experiments for muon induced single event upset (SEU) are reported, no negative muon irradiation tests for sub-micrometer devices have been reported.

In this paper, we report tests of 65-nm bulk and SOTB SRAMs with operation voltage scanning [6], [7]. Fig. 4 shows the dependency of single bit upset (SBU) and MCU cross sections on operation voltage under the irradiation of positive and negative muons in the bulk SRAM. The cross sections under negative muon irradiation are larger than those under positive muon irradiation due to muon capture process, which is unique to negative muon. Under positive muon irradiation, the cross sections increase monotonically as the supply voltage lowers, which can be explained by the decrease in critical charge. We observed only two MCU events at 0.4 V and no MCU events at 0.5 V and above under positive muon irradiation. As for negative muon irradiation, SBU also increases as the operating voltage decreases. MCU, on the other hand, rises above 0.5 V. At the low voltage of 0.5 V, the ratio of larger-bit MCU event is smaller. Meanwhile, at the high voltage 1.2

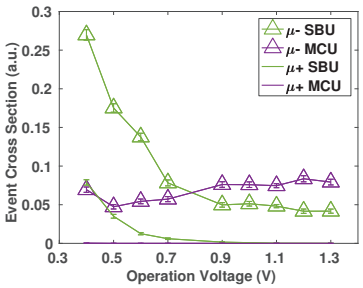

Fig. 4: SBU and MCU event cross sections. The momentum of negative and positive muons is 38 MeV/c.

V, large-bit MCUs, such as over 20-bit MCUs are observed. These results indicate that negative muon-induced MCUs are caused by PBA similar to neutron-induced ones.

We also characterized the cross sections of the SOTB SRAM [7]. Comparing these measurement results, we found that the MCU cross section of SOTB SRAM is about 50 times smaller than that of bulk SRAM at 1.1 V. Similar to neutrons, SOTB SRAM is more immune to muons than bulk SRAM.

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References

[1] E. Ibe, "Terrestrial Radiation Effects in ULSI Devices and Electronic Systems," *Wiley-IEEE Press*, 2015.
[2] Y. Morita, et al., "Smallest Vth variability achieved by intrinsic silicon on thin box (SOTB) CMOS with single metal gate," *Symp. VLSI Technology*, 2008.
[3] S. Hirokawa, et al., "Characterizing Alpha- and Neutron-Induced SEU and MCU on SOTB and Bulk 0.4-V SRAMs," *IEEE Trans. Nucl. Sci.*, Vol. 62, No. 2, Apr. 2015.
[4] R. Harada, et al., "Angular Dependency of Neutron Induced Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM," *IEEE Trans. Nucl. Sci.*, Vol. 59, No. 6, Dec. 2012.
[5] B. D. Sierawski et al., Muon-Induced Single Event Upsets in Deep-Submicron Technology, *IEEE Trans. Nucl. Sci.*, Vol. 57, No. 6, Dec. 2010.
[6] W. Liao et al., "Measurement and Mechanism Investigation of Negative and Positive Muon-Induced Upsets in 65nm Bulk SRAMs," *IEEE Trans. Nucl. Sci.*, Vol. 65, No. 8, Aug. 2018.
[7] S. Manabe et al., "Negative and Positive Muon-Induced Single Event Upsets in 65-nm UTBB SOI SRAMs," *IEEE Trans. Nucl. Sci.*, Vol. 65, No. 8, Aug. 2018.