Multiple Sensitive Volume Based Soft Error Rate Estimation with Machine Learning

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***Abstract*—We propose a new methodology for soft error rate estimation using multiple sensitive volumes and machine learning. The proposed methodology assigns multiple sensitive volumes to a unit circuit (e.g. SRAM cell) and constructs a discriminator from TCAD simulations by machine learning. For each ion reproduced by radiation transport simulation, the discriminator judges whether an upset occurs or not, and consequently we can obtain soft error rate by counting the number of events judged as upset events. Advantages of the proposed methodology are: (1) empirical construction and adjustment of sensitive volume and critical charge is no longer necessary, (2) multiple transistors can be easily considered, and (3) event-wise accuracy can be improved. We confirmed the correlation between irradiation results and simulation results for 65-nm silicon on thin buried oxide (SOTB) SRAM. The estimation error was 7% without any empirical optimization of sensitive volume and critical charge.**

I. Introduction

Due to miniaturization and highly integrated VLSI, radiation effect become one of serious problem on microelectronics devices. Especially in terrestrial environments, neutron-induced soft errors become one of primary reliability issues.

To estimate the impact of neutron-induced soft error, various soft error rates (SERs) estimation methods using Monte Carlo radiation transport simulation have been proposed (see [1]). To simplify the simulation model and save CPU time, most of them introduce sensitive volume method [2]. Basically, this method considers that the charge deposited in the sensitive volume by a secondary ion is collected to drain node. According to the amount of the collected charge, this method classifies whether an SEU occurs or not.

To consider the spatial variation of charge collection efficiency, K. M. Warren et al. introduced multiple sensitive volume method [3]. The total collected charge is calculated as the weighted sum of the charge deposited in each sensitive volume, where each weight represents the charge collection efficiency of its corresponding sensitive volume. Furthermore, the contribution of charge deposition to on-transistor is pointed out recently, and sensitive volume is assigned to on-transistor in addition to off-transistor in [4]. A problem of the conventional multiple sensitive volume method is that careful assignment of multiple sensitive volumes and characterization of the weight are necessary before the Monte Carlo radiation transport simulation, and sometimes those require empirical optimization. In addition, those assignment and characterization depend on the supply voltage and body voltage, and hence the Monte Carlo simulation must be executed for each voltage configuration.

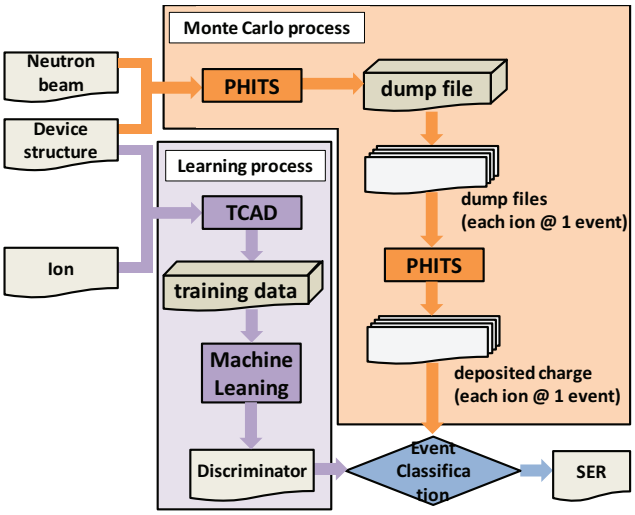

Fig. 1. Proposed SER estimation flow with PHITS and machine learning.

This paper proposes to incorporate machine learning with multiple sensitive volume based Monte Carlo radiation transport simulation. The proposed method constructs a discriminator for upset occurrence classification from TCAD simulations using machine learning. The discriminator is applied to events reproduced in the Monte Carlo radiation transport simulation with multiple sensitive volumes. The proposed machine learning based method decouples the Monte Carlo radiation transport simulation and the event classification, and hence the same radiation transport simulation results can be reused for various discriminators corresponding to, for example, different voltage configurations. In this work, we apply the proposed method to 65-nm FD-SOI SRAM and investigate the correlation between the irradiation result and estimated result.

II. Proposed SER Estimation Method with Machine Learning

Fig. 1 shows the flow of the proposed multiple sensitive volume based SER estimation. We can assign multiple sensitive volumes within a single transistor, and such an assignment can be applied to multiple transistors within a unit circuit (e.g. an SRAM cell). There are Monte Carlo process and learning process. In Monte Carlo process, Monte Carlo radiation transport simulation is performed with the information

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on neutron beam and device structure. Here, PHITS (Particle and Heavy Ion Transport code System) [5] is selected as one of radiation transport simulators, but other radiation transport simulation tools can be also used. PHITS outputs the dump file that contains information on a number of secondary ions. Subsequently, the information on each secondary ion in dump file is given to PHITS, and the amounts of charge deposited in individual sensitive volumes are obtained. The charge information is arranged for each event.

When the multiple sensitive volume method is adopted, it is not easy to judge whether an upset occurs or not. In the conventional single sensitive volume method, such as [3], a single value is calculated from the amounts of charge deposited in individual sensitive volumes, and the calculated value is compared with a given threshold value. In [3], the single value is calculated as the weighted sum of the individual charge amounts so that the single value represents the collected charge. In this case, the weights represent the charge collection efficiency of each sensitive volume. The threshold value and weights are characterized by TCAD and circuit simulation. In this approach, the assignment of multiple sensitive volumes is a critical issue since the charge collection mechanism must be reproduced by the volume assignment. In addition, such an assignment depends on the supply voltage since the charge collection depends on the supply voltage, which means PHITS must be executed for each supply voltage.

Instead, for such a classification purpose, machine learning, more specifically, supervised machine learning is a suitable and powerful method, and several well-known methods are available, for example support vector machine, random forest, and so on. In the learning part, to construct a discriminator for upset classification, we prepare a training set of TCAD simulation data; ions are injected with various directions within a unit circuit and we record whether an upset occurs or not and how much charge is deposited in the individual sensitive volumes. Then, we construct a discriminator that tells us whether an upset occurs or not as a function of the amounts of charge deposited in the individual sensitive volumes. Once the discriminator is available, we can immediately judge whether an upset occurs or not for each event simulated in PHITS. By counting the number of upsets, we can obtain the SER.

An advantage of the proposed method is that the careful assignment of sensitive volumes is not necessary, or rather fine discretization is better since the machine learning works well for a large number of input variables. Therefore, we do not need to change the sensitive volume assignment for different voltage configurations, and the results obtained in the Monte Carlo process can be reused. In addition, the Monte Carlo process and learning process can be started simultaneously and executed in parallel.

III. Measurement

A. Measurement setup

Silicon on insulator (SOI) is one of the solutions for low voltage operation. Especially, fully depleted SOI (FD-SOI), whose channel region is thinner and more depleted than conventional partially depleted SOI (PD-SOI), has been developed to enable lower voltage operation. Moreover, a silicon on thin buried oxide (SOTB) device, which is a FD-SOI device, has better threshold voltage (Vth) controllability with body biasing by thinning the insulator layer (buried oxide; BOX) under the channel region [6]. The thickness of the BOX layer in SOTB devices is 10-nm while other SOI devices often have BOX layers thicker than 100-nm, which makes it possible to maintain the operation speed even at 0.4 V operation with aggressive body biasing.

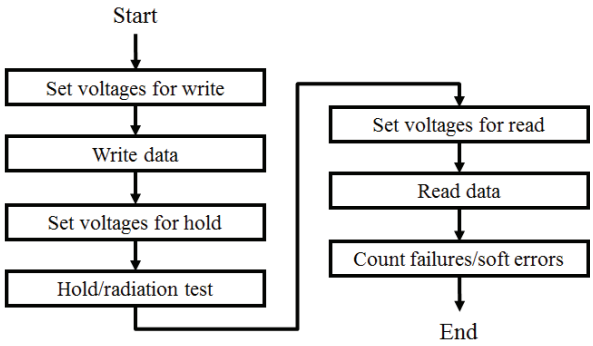

Fig. 2. A flow of hold and accelerated neutron tests.

Our previous work [7] reported that the number of neutron induced SEUs at 0.4 V was 0.08 times smaller than that on the bulk SRAM at 0.4 V and the number of measured multiple cell upsets (MCU) was two orders of magnitude smaller. However, SOTB SRAM reported in [7] was designed according to the logic design rule, and the SRAM cell area was 2.7 times larger than that of SRAM rule based SRAM [6]. As the SRAM cell becomes smaller, the sensitive volume could become smaller, but the distance between the sensitive volumes becomes shorter. These tendencies may increase the impact of on-transistor. In addition, SOTB SRAM has good Vmin [6], which is the minimum operatable supply voltage, but the immunity below 0.4 V was not evaluated.

Two test chips of SOTB and bulk SRAMs were fabricated in a 65 nm process with eight metal layers from the same Graphic Data System (GDS) data. A major difference between SOTB and bulk chips is the existence of BOX layer under the channel region. Both the test chips include 42 SRAM macros, and each SRAM macro consists of a memory array, which includes traditional 6T SRAM cells, read/write circuitry, control unit and data/address shift registers. The SRAM macros were designed according to SRAM design rule [6]. Due to this design rule difference, the total amount of SRAM memories on a test chip increased 1.75X and it is about 12 Mb.

SER during hold operation is evaluated. As supply voltage becomes lower, SRAM cells start failing to hold their values due to V_T unbalance between PMOS and NMOS transistors. This V_T unbalance is induced by within-die process. To distinguish such failure bits from soft errors, hold operation is firstly tested for every SRAM cell. The failure bits are excluded from soft error evaluation. Note that the number of failure bits at 0.3 V in the SOTB SRAM is 27,000X smaller

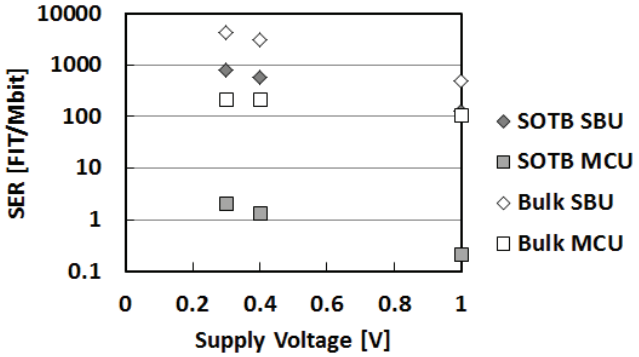

Fig. 3. Measured SBU and MCU rates.

than in the bulk SRAM.

Fig. 2 illustrates the flow of both hold and irradiation tests. The supply and body voltages are first set for write operation. The SRAM memories are initialized by writing a data pattern for test through the data/address shift registers. Then, the supply and body voltages are changed to those for hold operation and the SRAM is turned into hold operation. In case of irradiation test, neutron irradiation is performed during this hold operation. After that, the voltages are set back for read operation, and read the data stored in the SRAM through the shift registers. Finally, the number of failure bits or upsets is counted outside the test chip. This hold test procedure is performed for two situations; zero is stored in the SRAM, and one is stored in the SRAM. Repeating this test flow without irradiation, failure bits for hold operation are identified and then eliminated for the next irradiation test. Note that transitions of supply and body voltages from write operation to hold operation and from hold operation to read operation are performed with a large time interval at sufficiently small voltage steps to avoid overshoot/undershoot causing unexpected failures.

B. Measurement results

Accelerated neutron irradiation test was performed at Research Center for Nuclear Physics (RCNP) in Osaka University using an accelerated spallation neutron beam. The average flux density of irradiated neutron beam was 2.46×10^{9} cm^{-2} h^{-1}. In this test, the six test boards, each of which has 16 test chips, were placed in series on the beam track, so that 64 SOTB test chips (about 792 Mb) and 32 bulk test chips (about 396 Mb) were tested simultaneously. Hold operation was set to 600 s. The neutron beam was given at perpendicular direction to the test boards.

Fig. 3 shows the numbers of SBU and MCU events. Each error bar indicates the standard deviation of the observed events. Note that MCU is defined two or more simultaneous upsets in vertically, horizontally, and/or diagonally adjacent bits in this paper. The number of measured SBUs in the SOTB SRAM at 0.3 V is 1.4 times and 6.2 times larger than those at 0.4 V and 1.0V. The SBU increase from 0.4 V to 0.3V voltage scaling was not drastic. The number of measured MCUs in the SOTB SRAM at 0.3 V was two orders of magnitude smaller than that in the bulk SRAM. Even compared with the bulk SRAM at 1.0V, the number of MCUs was almost two orders of magnitude smaller, which reveals that 0.3V SOTB SRAM with ECC is 100X higher soft error immunity compared to 1.0V bulk SRAM with ECC. These result were almost independent of the board and chip locations. The measurement result of 0.3V SOTB SRAM will be reproduced with the proposed method in the next section.

IV. SER Estimation Results

A. Setup

In the learning process, we prepared the training data using 3D TCAD simulator (Sentaurus of Synopsys). We constructed a 3D model of an SRAM cell consisting of six SOTB transistors. This model had a 10-nm thick SOI layer and 12-nm thick BOX layer. The depth of the STI was 0.4 μm. To reproduce the measurement condition, the supply voltage was set to 0.3 V. The density of charge generation followed a Gaussian distribution with a standard deviation of 30 nm [8]. Ions whose LET was less than 100 MeV/(mg/cm^2) were randomly injected. The ion tracks were also randomly generated whereas the ion tracks that did not go through any sensitive volumes were discarded before performing TCAD simulation. The flight length of the ions was randomly determined, where the minimum flight length was 0.3 μm. For each simulation, we calculated the charge deposited in each sensitive volume and recorded the charge values and whether an upset occurred or not as a sample. In total, we obtained the training data consisting of 1,000 samples. The number of upset samples was 200 and the number of non-upset samples was 800. We chose random forest as a machine learning method since random forest achieved high accuracy for this training data and its accuracy was 97.3%.

Next, Monte Carlo process is explained. Nuclear reactions and the subsequent transport of secondary ions were simulated by PHITS. Fig. 4 illustrates the configuration of the test device used in PHITS simulation. An SRAM memory cell with the size of 0.52 μm $\times$ 1.04 μm was placed in the bottom of a 4.8 mm $\times$ 2.4 mm $\times$ 6 μm silicon substrate as two-dimensional grid. The thickness of the SOI layer and the BOX layer is 12nm and 10nm, respectively. Above the SOI layer, there were a gate oxide layer (SiO2) whose thickness was 4nm, a

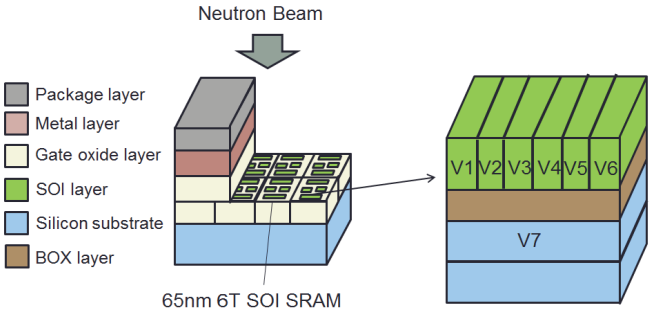

Fig. 4. Multiple sensitive volume assignment to a transistor. Seven volumes of V1 to V7 are assigned.

metal layer (Cu and SiO2) whose thickness was 2.43μm and a package layer whose thickness was 1.00mm.

Fig. 4 also shows the sensitive volume allocation. We set seven sensitive volumes to each transistor: (V1) the left half of source region under the gate, (V2) the right half of that, (V3) the left half of SOI layer under the gate, (V4) the right half of that, (V5) the left half of drain region under the gate, (V6) the right half of that, and (V7) the region under the BOX layer. Such fine volume allocation is motivated by the observation that the minimum LET for upset occurrence is much different even inside a transistor [7].

For every event of nuclear reaction, we gave the amounts of charge deposited in the sensitive volumes in an SRAM cell to the discriminator constructed by random forest and judged whether an SEU occurred or not. Besides, the neutron beam whose energy spectrum was the same with RCNP beam spectrum was irradiated in the direction of the arrow in Fig. 4, similar to the irradiation experiment condition.

For clarifying the advantage of the multiple sensitive volume method, we also estimated SER assigning a single sensitive volume per transistor. Here, the sensitive volume was composed of V3 and V4 in Fig 4. With this setup, the following two configurations were tested as conventional methods.

- Only off-state NMOS was considered. If the charge deposited at the sensitive volume in off-state NMOS exceeded the threshold value, it was considered that an upset occurred. The threshold value was set to 8.9×10^{-3}[fC] from the result of TCAD simulation.
- Off-state NMOS and off-state PMOS were considered. If the charge deposited at the sensitive volume in off-state NMOS and off-state PMOS exceeded the corresponding threshold values respectively, it was considered that an upset occurred. The threshold value for off-state NMOS was set to 8.9×10^{-3}[fC] and the threshold value for off-state PMOS was 1.34×10^{-2}[fC].

B. Simulation results

We evaluate the correlation between the measurement and estimation results. First, 3×10^{9} neutrons were injected to the device in the PHITS simulation. Fig. 5 shows SERs of the experiment, the proposed method and two conventional methods. The figure shows that the order of estimated SERs matches roughly. On the other hand, the estimate of the proposed method is much closer to the experimental result than those of the conventional methods. The estimation error of the proposed method is 7% whereas the errors of "only off-state NMOS" and "off-state NMOS and off-state PMOS" with a single sensitive method are 76% and 65%, respectively. Thus, the multiple sensitive volume assignment is helpful for improving the estimation accuracy. Fig. 5 also tells us that the upset due to off-state PMOS is not ignorable in SER estimation.

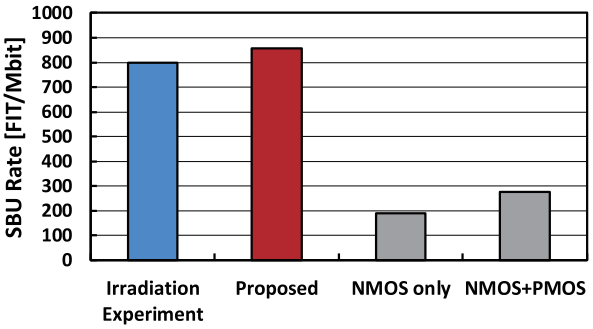

Fig. 5. SERs of experiment and each simulation method.

V. Conclusion

We proposed a SER estimation method that exploited machine learning to facilitate event discrimination in the multiple sensitive volume method. The discriminator is constructed with machine learning using TCAD simulation results as a set of training data. We compared the estimation result with the neutron irradiation result for SOTB SRAM. The estimation error was 7% even though we did not performed any empirical optimization of sensitive volume or critical charge. Compared with the single sensitive method that considered only off-state NMOS, the error was reduced from 76% to 7%, which clarifies the importance of the multiple sensitive volume method.

Acknowledgments

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