Measurement and Mechanism Investigation of Negative and Positive Muon-Induced Upsets in 65-nm Bulk SRAMs

Wang Liao, Masanori Hashimoto, Seiya Manabe, Yukinobu Watanabe, Shin-Ichiro Abe, Keita Nakano, Hikaru Sato, Tadahiro Kin, Koji Hamada, Motonobu Tampo, and Yasuhiro Miyake

***Abstract*—Irradiation experiments of positive and negative muon were conducted for 65-nm bulk CMOS static random-access memory. The experimental results reveal that parasitic bipolar action (PBA) contributes to negative muon-induced upsets. We observe an increase in single event upset (SEU) cross section at higher operation voltage under negative muon irradiation while positive muon shows an opposite decreasing tendency. Also, the proportion of multiple-cell upset (MCU) events to all the negative muon-induced upset events is up to 66, and more than a 20-bit MCU is observed. Furthermore, Monte Carlo simulation of particle and heavy ion transport code system (PHITS) is performed for explaining the difference in SEU between positive and negative muons. We also discuss the charge threshold that triggers PBA-induced MCU using measurement and simulation results with different momentum muons. The estimated threshold is much larger than the charge that the positive muons can deposit, which well explains that no PBA-induced MCUs are observed under positive muon irradiation.**

***Index Terms*—Muons, parasitic bipolar action (PBA), single event upset (SEU), static random-access memorys (SRAMs).**

I. Introduction

Soft errors induced by cosmic rays in the terrestrial environment have been of concern since the susceptibility of devices to soft error increases with the scaling of semiconductor manufacturing technology. Recent literature points out that muons are a potential source of soft error in the terrestrial environment [1]–[5]. Muons are the majority particle on the ground [1], and hence muon-induced soft error is drawing attention in the research community of single event effects.

On one hand, available muon beamlines for irradiation experiments are limited, and hence, up to now, only several accelerator-based irradiation experiments for muon-induced single event upset (SEU) cross section evaluation are reported [1], [2], [4]. Sierawski *et al.* [1] investigated the dependence of static random-access memory (SRAM) SEU on process technologies of 65, 45, and 40 nm at the TRI University Meson Facility (TRIUMF) with a conclusion that the sensitivity to positive muons increase in lower voltage operation. They also evaluated 28 nm SRAMs with operation voltage and momentum scanning at the RIKEN-Rutherford Appleton Laboratory (RIKEN-RAL) [6] and reported the SEU dependence on supply voltage and muon momentum [2]. Seifert *et al.* [4] used a low-energy muon beam at TRIUMF to test SRAMs of 32-nm planar, 22-nm, and 14-nm tri-gate technologies and concluded that the muon-induced SEUs could be neglected in the investigated technologies due to low charge collection efficiencies. On the other hand, simulation-based SEU evaluations are also reported. Seifert *et al.* [4] and Serre *et al.* [5] explained the recent experimental results of positive muons using critical charge. Both of them point out that the negative muons deposit larger charge due to the negative muon capture process. However, no negative muon irradiation tests for submicrometer devices have been reported until now. The most recent irradiation test using negative muons was conducted during 1983–1985 with 4K nMOS SRAM, and only a few errors were observed in [7]. Therefore, we are motivated to carry out irradiation experiments with negative muons on recent technology devices.

In this paper, we report tests of 65-nm bulk CMOS SRAMs with operation voltage and body bias scanning at the Muon Science Facility (MUSE) in Materials and Life Science Experimental Facility (MLF), Japan Proton Accelerator Research Complex (J-PARC). In MUSE, both low-energy negative and positive muons are available. Therefore, we can clarify the difference between positive muons and negative muon-induced upsets. The purpose of this paper is to fill the blank of irradiation experiments with negative muons and to investigate the mechanism of negative muon-induced upset.

The rest of this paper is organized as follows. Section II explains the experimental setup and the structure of SRAM

Manuscript received March 2, 2018; revised April 4, 2018; accepted April 8, 2018. Date of publication April 11, 2018; date of current version August 15, 2018. This work was supported by Grant-in-Aid for Scientific Research (B) from the Japan Society for the Promotion of Science under Grant 16H03906. *(Corresponding author: Wang Liao.)*

W. Liao and M. Hashimoto are with the Department of Information System Engineering, Osaka University, Suita 565-0871, Japan (e-mail: wang.liao@ist.osaka-u.ac.jp; hasimoto@ist.osaka-u.ac.jp).

S. Manabe, Y. Watanabe, K. Nakano, H. Sato, and T. Kin are with the Department of Advanced Energy Engineering Science, Kyushu University, Fukuoka 816-8580, Japan (e-mail: manabe@aees.kyushu-u.ac.jp; watanabe@aees.kyushu-u.ac.jp; knakano@aees.kyushu-u.ac.jp; h.sato@aees.kyushu-u.ac.jp; kin@aees.kyushu-u.ac.jp).

S.-I. Abe is with the Research Group for Radiation Transport Analysis, Japan Atomic Energy Agency, Funaishikawa 319-1184, Japan (e-mail: abe.shinichiro@jaea.go.jp).

K. Hamada and M. Tampo are with the Muon Science Laboratory, High Energy Accelerator Research Organization (KEK), Tsukuba 319-1106, Japan (e-mail: z-hamada@post.kek.jp; mtampo@post.kek.jp).

Y. Miyake is with the Muon Science Laboratory, High Energy Accelerator Research Organization (KEK), Tsukuba 319-1106, Japan, and also with the Materials and Life Science Division, Japan Proton Accelerator Research Complex Center, Muon Section, Shirane Shirakata 319-1195, Japan (e-mail: ymiyake@post.kek.jp).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNS.2018.2825469

0018-9499 © 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

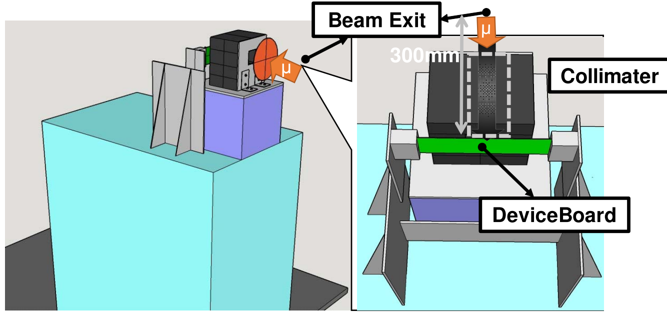

Fig. 1. Overall setup for experiment.

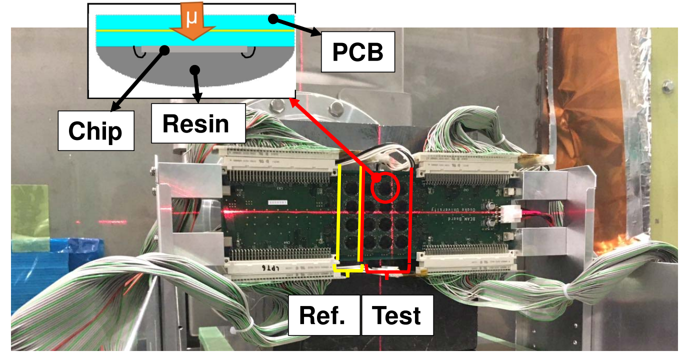

Fig. 2. Device board setup. 12 chips on the board were under test, while the rest of the chips were shaded by the collimator for reference.

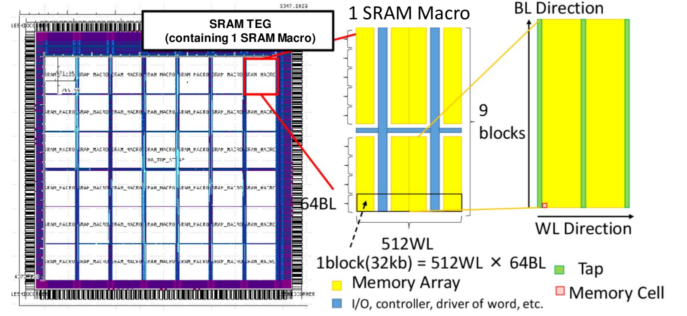

Fig. 3. Structure of SRAM chip under test. For each chip, there are 42 SRAM TEGs. Each TEG contains a 32-kbit SRAM macro. Bit cell distribution in the macro is shown in the right figure of the array. 2 BL × 64 WL cells share the same well.

chips under test. In Section III, we show the test results of positive and negative muons. In Section IV, we analyze the results and confirm our hypothesis that parasitic bipolar action (PBA) contributes to negative muon-induced upsets. For characterizing PBA-induced multiple-cell upset (MCU), Section V conducts Monte Carlo simulation to obtain the distribution of deposited charge, and estimates charge threshold of PBA-induced MCU by combining the simulation and irradiation results with different momentum muon beams.

II. Experimental Setup

Irradiation tests using muons were conducted in MUSE of MLF and J-PARC [8], [9]. Fig. 1 shows the overall setup of our muon irradiation experiment. We placed the device board perpendicularly to the muon beam track, where a collimator was located between the beam exit and the device board. The distance from the beam exit to the device board is 300 mm. Fig. 2 shows the device board and its alignment to the collimator. The device board includes 16 SRAM chips, and it is aligned such that 12 chips are irradiated while the other four chips are shaded by the collimator for reference. In this configuration, 99.98% of upsets were observed in the irradiated 12 chips, which confirm that muon-induced upsets are measured in this setup, and other background particles, e.g., neutrons from other beam lines in MLF and secondary cosmic rays, can be ignored. It should be noted that all the data in this paper were successively measured without any disturbance of the devices to make the results of SEU cross sections comparable.

The thickness of the resin layer on the chips is not spatially uniform as shown in Fig. 2, which changes the depth at which muons stop depending on the location. Instead, the beam was incident from the polychlorinated biphenyl side to make muons with the same momentum stop at a more similar depth. Rigorously speaking, positive and negative muons stop at slightly different depths [10], but this difference was not distinguished in our experiments, which will be explained later. In MUSE, the momenta of negative and positive muons are configurable and quasi-monoenergetic ranging from 24 to 120 MeV/c [8]. In this range, the momentum deviation of the muon beam is of 5%. We take advantage of the narrow momentum deviation to search the momentum that makes muons stop near sensitive volumes inside the chips. Note that we use momentum to express muon energy in this paper. The relationship between momentum P and energy E_k is given by $E_k = (P^2 + m_\mu^2)^{1/2} - m_\mu$, where m_μ is the mass of a muon. The momentum range from 24 to 120 MeV corresponds to the energy range from 2.7 to 54.2 MeV.

Test SRAM chips were fabricated in 65-nm bulk CMOS technology with a deep well option. Fig. 3 shows the structure of the chip used in this paper. Each chip contains 42 SRAM test element groups (TEGs), and each TEG contains 32 kbit. The SRAM cells (bits) in TEG are designed with regular Vth transistors. The cells are arranged in 64 BL × 512 WL, and the cells in every 2 BL × 64 WL share the same well tap, where BL and WL stand for bitline and wordline, respectively. We read out and refresh the data in SRAM chips every ten minutes due to small number of errors and slow voltage transitions for low operation voltage measurement. At a low supply voltage, some SRAM bit cells fail to be read and written. To distinguish read and write fails from muon-induced upsets, we read and write bit cells at a higher voltage and decrease the supply voltage to count upsets during low-voltage hold operation. To make sure the data stored inside cells are unchanged, the voltage transition between low and high voltages is conducted in a slow pace of around 0.1 V/s. In this case, the transition between 1.2 and 0.4 V takes 16 s for a round trip. Note that we did not stop the beam for every read/write process to eliminate manual operation for stopping and restarting the beam and avoid the extra time cost to wait for the beam operation. Without beam stopping, when we read the data more frequently, the hold time becomes relatively

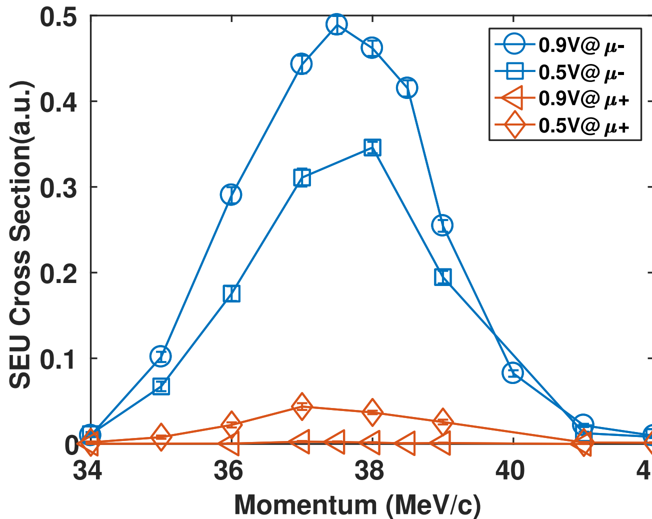

Fig. 4. Dependence of SEU cross section on muon momentum. Zero body bias is given.

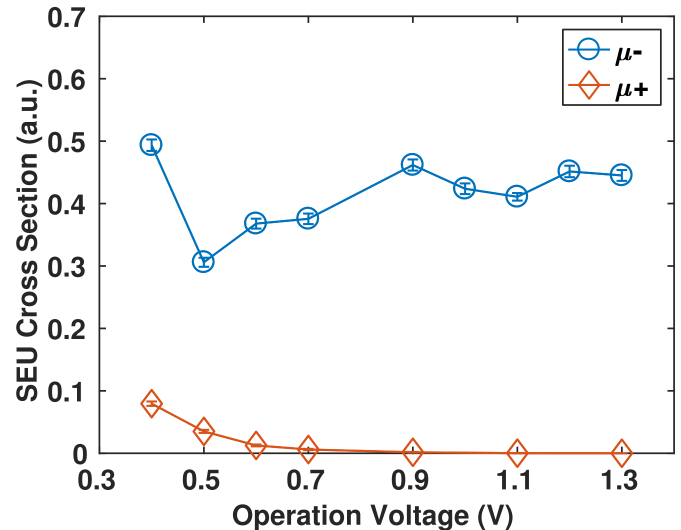

Fig. 5. Dependence of SEU cross section on operation voltage under positive and negative muon irradiation with a momentum of 38 MeV/c. The values of cross section are normalized with the same value as in Fig. 4. Each error bar corresponds to the standard deviation. Zero body bias is given.

shorter than the transition time, and then it becomes difficult to regard the observed errors as errors during the hold operation. On the other hand, when the hold duration is too long, pseudo MCUs caused by single bit upsets (SBUs) in close proximity become a concern. To mitigate these issues, we chose ten minutes. Due to the low proportion of transition time in the total test time, we considered the test as a static test, in which the observed errors mostly occurred during the hold time. The possibility of pseudo MCU is examined in Section III.

A few bits of SRAM fail to be read out properly even with the slow voltage transition, and they are removed from the data for SEU analysis. This failure bit information is carefully acquired before and after the experiments.

III. Experimental Results

A. Momentum Scanning of Positive and Negative Muon

We conducted momentum scanning to search for the maximum peak value of SEU cross section, where the number of upset bits is used for calculating SEU cross section. The number of muons was estimated by the measurement using a plastic scintillator. Fig. 4 shows the dependence of SEU cross section on the momentum of negative and positive muons at 0.5 and 0.9 V operation voltage. These voltages are selected based on the SEU cross section dependence on supply voltage, which will be shown later.

From the result, we find that the SEU cross section reaches a maximum at the momentum between 37 and 38 MeV/c for both positive and negative muons at both operation voltages. This result suggests that the muons with the momentum in the range between 37 and 38 MeV/c are most likely to stop near transistors inside the chip. We will confirm this in Section V with particle and heavy ion transport code system (PHITS) simulator [11]. Here, [10] and [12] point out that the negative muons have a longer flight length compared to that of the positive muons with the same momentum. On the other hand, we observe little peak difference in Fig. 4. Due to the 5% momentum deviation of the muon beam, the difference of flight length might be concealed. Another finding is that the cross section of negative muon-induced SEU is larger at 0.9 V than at 0.5 V, which cannot be explained by critical charge. Detailed voltage dependence will be presented in Section III-B, and the mechanism will be discussed later. To obtain a large enough number of upsets, we fixed the momentum to 38 MeV/c in the following experiments. Furthermore, we will investigate the charge deposited by muons with 38 MeV/c via simulation in Section V.

B. SEU Dependencies on Supply Voltage and Body Bias

Fig. 5 shows the dependence of SEU cross section on operation voltage under the irradiation of positive and negative muons. In Fig. 5, the SEU cross section under negative muon irradiation is at least 9X larger than that under positive muon irradiation. This result confirms that the negative muons induce more upsets in SRAM than the positive muons. We also observe that, under positive muon irradiation, SEU cross section increases monotonically as the supply voltage lowers. This tendency can be explained by the decrease in critical charge. On the other hand, under negative muon irradiation, SEU cross section reaches a lower peak at 0.5 V, and it increases above 0.5 V. These totally different dependencies on supply voltage suggest different upset mechanisms under positive and negative muon irradiation.

Next, Fig. 6 shows the dependence of SEU cross section on body bias under positive and negative muons. Although, the SEU cross section due to negative muons is larger than that due to positive muons in all the bias conditions, the dependence on the body bias is different. Forward body bias (FBB) increases the SEU cross section under negative muon irradiation, while reverse body bias (RBB) increases it under positive muon irradiation. From upset mitigation point of view, RBB is helpful since the cross section reduction for negative muons is much larger than the cross section increase

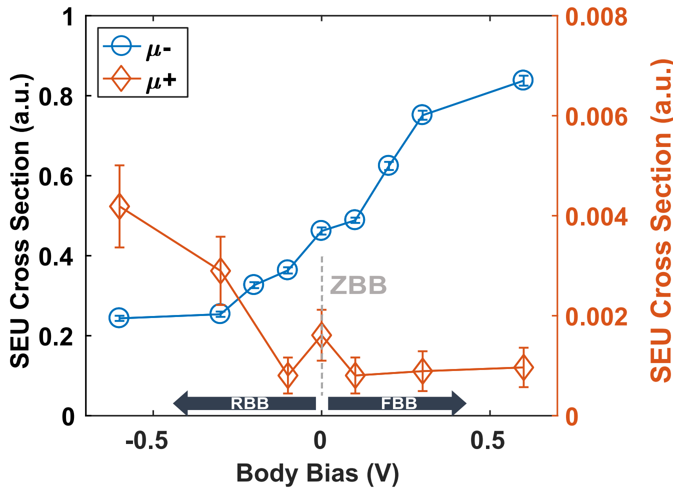

Fig. 6. Dependence of SEU cross section on body bias. The momentum of muons is 38 MeV/c. The values of cross section are normalized with the same value as in Fig. 4. The supply voltage is 0.9 V. Each error bar corresponds to the standard deviation.

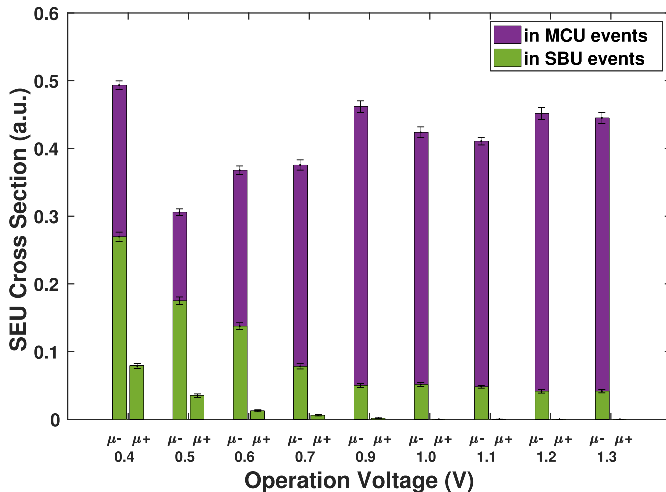

Fig. 7. SEU cross section in which the contributions from MCU and SBU events are separated from Fig. 5. The momentum of negative and positive muons is 38 MeV/c. Zero body bias is given. Each error bar corresponds to the standard deviation.

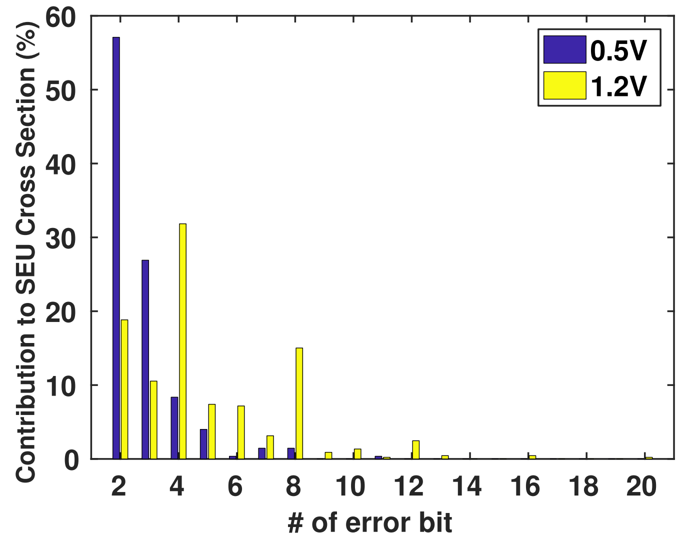

Fig. 8. MCU distributions at 1.2 and 0.5 V. The data come from 0.5 and 1.2 V at voltage dependence scanning under negative muon irradiation with 38 MeV/c in Fig. 5. Zero body bias is given.

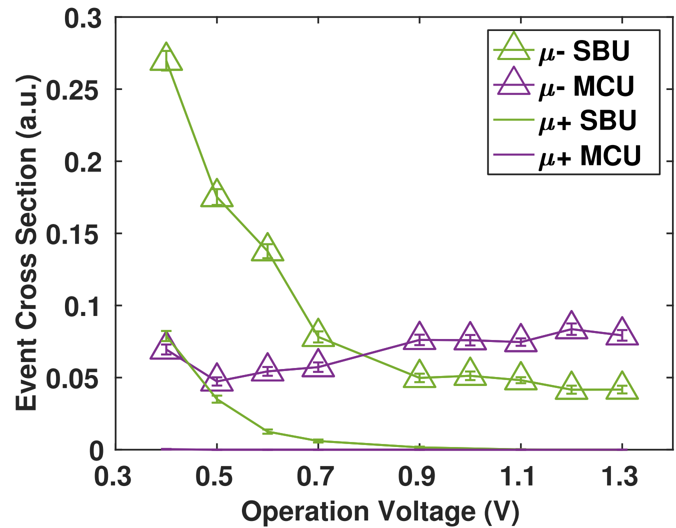

Fig. 9. SBU and MCU event cross sections. The cross sections are calculated with the number of events instead of upset bit numbers. For example, a 2-bit MCU is counted as one event here. The momentum of negative and positive muons is 38 MeV/c. Zero body bias is given. Each error bar corresponds to the standard deviation.

for positive muons, where the fluxes of negative and positive muons are almost the same in terrestrial environment [13].

C. Multiple-Cell Upset versus Single Bit Upset

We categorized the negative muon-induced upsets into MCU and SBU. MCU refers to upsets that happen in adjacent cells and are caused by the same event. MCU can spoil error correction code and hence its proportion and tendency are crucially important. The contributions of MCU and SBU to SEU cross section are plotted in Fig. 7. Note that the total SEU cross sections in Fig. 7 are the same with those in Fig. 5. In Fig. 7, SBU increases as the operating voltage decreases. MCU, on the other hand, rises above 0.5 V. Fig. 8 shows the MCU distributions at 1.2 and 0.5 V, respectively. At the low voltage of 0.5 V, the ratio of larger bit MCU event is smaller. Meanwhile, at a high voltage of 1.2 V, large-bit MCUs, such as over 20-bit MCUs, are observed.

On the other hand, we observed only two MCU events at 0.4 V and no MCU events at 0.5 V and above under positive muon irradiation. Fig. 9 shows the event cross sections of SBU and MCU, where the cross sections are calculated with the number of events. This means, for example, a 2-bit MCU is counted as only one MCU event here. The MCU event cross section due to negative muons is at least three orders of magnitude higher than that due to positive muons, which clearly points out that the negative muons lead to a significant increase in MCUs.

Meanwhile, due to the interval of ten minutes for data reading, we need to prove the MCUs observed in our experiment were caused by a single event. For this purpose,

we calculated the maximum percentage of two-bit pseudo-MCUs caused by multiple events. The probability of SBU is calculated as

$$P_{\mathrm{SBU}} = \frac{N_{\mathrm{SBU}}}{N_{\mathrm{TotalBits}}} \tag{1}$$

where N_{SBU} represents the number of SBUs in a period of irradiation, and $N_{\mathrm{TotalBits}}$ stands for the total number of bits under test. Here, we consider all the upsets as SBUs to maximize P_{SBU} and consequently the probability of pseudo-MCU. Then, the probability of pseudo MCU is calculated as follows:

$$P_{\mathrm{pseudoMCU}} = {}_8C_1 \cdot P_{\mathrm{SBU}}^2 \tag{2}$$

where ${}_8C_1 = 8$ stands for eight possible positions next to the bit cell of interest in either horizontal, vertical, or diagonal direction. The maximum number of MCU is calculated as the product of $N_{\mathrm{TotalBits}}$ and $P_{\mathrm{pseudoMCU}}$, and then the maximum percentage of pseudo-MCU over the number of measured MCUs N_{MCU} is

$$\mathrm{Per}_{\mathrm{pseudoMCU}} = \frac{\mathrm{N_{TotalBits}} \cdot \mathrm{P_{pseudoMCU}}}{\mathrm{N_{MCU}}}. \tag{3}$$

The calculated percentages of pseudo two-bit MCU at 1.2 and 0.5 V are 0.054% and 0.088%, respectively. Therefore, we can statistically conclude that all MCUs observed in our experiment can be regarded as MCUs caused by a single event.

IV. Discussion on Parasitic Bipolar Action With Measurement Results

Section III shows that the SEU cross section due to negative muons is higher than that due to positive muons. This difference of SEU cross section is thought to originate from larger charge deposition due to negative muon capture process since the charge deposition due to direct ionization is supposed to be almost identical for negative and positive muons. A detailed comparison of the charge deposition between positive and negative muons is presented in [5] by simulation.

In this paper, we investigate the upset mechanism, especially due to negative muons, to explain the dependence of SEU cross section on supply voltage under negative muon irradiation. Deposited charge is collected at the drain by drift and diffusion. In addition, the deposited charge can cause PBA [14]–[16]. Fig. 10 illustrates the mechanism of PBA taking nMOS transistors as an example. The deposited charge is collected at the p-well tap. During this charge collection, a current flows in the well, which induces a well potential rise due to R_{PW2}. This potential rise turns on the parasitic n-p-n bipolar transistor, and a large current flows through this parasitic bipolar transistor, which results in SRAM bit upset. It should be noted that the base of the bipolar transistors in the same well is shared in the same p-substrate/n-well, and hence the bipolar transistors within the adjacent bit cells tend to turn on simultaneously. It is reported that this is the main mechanism of neutron-induced larger bit MCU in bulk SRAM [17].

Meanwhile, critical charge increases with supply voltage. Therefore, taking into account only drift and diffusion charge

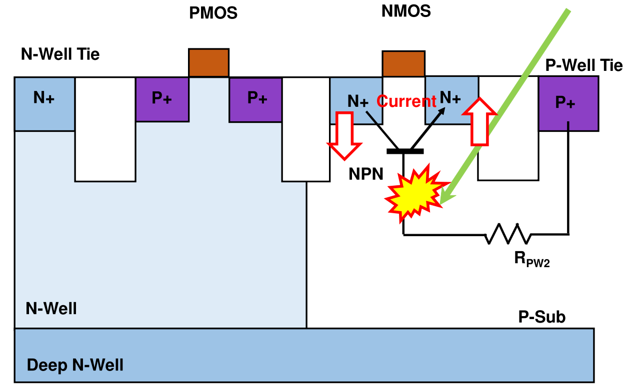

Fig. 10. PBA caused by nMOS transistors is exemplified. The parasitic n-p-n bipolar transistor can provide a current conducting path between source and drain. When charge deposition elevates the potential of substrate and it reaches a threshold, n-p-n becomes ON. Body bias changes the amount of charge necessary to reach the threshold.

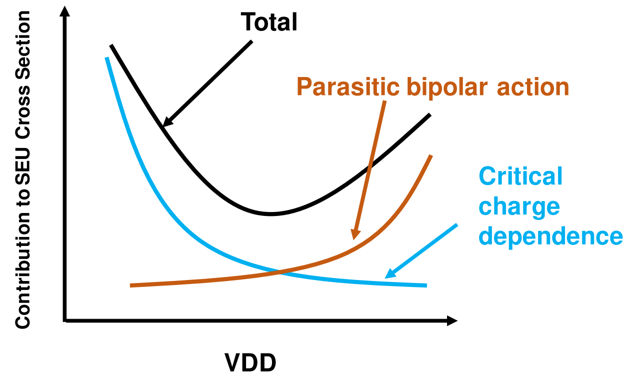

Fig. 11. A conceptual illustration explaining SEU cross section dependence on supply voltage.

collection, SEU decreases as the supply voltage rises. This tendency is observed in the cross section of positive muon-induced SEU in Fig. 5, which indicates that the upsets due to positive muons are caused by collecting the charge produced by direct ionization via drift and diffusion.

In the case of negative muons, on the other hand, upsets are thought to be caused by PBA in addition to drift and diffusion charge collection. Similar to neutron-induced upsets [18], the contribution of PBA to SEU cross section is expected to become significant as the supply voltage rises. On the other hand, as the supply voltage becomes lower, the PBA contribution becomes less significant, and the drift/diffusion charge collection becomes more dominant similar to positive muon. In this case, as the supply voltage lowers, the SEU cross section increases. These two tendencies are superposed as illustrated in Fig. 11, and then the SEU cross section has a minimum point in terms of supply voltage as observed in Fig. 7. It should be noted that MCUs at 0.4 V are also caused by charge sharing at the adjacent SRAM cells via drift and diffusion since the critical charge decreases. Consequently, two-bit MCU is dominant at 0.5 V.

In our test SRAM, as explained in Section II, a large bit block of 2 BL × 64 WL shares the same well/substrate, and

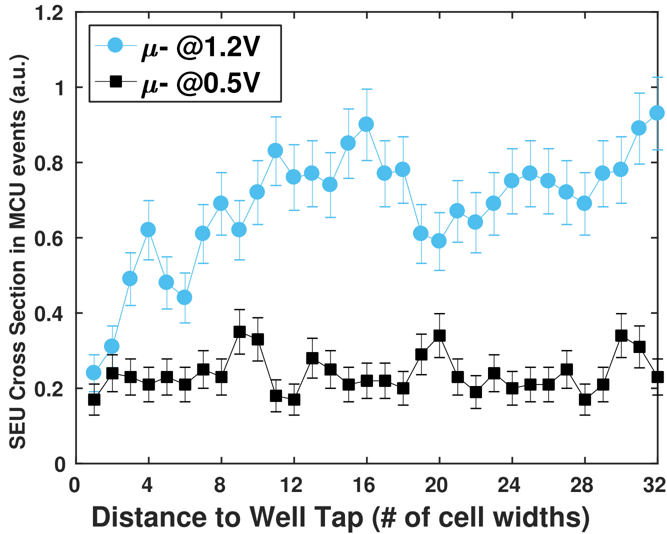

Fig. 12. SEU cross section in MCU events as a function of distance from well tap. Strong dependence on distance near the well tap at 1.2 V is explained by PBA. 38-MeV/c negative muon is irradiated. Zero body bias is given.

then PBA can cause MCUs within it. We confirmed that 99.95% of the observed MCUs occurred in the same well. Most of the MCUs being in the same well are consistent with the possibility of pseudo MCUs calculated in Section III-C. MCUs having more than three bits, which are difficult to occur due to charge sharing, are observed as shown in Fig. 8. In addition, the MCU cross section is gradually increasing as the operation voltage becomes higher than 0.5 V in Fig. 9. All these tendencies suggest that PBA plays a significant role in negative muon-induced upsets. This hypothesis is also supported by the dependence of SEU cross section on body bias shown in Fig. 6. With FBB, the charge required to turn on the n-p-n transistor decreases because smaller potential fluctuation at p-substrate/n-well exceeds the base–emitter threshold. Therefore, the SEU cross section increases under FBB and, on the contrary, it decreases under RBB. This explanation is consistent with the SEU cross section measured in our experiment.

In addition, we investigate the number of upsets of MCUs associated with the distance from the well tap. If PBA is prominent, cells distant from the well tap should be more susceptible, whereas PBA is suppressed near the well tap. In our test SRAM chip, 64 BL $\times$ 2 WL cells share the same well taps. Therefore, the longest distance to the well tap is 32 cell widths. Fig. 12 shows the SEU cross section in MCU events as a function of the distance to the well tap in negative muon irradiation at 0.5 and 1.2 V. At 1.2 V, the cross section of the cells near the well tap strongly depends on the distance and beyond the distance of eight, the cross section keeps large compared to that of the cells near taps, while such a dependence on the distance of the cells near the well tap is not observed at 0.5 V. Therefore, PBA is highly possible to contribute to upsets in the negative muon irradiation test. Meanwhile, for the cells relatively far away from the well taps, we observed some fluctuations in the cross section values, e.g., the cross section value at nine cell widths was higher than that of neighbor cells at 0.5 V. On the other hand, due to the low statistical error numbers, we could not make a further conclusion on the relationship between the distance from the tap and the cross section.

Finally, let us make a brief comment on the influence of deep n-well option. Reference [19] reports that deep n-well increases the cross section of neutron-induced MCU. Meanwhile, even without deep n-well, [19] observed neutron-induced 8-bit MCUs caused by PBA, which may suggest negative muon also could cause large-bit MCUs even in SRAMs without deep-well while the cross section could be lower.

V. Estimating Charge Threshold of PBA-Induced MCU With Different Momentum Muon Beams

In Section IV, we revealed the existence of PBA-induced MCU under negative muon irradiation. However, we also noticed the PBA-induced MCU is unlikely to occur under positive muon irradiation. For explaining the difference of negative and positive muon irradiation, it is necessary to compare the amount of deposited charge and the charge threshold of PBA-induced MCU. Monte Carlo simulation with PHITS [11] can provide the estimate of deposited charge. The charge threshold of PBA-induced MCU is, on the other hand, generally difficult to predict since a large 3-D structure that includes multiple SRAM cells must be simulated by technology computer aided design whereas [20] provided an efficient way to simulate PBA-induced MCU by a combination of device and circuit simulations.

In this paper, we notice the advantage of manipulatable charge deposition thanks to different momentum beams and propose another method to estimate charge threshold of PBA-induced MCU by a combination of experiment and Monte Carlo simulation. This method may give a hint about charge threshold characterization with muon beams.

A. Momentum Dependence of Deposited Charge

As a preparation for estimating threshold charge of PBA-induced MCU, we first discuss the depth at which muons stop and the deposited charge for various momenta muons with simulation. For calculating these, we reproduced the experiment setup of Fig. 1 as a 3-D model for PHITS [11].

First, to verify the model, the stopping depth of positive muons with different momenta is investigated with PHITS simulation. The result in Fig. 13 shows that muons with 38 MeV/c stop most closely to the sensitive volume compared with the other momenta. Here, the current PHITS cannot consider Barkas correction [12] to compensate the small difference of stopping power between positive and negative muons, and hence the result of negative muons, which is expected to be almost identical, is not presented.

Next, for obtaining the deposited charge data, we injected a total number of 6×10^8 muons for each momentum. Momenta of 38, 36, and 40 MeV/c are selected for simulation, since, the relatively large number of upsets were observed in the irradiation experiment. We selected the sensitive volume (SV) including the depletion region and calculated the charge deposited in the SV, where the SV depth is 400 nm.

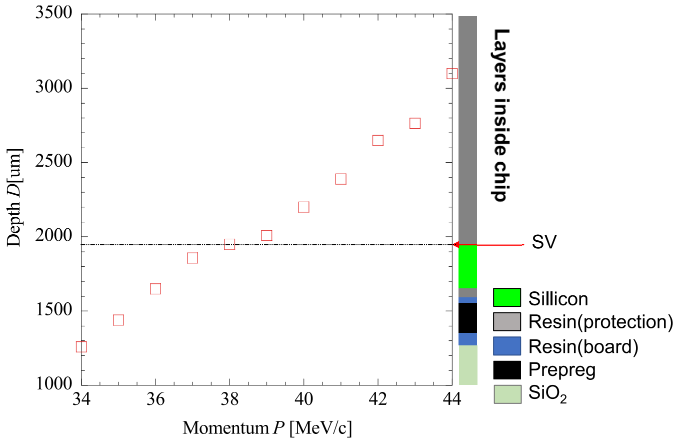

Fig. 13. Stopping depth of muons with different momenta is used in experiment. The depth of 38-MeV/c muon is the closest to SV compared with the other momenta.

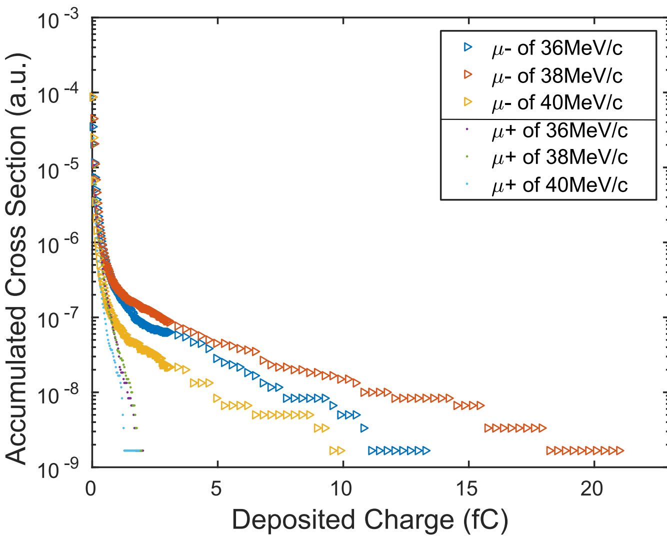

Fig. 14. Accumulated cross section $\sigma_{\mathrm{ac}}(C_{\mathrm{dep}})$ of events associated with deposited charge C_{dep} corresponds to the number of events that deposit over C_{dep}.

The accumulated cross section $\sigma_{\mathrm{ac}}(C_{\mathrm{dep}})$ in terms of the deposited charge C_{dep} is shown in Fig. 14 for both negative and positive muons. Focusing on negative muons, we observe that the accumulated cross section of 38 MeV/c is higher than those of 36 and 40 MeV/c above 2 fC, which explains the reason why the SEU cross section reached a maximum at 38 MeV/c in the momentum scanning. On the other hand, a similar observation is found for positive muons as shown in Fig. 14 while the spread is much smaller than that of negative muons. Looking back at the SEU cross sections shown in Fig. 4, we find the consistency, i.e., the muon that deposits larger charge tends to have larger SEU cross section, especially for negative muon.

The key observation is that the negative muon can cause events that deposit large charge over 5 fC, whereas the positive muon cannot deposit 5 fC. For giving a reference, we estimated the threshold of charge collected at the drain that can induce an SBU by circuit simulation with a double-exponential model.

TABLE I
ESTIMATED RESULT OF MCU CHARGE THRESHOLD AT 0.9 V

N	2	3	4	5
C_N(fC) from 36, 38 MeV/c	6.5	6.6	7.1	8.2
C_N(fC) from 38, 40 MeV/c	7.7	7.6	7.9	8.3

The threshold of collected charge is 1.0 fC at 0.9 V, suggesting that both the negative and positive muons are able to induce SBUs. In Section V-B, we conduct a further investigation on the threshold for PBA via the relationship between the MCU event cross section and the accumulated cross section.

B. MCU Charge Threshold for PBA

For estimating charge threshold C_N of N-bit and larger MCUs due to PBA, we use a simple assumption of linear relation between MCU event cross section $\sigma_{N\text{-MCU}}$, which represents the cross section of events that cause N-bit and larger MCUs, and accumulated cross section $\sigma_{\mathrm{ac}}(C_N)$, that is

$$\sigma_{N-\mathrm{MCU}} = k_N \sigma_{\mathrm{ac}}(C_N) \tag{4}$$

where k_N is a coefficient and C_N is the parameter to be estimated. Reference [20] shows a relationship between charge deposit in sensitive volume and MCUs. The relationship is not linear, but monotonic before saturation. Here, $\sigma_{N\text{-MCU}}$ is available with the irradiation experiment and $\sigma_{\mathrm{ac}}(C_{\mathrm{dep}})$ can be prepared with the simulation. On the other hand, there are two unknown parameters of k_N and C_N, and hence we need to prepare two different data sets to determine k_N and C_N. Fortunately, we have several data sets that are obtained for different momenta of muon beams. Let us suppose $\sigma^{(m1)}_{N\text{-MCU}}$, $\sigma^{(m2)}_{N\text{-MCU}}$, $\sigma^{(m1)}_{\mathrm{ac}}(C_{\mathrm{dep}})$, and $\sigma^{(m2)}_{\mathrm{ac}}(C_{\mathrm{dep}})$ are available for the momenta of $m1$ and $m2$. In this case, we can eliminate k_N from (4) as follows:

$$\frac{\sigma^{(m1)}_{\mathrm{ac}}(C_N)}{\sigma^{(m2)}_{\mathrm{ac}}(C_N)} = \frac{\sigma^{(m1)}_{N\text{-MCU}}}{\sigma^{(m2)}_{N\text{-MCU}}}. \tag{5}$$

By solving (5) with respect to C_N, we can obtain C_N.

For validating the discussion above, we estimated MCU charge threshold C_N for two sets of momenta; (36 and 38 MeV/c) and (38 and 40 MeV/c). The estimated results are listed in Table. I.

For two-bit MCU, the charge thresholds are estimated to be 6.5 and 7.7 fC, which are not identical but similar with 15% difference. For larger MCU, the difference becomes smaller. These results suggest that the assumption of (4), the PHITS simulation and the derivation of charge threshold are reasonable. On the other hand, we notice that C_3 is larger than C_2 when they are calculated from 38 and 40 MeV/c momenta. A possible reason is a statistical uncertainty originating from the relatively small number of MCUs. A similar trend is also observed when calculating C_N for larger N values. This suggests a necessity of a much larger number of MCU events for the MCU charge threshold characterization with higher precision.

The estimated MCU charge threshold clearly demonstrates that the PBA-induced MCU cannot occur under positive muon

irradiation since there are no events that can deposit more than 5 fC as presented in Fig. 14.

VI. Conclusion

The cross section of negative muon-induced SEUs in bulk SRAM is characterized with comprehensive statistics through irradiation test. Experimental results under positive and negative muon irradiation show the negative muons lead to higher SEU cross section than the positive muons. The cross section of negative muon-induced SEUs increases at both low and high voltages. RBB benefits the SRAM for smaller SEU cross section. In addition, negative muons cause large MCUs of more than 20 bits, and the ratio of MCU events to all the events is 66% at 1.2 V. These results indicate that the negative muons lead to a significant increase in MCU cross section. To clarify the mechanism of negative muon-induced upsets, we focused on PBA and discussed its consistency with the measurement results. Our discussion confirmed that all the measurement results were consistent with the knowledge of PBA effects acquired by studies on neutron-induced upsets. Taking advantage of the manipulatable momentum of muons at MUSE, we proposed a method to predict charge threshold for PBA-induced MCU. The estimated charge threshold well explains the few MCU occurrences in positive muon irradiation.

Our future work will include the calculation of muon-induced SER in terrestrial environment by integrating SEU cross section multiplied by differential flux in terms of particle energy according to [21]. On the other hand, the cross section in a wide range of energy, especially at high energy range, needs to be measured. However, the cross section at high energy range is expected to be low and its measurement is time-consuming while the beam time is limited. Simulation-based cross section evaluation needs to be studied. We will include the comparison with other particles, such as neutron and alpha particle, in the future work.

Acknowledgment

This muon experiment was performed at Materials and Life Science Experimental Facility of the J-PARC under user programs Nos. 2016B0046 and 2017A0139.

References

[1] B. D. Sierawski *et al.*, "Muon-induced single event upsets in deep-submicron technology," *IEEE Trans. Plasma Sci.*, vol. 57, no. 6, pp. 3273–3278, Dec. 2010.

[2] B. D. Sierawski *et al.*, "Bias dependence of muon-induced single event upsets in 28 nm static random access memories," in *Proc. IRPS*, Jun. 2014, pp. 2B.2.1–2B.2.5.

[3] E. W. Blackmore, M. Stukel, M. Trinczek, C. Slayman, S.-J. Wen, and R. Wong, "Terrestrial muon flux measurement at low energies for soft error studies," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 6, pp. 2792–2796, Dec. 2015.

[4] N. Seifert, S. Jahinuzzaman, J. Velamala, and N. Patel, "Susceptibility of planar and 3D tri-gate technologies to muon-induced single event upsets," in *Proc. IRPS*, Apr. 2015, pp. 2C.1.1–2C.1.6.

[5] S. Serre, S. Semikh, J. L. Autran, D. Munteanu, G. Gasiot, and P. Roche, "Effects of low energy muons on electronics: Physical insights and geant4 simulation," in *Proc. Eur. Conf. RADECS*, Sep. 2012, pp. 1–7. [Online]. Available: http://www.im2np.fr/news/articles/RADECS2012_Muons_Proceedings.pdf

[6] K. Nagamine *et al.*, "Construction of RIKEN-RAL muon facility at ISIS and advanced μSR," *Hyperfine Interact.*, vol. 87, pp. 1091–1098, Dec. 1994.

[7] J. F. Dicello, "Microelectronics and microdosimetry," *Nucl. Instrum. Methods Phys. Res. B, Beam Interact. Mater. At.*, vols. 24–25, no. 2, pp. 1044–1049, Apr. 1987.

[8] Y. Miyake *et al.*, "J-PARC muon source, MUSE," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 600, no. 1, pp. 22–24, Feb. 2009.

[9] Y. Miyake *et al.*, "Current status of the J-PARC muon facility, MUSE," *J. Phys., Conf. Ser.*, vol. 551, no. 1, p. 012061, 2014.

[10] D. E. Groom, N. V. Mokhov, and S. I. Striganov, "Muon stopping power and range tables 10 MeV–100 TeV," *Atomic Data Nucl. Data Tables*, vol. 78, no. 2, pp. 183–356, Jul. 2001.

[11] T. Sato *et al.*, "Particle and heavy ion transport code system, PHITS, version 2.52," *J. Nucl. Sci. Technol.*, vol. 50, no. 9, pp. 913–923, Jul. 2013.

[12] W. H. Barkas, W. Birnbaum, and F. M. Smith, "Mass-ratio method applied to the measurement of *L*-meson masses and the energy balance in pion decay," *Phys. Rev.*, vol. 101, no. 2, pp. 778–795, Jan. 1956.

[13] T. Sato, "Analytical model for estimating the zenith angle dependence of terrestrial cosmic ray fluxes," *PLoS ONE*, vol. 11, no. 8, p. e0160390, pp. 1–22, Aug. 2016.

[14] J. D. Black, P. E. Dodd, and K. M. Warren, "Physics of multiple-node charge collection and impacts on single-event characterization and soft error rate prediction," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 1836–1851, Jun. 2013.

[15] T. Uemura, T. Kato, and H. Matsuyama, "Impact of parasitic bipolar action and soft-error trend in bulk CMOS at terrestrial environment," in *Proc. IRPS*, Apr. 2013, pp. 6C.4.1–6C.4.6.

[16] E. Ibe *et al.*, "Spreading diversity in multi-cell neutron-induced upsets with device scaling," in *Proc. Custom Integr. Circuits Conf.*, Sep. 2006, pp. 437–444.

[17] H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "Neutron-induced soft errors and multiple cell upsets in 65-nm 10T subthreshold SRAM," *IEEE Trans. Plasma Sci.*, vol. 58, no. 4, pp. 2097–2102, Aug. 2011.

[18] T. Uemura, "A study on soft error mitigation for microprocessor in bulk CMOS technology," Ph.D. dissertation, Dept. Syst. Eng., Osaka Univ., Suita, Japan, 2015.

[19] G. Gasiot, D. Giot, and P. Roche, "Multiple cell upsets as the key contribution to the total SER of 65 nm CMOS SRAMs and its dependence on well engineering," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2468–2473, Dec. 2007.

[20] K. Osada, K. Yamaguchi, Y. Saitoh, and T. Kawahara, "SRAM immunity to cosmic-ray-induced multierrors based on analysis of an induced parasitic bipolar effect," *IEEE J. Solid-State Circuits*, vol. 39, no. 5, pp. 827–833, May 2004.

[21] M. S. Gordon *et al.*, "Measurement of the flux and energy spectrum of cosmic-ray induced neutrons on the ground," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3427–3434, Dec. 2004.