Negative and Positive Muon-Induced Single Event Upsets in 65-nm UTBB SOI SRAMs

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***Abstract*— We have performed an irradiation test of low-energy positive and negative muons on 65-nm ultra-thin body and thin buried oxide silicon-on-insulator static random access memories. The single event upset (SEU) cross sections were measured systematically as a function of incident muon momentum and operating supply voltage. The experimental results show that the negative muon SEUs occur at about three times higher rate than the positive muon ones at the supply voltage of 0.5 V when the incident muons stop near the sensitive volume (SV). A Monte-Carlo simulation with the particle and heavy ion transport code system (PHITS) was carried out using a simple SV model. The simulation based on the PHITS using the SV model is found to reproduce generally well the momentum dependence of the measured SEU cross sections for both positive and negative muons. From the simulation, the charged particles and secondary ions having significant influence on SEUs are specified and the differences between negative and positive muons are discussed.**

***Index Terms*— 65-nm ultra-thin body and thin buried oxide silicon-on-insulator (UTBB-SOI) static random access memory (SRAM), accelerated testing, negative and positive muons, single event upset (SEU).**

I. Introduction

THE problem of soft errors in very large scale integrated (VLSI) circuits subjected to the terrestrial radiation environment has been recognized as a major threat for electronics used at ground level. Radiation-induced soft error means a temporary malfunction in VLSI circuits due to single event upsets (SEUs) caused by the transient signal induced by energetic ionizing radiation, e.g., resulting in upset of memory information in static random access memories (SRAMs).

A major component of secondary cosmic rays at ground level is known to be muons and its fraction is about three-quarters of the total cosmic-ray flux. Many works have been devoted to muon-induced soft errors. Ziegler and Lanford [1] investigated cosmic-ray-induced error rates on typical computer memory circuits and predicted that devices with extremely low critical charge will be susceptible to soft errors induced by cosmic-ray muons. Dicello *et al.* [2]–[5], reported on experimental investigation of muon and pion-induced SEUs and discussed their contribution to the sea level error rate. They performed some experiments with negative and positive muon beams at LAMPF [6]. However, only a few errors were observed during muon irradiation because the beam intensity was not enough and the critical charge of devices used in the irradiation tests (e.g., 4 K nMOS SRAM) was relatively high compared to modern devices.

For a while after these works performed in 1980s, the effect of cosmic-ray muons on soft errors had not been considered to be serious because only a small amount of energy is deposited in devices due to their small stopping power and the deposition charge cannot exceed the critical charge. In recent years, a reduction in resilience to soft errors has become evident since the critical charge has decreased by the miniaturization and low-voltage operation of circuits. Thus, muon-induced soft error is drawing attention again and several papers have been published [7]–[12]. A series of muon-induced SEU experiments were performed using low-energy positive muon beams at TRIUMF and the Rutherford Appleton ISIS facility by Sierawski *et al.* [7]–[9]. They demonstrated the effects of muon direct ionization for bulk SRAMs of different technology nodes (65, 55, 45, and 40 nm). Then, similar SEU experiments with a low-energy positive muon beam were conducted at TRIUMF: 28-nm ultra-thin body and thin buried oxide (UTBB) fully depleted silicon-on-insulator (FDSOI) and bulk SRAMs [10], and SRAMs built on 32-nm planar and 22- and 14-nm 3-D tri-gate technologies [11]. Their experimental results [10], [11] showed the advantage of FDSOI and 3-D tri-gate technologies with respect to the tolerance on muon-induced SEUs.

However, no negative muon irradiation test with modern devices has been reported until now. In a recent numerical

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simulation on 65-nm SRAMs Serre *et al.* [12], showed that a residual heavy nucleus and light particles generated by negative muon capture reactions cause SEUs significantly if muons are stopped and captured by nuclei near the sensitive drain region. Thus, negative muon irradiation tests have been needed for reliable simulation-based estimations of muon-induced soft errors at ground level.

Under these circumstances, we have conducted a series of irradiation experiments with both "positive" and "negative" muon beams at the muon science (MUSE) facility [13], [14] in Materials and Life Science Experimental Facility of the Japan Proton Accelerator Research Complex (J-PARC). The SEU cross sections for 65-nm UTBB-SOI SRAMs were measured as a function of incident muon momentum and operating supply voltage. In addition to the experiment, we have carried out a Monte-Carlo simulation based on the particle and heavy ion transport code system (PHITS) [15] using the sensitive volume (SV) model [16] in order to analyze the experimental result. The momentum dependence of the calculated SEU cross sections is compared with the measured ones. Moreover, the simulation clarifies which charged particles and/or secondary ions contribute mainly to muon-induced SEUs. The main purpose of this paper is to investigate the effect of negative muon capture reactions on SEUs by comparison with positive muon-induced SEUs through both the measurement and simulation.

The rest of this paper is organized as follows. Section II describes the characteristics of muons briefly. In Section III, the experimental setup and the method of measuring muon-induced SEU cross sections are explained. In Section IV, the measured SEU cross sections are shown and discussed with comparison to the previous studies. In Section V, the simulation method is described and the experimental result is compared with the simulation. Finally, Section VI concludes with a brief summary.

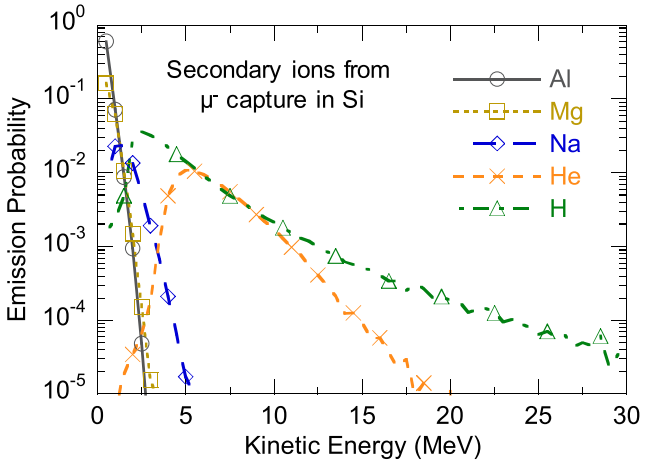

Fig. 1. Calculated energy spectra of secondary light and heavy ions from the negative muon capture reaction in silicon.

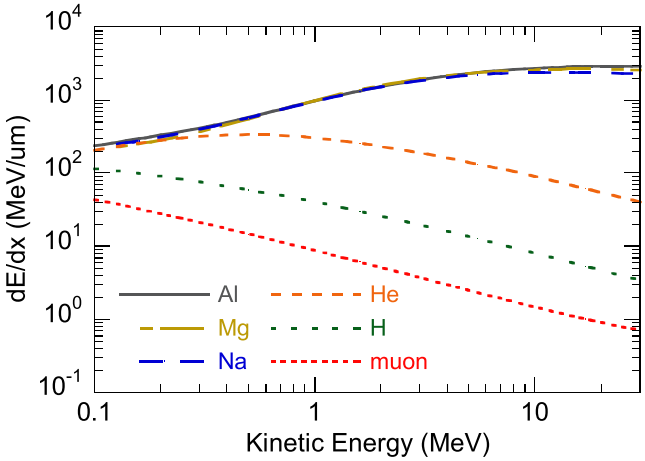

Fig. 2. Stopping power, *dE*/*dx*, for muons and secondary ions in silicon as a function of kinetic energy, which was calculated using SRIM [19].

II. Characteristic of Muons

Muons are elementary particles similar to electrons, but the muon mass is 105.7 MeV/c^2 which is 207 times larger than the electron mass. Muons are classified into negatively charged muons (negative muons) and positively charged antiparticles (positive muons). Negative and positive muons are denoted by μ^- and μ^+, respectively. Muons are unstable particles and decay into three particles with the mean lifetime of 2.2 μs

$$\begin{aligned} \mu^- &\rightarrow e^- + \bar{\nu}_e + \nu_\mu \\ \mu^+ &\rightarrow e^+ + \nu_e + \bar{\nu}_\mu. \end{aligned} \tag{1}$$

A muon passing through matter loses its kinetic energy by generating electron–hole pairs along the track. After losing incident kinetic energy and stopping in matter, the positive muon decays into a positron and two neutrinos as shown in (1). On the other hand, the negative muon is captured by an atom in matter into high orbital momentum states, forming a muonic atom. The captured muon cascades down to the 1-s orbital while emitting characteristic X-rays. A portion of the captured negative muons decay into an electron and two neutrinos in the 1-s orbital as shown in (1). The remaining negative muons are finally absorbed by the nucleus, and a highly excited nucleus is formed. Then, the nucleus is deexcited by emission of neutrinos, photons, neutrons, and other light ions. The muon capture in nuclei is reviewed from the viewpoint of nuclear physics in [17]. When the negative muons stop in silicon, about 65% of them are captured by the nucleus and the remaining muons decay into electrons and neutrinos in the 1-s orbital. Thus, the capture reaction generates a heavy recoiling nucleus with simultaneous emission of secondary light ions (protons, deuterons, α-particles, etc.,) Fig. 1 shows the energy spectra calculated by PHITS [15], [18] for the secondary light and heavy ions from the negative muon capture reaction in silicon. The H and He ions are energetically favored, while the heavy recoiling nuclei (Al, Mg, and Ng) have kinetic energies lower than 5 MeV. In Fig. 2, the stopping power for muons is compared with that for secondary ions as a function of kinetic energy. Since all secondary ions have much larger stopping power than muons, it is expected that the secondary ions deposit sufficient charge in the small SV of SRAMs to cause single event effects.

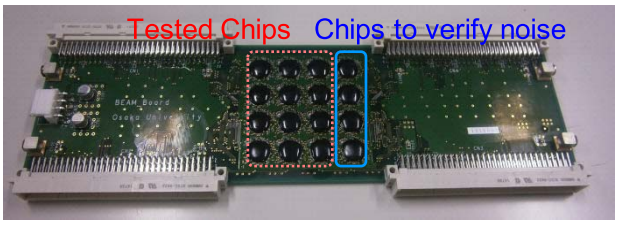

Fig. 3. Photograph of the device board under test.

III. Experiment

A. Test Facility

Accelerator-based tests with both negative and positive muons were performed using the D2 experimental area at J-PARC Muon Facility, MUSE [13], [14]. Muons are decay products of pions. The facility produces pions through nuclear reactions between a 3-GeV proton beam and a 20-mm-thick graphite target. The produced pions decay into muons in a long superconducting solenoid magnet and the decay muons are transported downstream to the D experimental area. In the experiment, the 3-GeV proton synchrotron was operated in a single bunch mode with a repetition rate of 25 Hz and the average power was 150 kW. The momentum distribution of the muon beam can be approximated as a normal distribution with a 5% standard deviation, and the temporal width of the pulsed muon beam was 100–130 ns.

B. Tested Device

Silicon on a thin buried oxide (SOTB)/UTBB FD-SOI device [20] was used in the experiment. The SOTB device has better threshold voltage controllability with body biasing by thinning the insulator layer under the channel region [21]. Fig. 3 shows the device board under test, on which 16 chips of SOTB SRAMs are configured. Each chip has 12-Mbit memories. The chips were fabricated in 65-nm complementary metal–oxide–semiconductor technology. The same test board was used in the previous neutron irradiation experiment and the details of the device were described in [22] and [23]. SRAMs at the 65-nm technology scale were chosen to compare experimental results with the previous numerical simulation by Serre *et al.* [12].

C. Experimental Method of Muon Irradiation

The experimental setup at the D2 experimental area is shown in Fig. 4. The configuration of muon irradiation is schematically illustrated in Fig. 5. The beam collimator was placed between the beam exit and the device board. The collimator slit was 50 mm × 50 mm square-shaped. The collimator consisted of a 5-mm-thick aluminum plate and piled-up 150-mm-thick lead blocks. The aluminum plate was chosen so that the emission of background particles (e.g., neutrons and light ions) from negative muon capture by nuclei in the plate can be reduced because low-Z materials have lower capture rate of negative muons. The lead blocks play a role in the shielding of decay electrons/positrons from the aluminum plate and background γ-rays. 12 chips in the

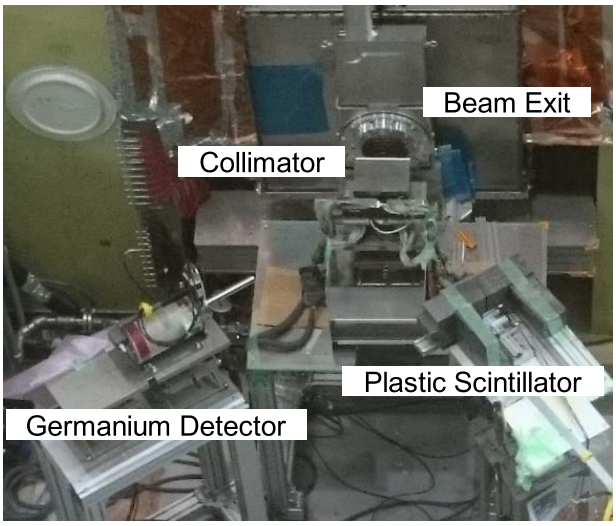

Fig. 4. Experimental setup.

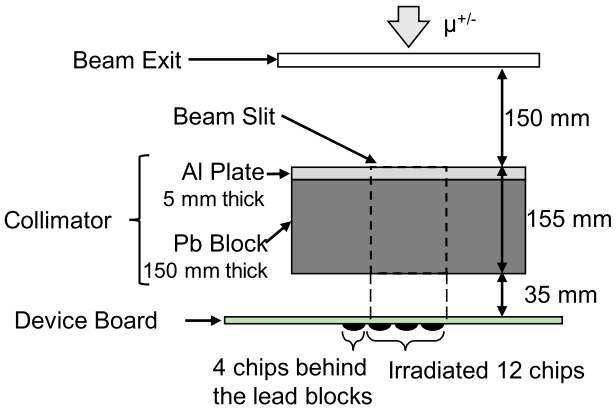

Fig. 5. Schematic illustration of muon irradiation on the device board.

device were irradiated and the remaining four chips were placed behind the lead blocks in order to see the influence of background radiation in the environment.

The reverse side of the device board was irradiated with the muon beam passing through the collimator, as shown in Fig. 5. Muons stopped in the device board undergo the decay into electrons/positrons. They were detected by two plastic scintillators placed at the downstream of the device board, as shown in Fig. 4. To reduce background radiation events, the data acquisition system counted only the events for which the two signals from the two plastic scintillators were coincident. Also, a germanium detector was placed to monitor the muonic X-rays under the negative muon irradiation. The data of the muonic X-rays can provide additional information on the position where negative muons stopped in the device board.

Fig. 6 shows the temporal distribution of the coincident events measured by the two plastic scintillators in the case of irradiation of 38 MeV/c negative and positive muons. Both the counts decrease exponentially with time. The mean lifetime of positive muons is 2.2 μs, while that of negative muons is 1.7 μs and smaller than that of positive muons because

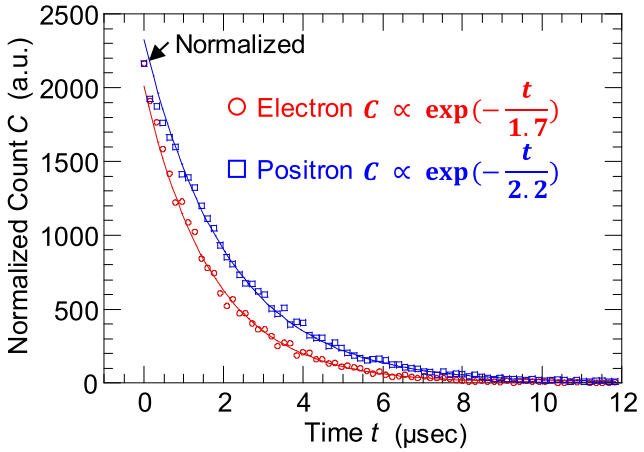

Fig. 6. Normalized number of coincident events of two plastic scintillators as a function of time.

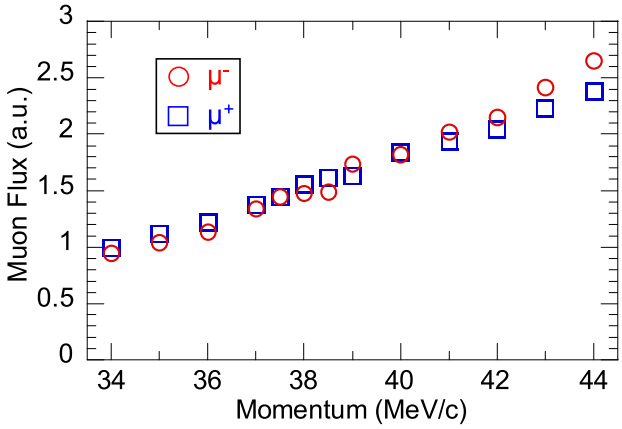

Fig. 7. Relative muon flux per proton beam pulse determined from the total coincidence count of decay electrons/positrons. The statistical errors for each measurement are below 3%.

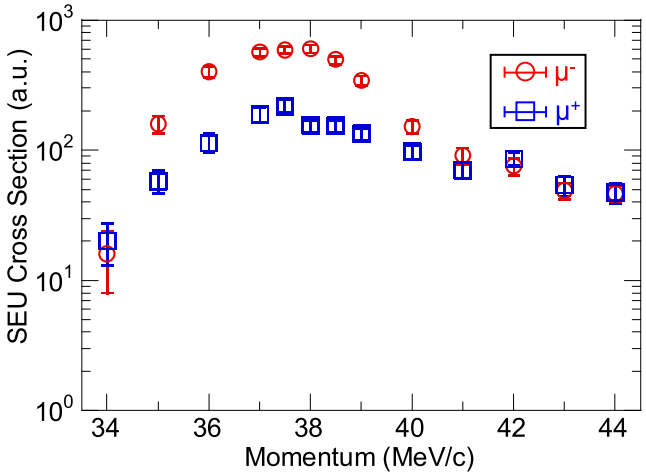

Fig. 8. Measured cross sections of SEUs induced by negative and positive muons as a function of momentum.

a certain fraction of negative muons are captured by nuclei. Here, the mean lifetime is defined by the time for the number of muons to reduce to 1/e of the initial number. To determine the mean lifetime by curve fitting of the measured temporal distribution, the coincident events were counted over enough longer time compared to the mean lifetime of the muons.

All SRAMs were initialized by writing the data "0" before each irradiation run. After irradiation, the number of bit errors was counted. The SEU cross section can be derived by dividing the number of the observed bit errors by the incident muon fluence which is defined by the product of flux and irradiation time. The flux per proton beam pulse was determined from the total coincidence counts of decay electrons/positrons which were obtained by integration of the coincidence counts over time in Fig. 6 and was corrected by the solid angle subtended by the scintillator detector. Some of the stopped negative muons are captured by nuclei and the electron is not emitted. The capture rate of negative muons depends on constituent elements in their stopping position. The device board contains a variety of elements such as silicon, carbon, oxygen, and copper. Therefore, it is difficult to know accurately the capture rate of negative muons in the stopping position if details of the structural components are not available. In the present irradiation experiment, thus, we measured the flux of incident negative and positive muons per proton pulse by placing a pure aluminum plate instead of the device board. The capture rate R_c of negative muons in aluminum was assumed to be 59% based on the experimental values [17]. The number of detected decay electrons divided by the decay rate ($=1 - R_c$) was used to determine the negative muon flux. Fig. 7 shows the measured muon flux per proton beam pulse. The positive and negative muon fluxes are almost the same in magnitude and increase monotonically with increasing momentum.

IV. Experimental Results and Discussion

A. Background Run

Prior to muon irradiation, the error bits of chips were checked without the muon beam to estimate background events. No error bit was observed at operating supply voltages from 0.25 to 1.1 V. Background runs with an aluminum plate placed in the entrance of the collimator were also conducted under some conditions with different muon momenta and operating voltages. In these cases, the incident muons stopped completely in the aluminum plate and radiation other than muons (decay electrons and positrons, neutrons, γ-rays, etc.) bombarded the device board. However, no SEU occurred by these radiations. Moreover, during muon irradiation on the device board, no SEU was observed in four chips placed behind the lead blocks shown in Fig. 5. Thus, it was confirmed that any background noises did not affect the results of SEU measurements mentioned below.

B. Momentum Dependence

The irradiation tests with negative and positive muons were performed in the momentum range from 34 to 44 MeV/c. All SRAMs were operated at a supply voltage of 0.5 V during the tests. The measured SEU cross sections are plotted as a function of momentum in Fig. 8. The error bars show the statistical uncertainties.

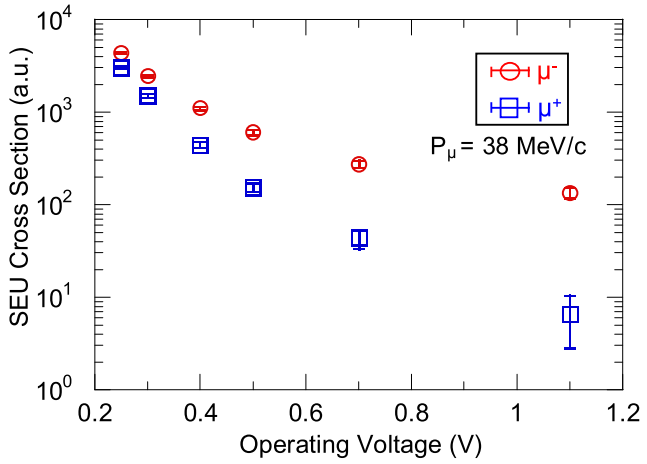

Fig. 9. Supply voltage dependence of measured SEU cross sections at the incident muon momentum of 38 MeV/c.

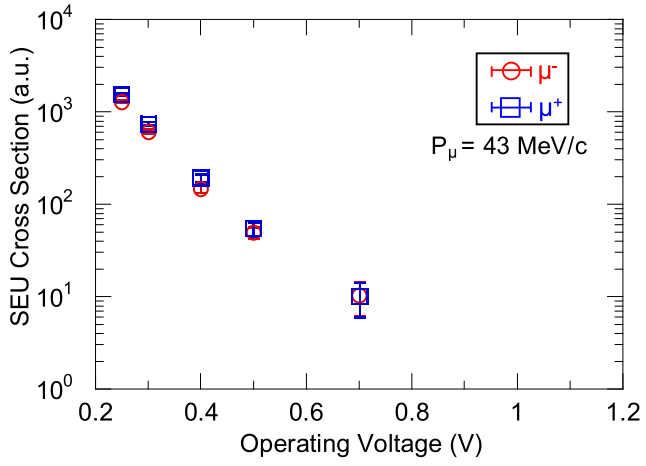

Fig. 10. Supply voltage dependence of measured SEU cross sections at the incident muon momentum of 43 MeV/c.

Both the negative and positive muon SEU cross sections have the peaks around 38 MeV/c, as shown in Fig. 8. Our simulation with PHITS [15] shows that the 38-MeV/c muon can stop in the vicinity of the SV as described later in Section V. This suggests that the muon deposits the maximum charge in the region localized at the end of its path and the deposited charge leads to the high probability of SEU occurrence. It should be noted that the peak momentum of 38 MeV/c depends on the experimental conditions that determine the range of incident muons in the SRAM chip, i.e., the geometry and composition of chip and device board.

Next, it is found that the negative muon SEU cross sections are approximately 2–4 times larger than the positive muon SEU ones in the momentum range from 35 to 39 MeV/c. From this result, the secondary ions generated during the negative muon capture process are expected to dominate SEU rates compared to SEU induced by direct ionization. As the muon momentum is higher than 40 MeV/c, the difference between both muons in the SEU cross section is smaller and smaller, and both are almost the same over 42 MeV/c. Most of the muons with momentum over 42 MeV/c pass through the device board, and negative muon capture reaction seldom happens near the SV. The direct ionization contributes mainly to the occurrence of SEUs. Therefore, the difference between the positive and negative muon SEU cross sections is approximately equivalent to the contribution from secondary heavy and light ions generated by negative muon capture reactions in the device.

C. Supply Voltage Dependence

Fig. 9 shows a comparison of the SEU cross sections between negative and positive 38-MeV/c muons as a function of operating supply voltage. Both the SEU cross sections decrease with increasing supply voltage. However, the negative muon SEU cross section is significantly larger than the positive muon one at higher supply voltage above 0.4 V. At higher supply voltage (i.e., at larger critical charge Q_c), therefore, negative muon SEU is expected to occur more frequently than positive muon SEU due to the larger amount of charge deposited by negative muons. This experimental result can be understood from consideration that the charge deposited by the secondary ions generated from the negative muon capture is much larger than that deposited by muon direct ionization.

A similar comparison is presented in Fig. 10 for muons with higher momentum of 43 MeV/c, which can pass through the device board. As mentioned in the preceding Section IV-B, the direct ionization is expected to provide predominant influence on the occurrence of SEU mainly at 43 MeV/c. Therefore, it is reasonable that the negative and positive muon SEU cross sections are almost the same over a wide range of supply voltage in this case.

D. Comparison With Previous Works

As mentioned in Section I, there are some experimental results of positive muon SEU cross sections [7]–[11]. The present result of the momentum dependence of SEU cross sections is qualitatively similar to the previous results. The SEU cross sections show the maximum value at a certain incident momentum (energy), although the momentum (energy) depends on the experimental conditions, i.e., the structure of devices under test, with/without package, and so on. Moreover, the strong supply voltage dependence shown in Figs. 9 and 10 is similar to the results in [7] and [9].

With respect to negative muon SEUs, only the numerical simulation result of Serre *et al.* [12] is available for 65-nm Bulk SRAMs. [12, Fig. 5] can be compared with Fig. 8 in the present result. The former provides the SEU cross sections in the kinetic energy range from 0.1 to 0.9 MeV, while the momentum range in the present measurement (i.e., 34–44 MeV/c) corresponds to the kinetic energy range from 5.3 to 8.8 MeV. The difference of the kinetic energy range is due to that of the SRAM structure which determines the relation of muon kinetic energy and range in the chip. Both results have the peaks near the momentum or the kinetic energy where the muons stop completely in the vicinity of the SV. However, the experimental peak is much broader than that of the simulation, because mono-energetic muons were assumed in the simulation and the muon beam having a

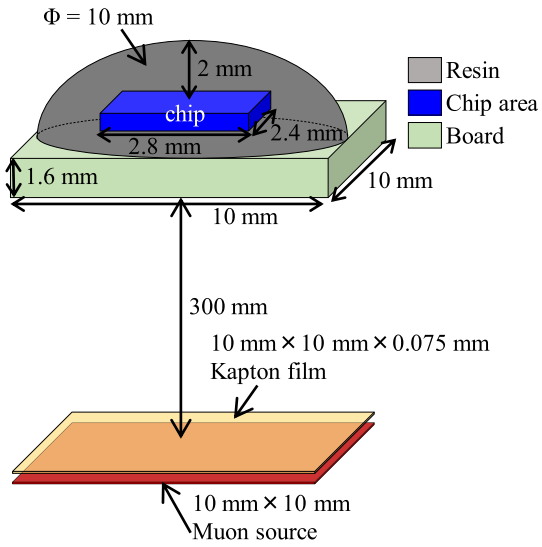

Fig. 11. Configuration of the test device used in PHITS simulation.

normal momentum distribution were used in the experiment. The simulation also shows the relative fraction of muon capture and direct ionization in SEUs separately. In the low kinetic energy range including the maximum peak, the muon capture is a dominant process to cause SEUs. As the kinetic energy increases, the direct ionization process becomes more dominant in SEU than the capture process. Our observation of negative muon SEUs supports the simulation result of Serre *et al.* [12] qualitatively.

V. Simulation

A. Method

The experimental data are analyzed based on the SV model [16] using the Monte-Carlo simulation with PHITS versus 2.95 [15]. PHITS has been successfully used in recent simulations of neutron-induced soft errors [22]–[26]. More recently, well-established muon interaction models have been implemented in PHITS [18] and the transport of muons in matter including negative muon capture reaction can be predicted with high accuracy. In addition, the generation of delta rays, i.e., secondary electrons with enough energy, can be taken into account. As a result, the energy deposition by the delta rays spread far away from the muon path. In PHITS, the generation of delta rays with the kinetic energy over 1 keV is simulated using the model proposed by Butts and Katz [27]. In this paper, the transport of muons and the deposited energy in the SV are simulated by PHITS. The occurrences of SEUs are judged using the SV model, in which SEU is assumed to occur when the total charge deposited in the defined SV exceeds the critical charge Q_c.

Fig. 11 illustrates the configuration of the test device used in PHITS simulation. A single chip is used in the simulation as a mock-up for the device board. The chip covered with the resin is placed on the board layer. The planar muon source having 10 mm × 10 mm area is placed in air 300 mm away from the board layer. The muons enter the test device vertically via a 75-μm-thick kapton film located in the beam exit. The momentum of the incident muon is determined by sampling

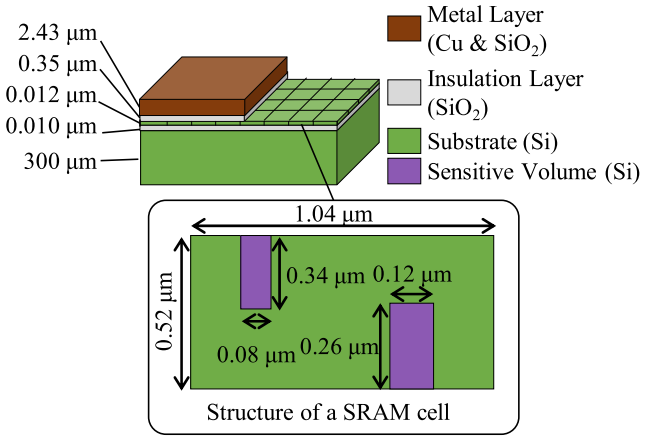

Fig. 12. Configuration of the chip used in PHITS simulation. 12-Mbit SOTB SRAMs are placed on a chip. Thickness of the SV is 0.012 and 0.010 μm insulation layer is placed just under the SV.

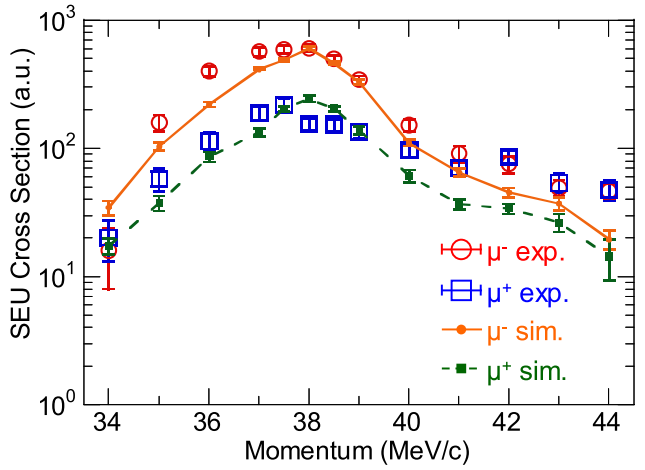

Fig. 13. Comparison between the simulated momentum dependence and the measured one.

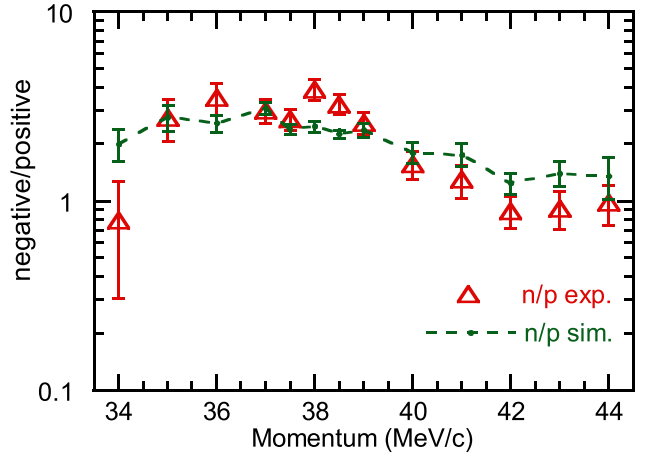

Fig. 14. Ratio of negative muon SEU cross sections to positive muon ones as a function of incident momentum.

using a normal distribution with 5% standard deviation to reproduce the muon beam of the MUSE facility.

The inner structure of the chip is depicted schematically in Fig. 12. The area size of the chip is 2800 μm × 2400 μm. It consists of 12-Mbits SOTB SRAM cells. A single SRAM

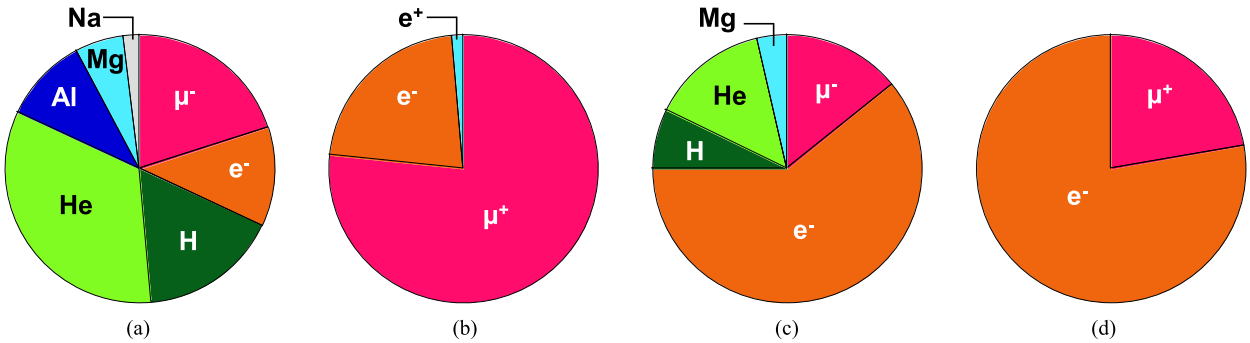

Fig. 15. Contribution of individual charged particles and secondary ions to negative and positive muon-induced SEUs. (a) 38 MeV/c negative muon. (b) 38 MeV/c positive muon. (c) 43 MeV/c negative muon. (d) 43 MeV/c positive muon.

memory cell has a size of 1.04 μm $\times$ 0.52 μm $\times$ 0.012 μm, and a total of 12-Mbit cells are configured in 2-D grid on a 0.010-μm-thick silicon dioxide insulation layer. A 300-μm-thick silicon substrate is located under a 0.010-μm-thick silicon dioxide insulation layer. A 0.35-μm-thick silicon dioxide insulation layer is placed above the SRAM memory cells and a 2.43-μm-thick metal layer consisting of copper and silicon dioxide is above a 0.35-μm-thick silicon dioxide insulation layer. With reference to the previous work [22], [23], the SV of the SRAM memory cell is defined as the source and drain regions, and SOI layer under the gate of the OFF-state nMOS and pMOS. The SV size is 0.34 μm $\times$ 0.08 μm and 0.26 μm $\times$ 0.12 μm for nMOS and pMOS areas, respectively. The thickness of both SVs is 0.012 μm, which is equal to that of the SOI layer.

B. Simulation Results and Discussion

In Fig. 13, the simulated momentum dependence of SEU cross sections is compared with the experimental result. The critical charge Q_c in the simulation was chosen as 0.08 fC so as to reproduce the ratio of the negative and positive muon-induced SEU cross sections at 38 MeV/c. The orange-full and green-dashed lines denote the simulated negative and positive muon SEU cross sections, respectively. Note that the simulated negative muon SEU cross section at 38 MeV/c is normalized to the measured one. At first glance, the overall behavior of the SEU cross section is reproduced generally well by the PHITS-SV simulation. Fig. 14 shows the ratio of negative muon SEU cross sections and positive muon ones. The experimental ratio is reproduced reasonably well by the present simulation, except at 34 MeV/c where the experimental statistics is poor.

Next, we have examined the species of charged particles and secondary ions which influence low-energy muon-induced SEUs using the present PHITS-SV simulation. Fig. 15 shows the results at two typical incident momenta, 38 and 43 MeV/c. It should be noted that the contribution of electrons includes both the decay electrons and delta rays in the negative muon incidence, while only the delta rays are the source of electrons in the positive muon incidence. Some obvious differences between negative and positive muons are seen in the charged particles and secondary ions influencing on SEUs.

As shown in Fig. 15(a), the direct ionization of negative muons contributes to SEUs by about 20%, while about 70% of the SEUs are caused by secondary charged particles and heavy recoils generated by the negative muon capture reaction at 38 MeV/c where the incident muons stop near the SV of the SRAM. Especially, the helium ion has the predominant contribution among all particle and ion species. On the other hand, the direct ionization is predominant in the positive muon incidence as shown in Fig. 15(b), and the influence of decay positrons is negligibly small. This suggests that the contribution of electrons in the negative muon incidence comes mainly from delta rays, but not from decay electrons.

In Fig. 15(c) and (d), it is shown that electrons contribute dominantly to SEUs induced by both negative and positive muons at 43 MeV/c, where the muons pass through the SV of the SRAM. Also, the electrons are expected to be the delta rays in both the cases, because the effect of decay positrons is negligible in the positive muon incidence. In addition, the relative contribution of secondary ions and heavy recoils in the negative muon incidence is much lower than that at 38 MeV/c. This is consistent with the experimental result that the measured negative and positive muon SEU cross sections are almost the same at incident momenta higher than 41 MeV/c. From these analyses, it is found that the delta rays contribute predominantly to SEUs when muons pass through the SV of the SRAM. If the generation of delta rays is neglected in the PHITS-SV simulation, the calculated SEU cross sections become much smaller at high momenta than the result of Fig. 13 and cannot reproduce the measured momentum dependence. This suggests that it is important to take into account the generation of delta rays in the SEU simulation, especially in the device with low Q_c.

Thus, the PHITS-SV simulation with $Q_c = 0.08$ fC was found to reproduce well the momentum dependence of measured muon-induced SEU cross sections, as shown in Fig. 13. The Q_c value was estimated by fitting the PHITS simulation to the experimental ratio of the negative and positive muon SEU cross sections at 38 MeV/c. Hence, the Q_c value depends on the accuracy of the physics models implemented in PHITS and the SV assumption in the simulation. Besides, the Q_c value is considerably low compared to the general Q_c trend of 65-nm technology SRAMs. In the present simulation, we have approximated the charge collection process by the simple SV model and have not simulated it accurately after the initial charge deposition. The previous work on SOI devices pointed out the importance of parasitic bipolar effects leading

to the enhancement of charge collection at the drain [28]. Therefore, device simulation will be necessary for further detailed discussion.

VI. Conclusion

We have measured the momentum and supply voltage dependences of SEUs induced by both negative and positive muons on 65-nm SOTB SRAMs in the momentum range of 34–44 MeV/c. It should be emphasized that the accelerated SEU test using negative muons was performed with high statistics by means of the intense and high-quality negative muon beam at the J-PARC MUSE facility.

The experimental results showed that the negative muon SEU cross sections are 2 to 4 times larger than the positive muon ones in the case where the muons stop in the SRAM chips, and both the SEU cross sections have the peak around 38 MeV/c. The difference seen at 38 MeV/c was found to become large with increasing supply voltage. On the other hand, the negative and positive muon SEU cross sections were almost the same, regardless of the supply voltage, at incident momenta over 42 MeV/c where the fraction of muons passing through the device becomes large.

To analyze these experimental results, the Monte-Carlo simulation with PHITS was carried out using the simple SV model. The simulation showed a generally good agreement with the momentum dependence of the measured SEU cross sections for both the positive and negative muons. In addition, we examined the species of charged particles and secondary ions which influence low-energy muon-induced SEUs. From these simulation results, it was clarified that the negative muon capture by constituent atoms in the device causes SEUs considerably. Moreover, it was found that the delta rays generated along the muon path have impact on the occurrence of SEUs.

As a next step, we plan to perform charge collection simulation with device simulators instead of the SV model for further understanding of the SEU mechanism induced by muons. New irradiation test data of positive and negative muons on 65-nm Bulk SRAMs are also available [29]. In the future, we will compare the experimental results of SOTB and Bulk SRAMs and investigate how the difference of device structure influences the SEU mechanism caused by low-energy muons.

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