Hold Violation Analysis for Functional Test of Ultra-Low Temperature Circuits at Room Temperature

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***Abstract*—VLSIs that perform signal processing near infrared sensors cooled to ultra-low temperature are demanded. Delay test of those chips must be executed at ultra-low temperature while functional test could be performed at room temperature as long as hold timing errors do not occur. In this paper, we focus on the hold timing violation and evaluate the feasibility of functional test of ultra-low temperature circuits at room temperature. Experimental evaluation with a case study shows that the functional test at room temperature is possible.**

I. Introduction

Infrared sensors equipped with satellites are classified into cooled and uncooled ones, and some cooled sensors operate at -200 degrees Celsius. With an increase in the number pixels of sensors, signal processing adjacent to the sensors is demanded, which means VLSIs operating at such a low temperature need to be designed and tested.

Generally, as the operating temperature falls, the signal switching and propagation in a chip become faster because the electron mobility becomes higher and the wiring resistance becomes lower. With a wide range of temperature variation, timing errors might occur due to a significant speed variation. Therefore, digital circuits are designed with a library which contains timing characteristics at the ultra-low temperature. Also, after fabrication, the circuit is tested at ultra-low temperature. Here, there are two types of tests; one is functional test, and the other is delay test. The delay test for timing verification must be performed at ultra-low temperature while the functional test, which is followed by the delay test, could be performed at any temperature as long as hold timing errors do not occur because the functionality of digital circuits is independent of temperature. For saving the test cost, this work evaluates the feasibility of the functional test at room temperature. We experimentally evaluate the probability of hold timing violation at room temperature in the circuits designed for ultra-low temperature operation. Also, we discuss the dependency of hold violation probability on the supply voltage.

The rest of this paper is organized as follows. Section II explains the impact of temperature on transistor and wire characteristics. Section III explains the calculation of hold violation probability under process variation. Section IV describes the procedure and setup of experiments with two design examples, and Section V shows the experimental results and discusses whether functional test at room temperature is possible. Finally, concluding remarks are given in Section VI.

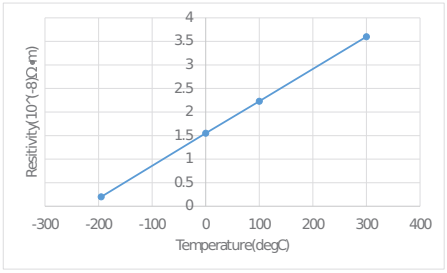

Fig. 1. Temperature dependency of the volume resistivity of copper

II. Impact of Temperature on Device Characteristics

This section reviews the temperature dependency of transistor performance, interconnect resistance and delay time. This paper assumes that the interconnects are made of pure copper.

A. Temperature dependency of transistors

The drain current of an NMOS transistor I_d is expressed by[1], where C_{OX} is capacitance / (thickness of gate oxide), L is channel-length, W is channel-width, μ is electron mobiliby, V_G is gate voltage, V_{th} is threshold voltage and V_D is drain voltage.

$$I_d = C_{OX}\frac{W}{L}\mu(V_G - V_{th} - \frac{1}{2}V_D)V_D \quad (1)$$

V_{th} and μ increase as the temperature decreases [2]. References [3] and [4] report that the temperature dependency of threshold voltage and electron mobility are unchanged even at ultra-low temperature.

B. Temperature dependency of interconnects

Reference [5] indicates that the volume resistivity of copper varies in almost proportion to temperature as shown in Fig. 1, and shows that the resistivity at -195 degree C is about 8 times lower than that at 0 degree C. Lower wiring resistance results in smaller wiring delay [6].

C. Temperature dependency of delay

Gate delay T_g is expressed by[2], where C_{out} is output load capacitance, and V_{dd} is supply voltage.

$$T_g \propto \frac{C_{out}V_{dd}}{I_d} = \frac{C_{out}V_{dd}}{\mu(T)(V_{dd} - V_{th}(T))^{\alpha}} \quad (2)$$

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As mentioned above, threshold voltage and electron mobility increase as temperature drops. On the other hand, Eq. (2) indicates that these parameters have opposite impacts on gate delay. When supply voltage is high, the denominator of $(V_{dd}-V_{th}(T))$ is large, and hence the temperature dependency of $V_{th}(T)$ has a smaller impact on gate delay. In this case, $\mu(T)$ has a relatively larger impact on gate delay. Conversely, when supply voltage is low, the temperature dependency of $V_{th}(T)$ is dominant. With these two impacts, we observe the following two tendencies; (1) when supply voltage is low, gate delay becomes larger at a lower temperature, and (2) when supply voltage is high, gate delay becomes smaller at a lower temperature. This behavior is called inverted temperature dependence (ITD) [2]. To include ITD in the evaluation, we will evaluate hold violation probability at various supply voltages.

Next, we examine the delay including gate and interconnect T_{gw}, which is expressed by [6], where R_{tr} is output resistance of the driver gate, C_p is parasitic drain capacitance, C_L is input capacitance of the receiver gate, c is wire capacitance per unit length, r is wire resistance per unit length and l wire length.

$$T_{gw} = R_{tr}(C_p + C_L) + (R_{tr}c + rC_L)l + \frac{1}{2}rcl^2 \tag{3}$$

The wire resistance becomes smaller as temperature becomes lower. Supposing R_{tr}, C_p and C_L are temperature independent for simplicity, T_{gw} decreases as temperature lowers, but the amount of delay decrease depends on the wire length l. This dependency on length may unbalance the impact of temperature on clock path and data path.

III. Hold violation probability

A. Hold violation

Timing violation may occur due to temperature variation. Setup timing violation can be solved in functional test by increasing clock cycle or supply voltage. On the other hand, hold timing violation cannot be resolved during the test without redesign. This work focuses on hold timing violation and discusses how frequently hold violation occurs at room temperature since functional test can be performed as long as no hold violations occur.

In digital circuits, clock signal is supplied to flip-flops (FFs) through a clock distribution network. Because of the difference in interconnect length and non-uniform FF placement across the chip, the clock signal is delivered to FFs not simultaneously but with a time lag, which is called clock skew. The clock skew varies depending on temperature since interconnect delay and clock driver delay change. As the clock skew becomes large and the clock arrives at the launch FF earlier than at the capture FF, a hold timing violation occurs. In addition to temperature change, process variations affect timing stochastically, and hence the hold violation occurrence depends on individual fabricated chips. Therefore, this work performs a statistical analysis of hold timing violation and calculates hold violation probability under process variations.

B. Calculation of hold violation probaiblity

This section explains how to calculate hold violation probability considering process variations. In this paper, we take into account intra-chip random variation, which fluctuates physical parameters of individual devices randomly. Evaluation with inter-chip variation is a future work. As representative fluctuating physical parameters, gate length l and NMOS and PMOS threshold voltages v_{thn} and v_{thp} are considered in this work.

First, we consider path-wise hold violation probability. As the path delay becomes smaller, the hold slack at the capture FF becomes smaller. When the amount of slack reduction becomes larger than the slack with no process variation $Slack_i$, hold violation occurs. Hence, the hold violation probability $V_{path,i}$ can be calculated by

$$V_{path,i} = \int_{-\infty}^{-Slack_i} f_i(x) \cdot dx, \tag{4}$$

where $f_i(x)$ expresses the probability density function of random variable x and it corresponds to delay variation of path i.

Second, V_{whole}, which is the hold violation probability of the whole circuit consisting of n paths, is represented by

$$V_{whole} = 1 - \prod_{i=1}^{n}(1 - V_{path,i}), \tag{5}$$

where correlation between $V_{path,i}$ and $V_{path,j}$ are not considered.

From now, we will derive probability density function $f_i(x)$ of path delay variation since $f_i(x)$ is necessary to compute $V_{path,i}$ in Eq. (4). Let us denote gate delay variation of logic gate j as ΔDg_j, and variations of gate length and NMOS and PMOS threshold voltages from the corresponding average values as Δl, $\Delta vthn$ and $\Delta vthp$, respectively. When Δl, $\Delta vthn$ and $\Delta vthp$ are small, $\Delta D_{gate,j}$ can be expressed as follows using the first-order sensitivities $S_{l,j}$, $S_{vthn,j}$ and $S_{vthp,j}$.

$$\Delta Dg_j = S_{l,j} \cdot \Delta l + S_{vthn,j} \cdot \Delta vthn + S_{vthp,j} \cdot \Delta vthp. \tag{6}$$

The sensitivities can be obtained with the following equations.

$$S_{l,j} = (Dg_{l,j} - D_j)/\Delta l \tag{7}$$

$$S_{vthn,j} = (Dg_{vthn,j} - D_j)/\Delta vthn \tag{8}$$

$$S_{vthp,j} = (Dg_{vthp,j} - D_j)/\Delta vthp \tag{9}$$

Here, D_j is the gate delay without process variations, and $Dg_{l,j}$, $Dg_{vthn,j}$, $Dg_{vthp,j}$ are the gate delays when the corresponding parameters are varied by Δl, $\Delta vthn$ and $\Delta vthp$, respectively. Using a timing analysis tool, we can obtain these values and consequently calculate $S_{l,j}$, $S_{vthn,j}$ and $S_{vthp,j}$. Letting σ_l, σ_{vthn} and σ_{vthp} denote the standard deviations of Δl, $\Delta vthn$ and $\Delta vthp$ and be uncorrelated, the standard deviation of gate delay variation σ_{gate_j} is expressed by

$$\sigma_{gate_j} = \sqrt{{\sigma_{Dg_{l_j}}}^2 + {\sigma_{Dg_{vthn_j}}}^2 + {\sigma_{Dg_{vthp_j}}}^2}.$$

$\sigma_{Dg_{l_j}}$, $\sigma_{Dg_{vthn_j}}$ and $\sigma_{Dg_{vthp_j}}$ are given by

$$\sigma_{Dg_{l_j}} = S_{l_j} \cdot \sigma_l, \quad (10)$$

$$\sigma_{Dg_{vthn_j}} = S_{vthn_j} \cdot \sigma_{vthn}, \quad (11)$$

$$\sigma_{Dg_{vthp_j}} = S_{vthp_j} \cdot \sigma_{vthp}. \quad (12)$$

When Δl, $\Delta vthn$ and $\Delta vthp$ follow normal distributions, the averages of them are 0 from the definitions and hence the average of gate delay variation in Eq. (6) is 0.

The path delay is the sum of gate delays in the path, and hence the delay variance of path i, $\sigma^2_{path_i}$, is expressed by the sum of delay variances of the gates included in path i, i.e.,

$$\sigma^2_{path_i} = \sum_{i=1}^{m} {\sigma_{gate_j}}^2. \quad (13)$$

The average of the path delay variation is also 0 since the averages of the gate delay variation is 0. From the above discussion, we can use the probability density function of a normal distribution whose average is 0 and standard deviation is σ_{path_i}, as $f_i(x)$. Then, we can calculate Eq. (4) and consequently obtain hold violation probability V_{whole} in Eq. (5).

IV. Experiment Procedure

The computation of hold violation probability discussed in the previous section needs $Slack_i$, $S_{l,j}$, $S_{vthn,j}$ and $S_{vthp,j}$. These must be obtained using a static timing analysis tool with timing libraries that cover process variations and a wide range of temperature variation. The first step of the experiment is the preparation of timing libraries that cover process variations at various temperatures. Next, we prepare design examples and calculate hold violation probabilities with the prepared libraries. The experiment procedure can be listed as follows.

1) Timing library preparation
   - Obtain I-V transistor characteristics at various temperatures
   - Generate transistor models for SPICE via fitting
   - Characterize cell delay characteristics
2) Hold probability calculation for design examples
   - Design example circuits dedicated for ultra-low temperature operation
   - Calculate hold violation probability at room temperature

Followings explain each item in the procedure.

A. Obtain I-V transistor characteristics at various temperatures

In timing library preparation, circuit simulation is indispensable. However, transistor models that guarantee ultra-low temperature operation are not generally provided. In this work, we decided to generate transistor models for each temperature based on TCAD simulation results for a 65nm process transistors. We carried out TCAD simulations to obtain V_g (gate voltage) - I_d (drain current) characteristics and V_d (drain voltage) - I_d characteristics at various combinations of temperature and supply voltage. Correlation analysis between TCAD simulation and hardware measurement is one of the future works.

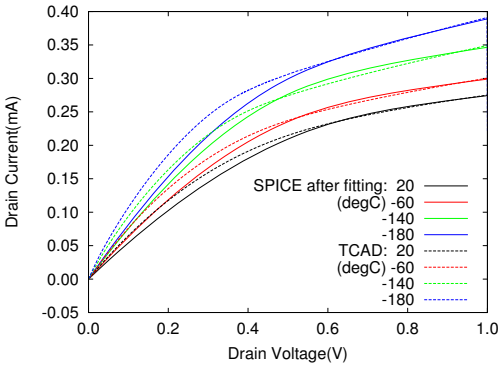

Fig. 2. Fitting results of NMOS $V_d - I_d$ characteristics.

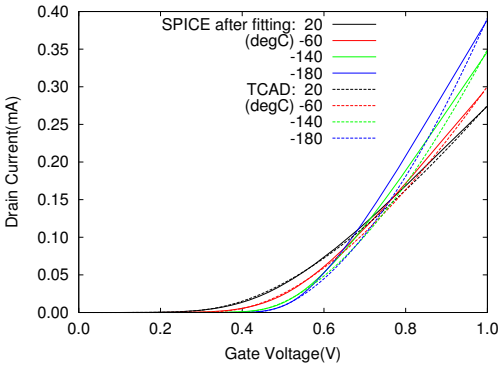

Fig. 3. Fitting results of NMOS $V_g - I_d$ characteristics.

B. Generate transistor models for SPICE via fitting

The next step is to generate transistor models for circuit simulation. We fit the I-V characteristics of SPICE simulation to the TCAD simulation results prepared in the previous subsection with three fitting parameters of "delvto," "mulu0" and "eta." Here, delvto represents the threshold voltage, mulu0 is the electron mobility, and eta is the DIBL coefficient. The fitting is performed for each combination of temperature and supply voltage. The evaluated temperatures are -180, -140, -100, -60, -20, 20, 60 and 100 degree Celsius and supply voltages are 0.6, 0.8 and 1.0 V.

Figs. 2 and 3 show the fitting results for NMOS transistor at supply voltage of 1.0V, where the dotted lines are TCAD simulation results and the solid lines are SPICE simulation results after the fitting. The TCAD and SPICE simulation results at the same temperature are drawn with the same color. We can see that the solid and dotted lines are well correlated. On the other hand, at low temperatures, we observe some discrepancy in the transitional region between linear and saturation regions. Here, for delay characteristics, the most critical region is the saturation region and the fitting works well in this region. We think that the generated SPICE models can be used for timing analysis in the following steps.

C. Characterize cell delay characteristics

We characterize standard cells with the SPICE transistor models generated in Section IV-B and prepare library files containing the delay characteristics of each cell for each combination of temperature and supply voltage. Moreover,

to analyze delay fluctuation due to process variations and obtain the sensitivities, for each combination, we also prepare three library files that correspond to the cases in which the NMOS and PMOS threshold voltages increase by 1mV and the channel length increases by 0.1nm individually.

D. Design example circuit dedicated for ultra-low temperature operation

As evaluation circuits, we designed circuits supposing ultra-low temperature operation at various supply voltages. The designed circuits are AES (Advanced Encryption Standard) circuits. We performed logic synthesis, cell placement, clock tree synthesis and routing with the library at -180 degree Celsius. The designed circuits do not have any timing violations. Note that the wire resistivity in the library is also varied depending on the temperature.

E. Calculate hold violation probability at room temperature

We finally calculate the hold violation probability V_{whole} derived in Section III-B. We change the library file and the wiring resistivity according to the temperature and supply voltage of interest and then perform timing analysis. The sensitivities in Eqs. (10) to (12) are computed from $Dg_{l,j}$, $Dg_{vthn,j}$ and $Dg_{vthp,j}$, which are obtained by timing analysis results with the library files having small variations of l, $vthp$ and $vthn$. On the other hand, calculating the hold violation probability for all the paths in the circuit is difficult in terms of computational complexity. Therefore, in this paper, five shortest paths are selected for each capture FF and analyzed. In the analysis, we assume the standard deviations of the NMOS and PMOS threshold voltage variations and channel length variation are 30 mV, 30 mV and 1 nm, respectively.

V. Experimental results

Fig. 4 shows the hold violation probabilities of the AES circuit designed at various supply voltages for ultra-low temperature operation. The vertical axis represents the hold violation probability. However, the probabilities less than 1e-09 % is not displayed since it is not possible to guarantee calculation accuracy. The horizontal axis represents the temperature at which the hold violation probability is calculated. We can see that the hold violation probability increases at low supply voltage. At lower supply voltage, the overdrive voltage, which is the difference between the supply voltage and the threshold voltage, becomes smaller, the sensitivity to the path delay becomes higher, and then the circuit becomes more likely to have hold violation. Also, the hold violation probability increases at low temperature. As Section II discussed, the threshold voltage of transistors rises at low temperature, which also decreases the overdrive voltage and the sensitivity to the path delay increases. As a result, the hold violation probability at low voltage and low temperature is unacceptably high. This suggests that careful hold analysis for process variations is necessary to design circuits for ultra-low temperature operation.

From the opposite point of view, the low temperature is more severe condition for hold violation regardless of the supply voltage. Therefore when we design circuits in which hold violations do not occur at ultra-low temperature, it is highly probable that hold violation will not occur at room temperature and we can perform function tests at room temperature.

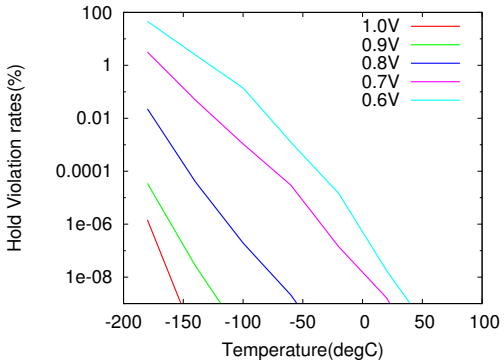

Fig. 4. Evaluated hold violation probability.

VI. Conclusion

In this paper, we designed evaluation circuits dedicated for ultra-low temperature operation, analyzed timing characteristics with temperature variation, and calculated hold violation probability to investigate whether functional tests of the ultra-low temperature circuits can be performed at room temperature. Experimental results show that the hold violation probability decreases as the temperature rises, and hence we conclude that the functionality of the ultra-low temperature circuits is highly probable to be tested at room temperature. Moreover, the experimental result suggests that ultra-low temperature circuits need to be designed with larger hold margin than usual since threshold voltage elevation due to temperature decrease increases hold violation probability.

Evaluation of other circuits is a future work. Also, hold violation analysis that takes into account not only intra-chip random variation but also inter-chip is also included in our future work.

Acknowledgment

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