Contributions of SRAM, FF and Combinational Circuit to Chip-Level Neutron-Induced Soft Error Rate
– Bulk vs. FD-SOI at 0.5 and 1.0V –

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***Abstract*—Soft error jeopardizes the reliability of semiconductor devices, especially those working at low voltage. In recent years, silicon-on-thin-box (SOTB), which is a FD-SOI device, is drawing attention since it is suitable for ultra-low-voltage operation. This work evaluates the contributions of SRAM, FF and combinational circuit to chip-level soft error rate (SER) based on irradiation test results. For this evaluation, this work performed neutron irradiation test for characterizing single event transient (SET) rate of SOTB and bulk circuits at 0.5V. Combining previously reported SRAM and FF error rates with the measured SET rate, we estimated chip-level SER and each contributionto chip-level SER for embedded and high-performance processors. For both the processors, 99% errors occur at SRAM in both SOTB and bulk chips at 0.5 and 1.0V, and the overall chip-level SERs of the assumed SOTB chip at 0.5V is at least 10x lower than that of bulk chip. On the other hand, when ECC is applied to SRAM in the SOTB chip, MCUs occurring at SRAM are dominant in the embedded processor while SEUs at FFs are not negligible.**

I. Introduction

In recent decade, new transistor structures that are suitable for low voltage operation are shifted to mass production. Fully depleted silicon-on-insulator (FD-SOI) is one of those promising devices [1]. Although the device miniaturization makes soft error occur more easily [2], FD-SOI devices have better immunity to soft error than conventional bulk devices thanks to the insulator layer between the substrate and SOI layer [3], [4].

Silicon-on-thin-box (SOTB), which is a FD-SOI device with thinner BOX (buried oxide) and SOI layers of 10nm and 12nm, respectively, was proposed to improve controllability of ultra-low voltage (0.6V and below) operation [5]. For assessing the soft error immunity of SOTB device, Kobayashi $et\ al.$ measured the soft error rate (SER) of flip flop (FF) of bulk and SOTB circuits at the supply voltage between 0.6V to 1.2V [6]. Hirokawa $et\ al.$ measured single bit upset (SBU) and multiple cell upsets (MCU) in SOTB and bulk SRAM at 0.4V to 1.0V [7]. Furuta $et\ al.$ measured single event transient (SET) in SOTB and bulk circuits at 1.2V.

This paper evaluates the chip-level neutron-induced SER of SOTB and bulk circuits at 0.5V and 1.0V and investigates the contributions of SRAM, FF and combinational circuit to the chip-level SER. For achieving this, we fabricated SOTB and bulk test chips and measured SET rate of SOTB and bulk combinational circuits at 0.5V due to lack of SET rate at ultra low voltage. Combining the measured SET rate with previously reported SERs of FF and SRAM [6], [7], chip-level SER of processors designed with SOTB and bulk CMOS is calculated. We compare the composition of chip-level SER between embedded and high-performance processors with and without ECC.

The rest of this paper is organized as follows. Section II explains test chips for irradiation test and shows measurement results. Section III estimates chip-level SER of SOTB and bulk processors and discusses the contributions of SRAM, FF and combinational circuit to the chip-level SER of embedded and high-performance processors. Section IV concludes the discussion.

II. SET rate measurement

A. Test chip design for SET measurement

We designed and fabricated test chips to evaluate the number of SET occurrence in SOTB and bulk circuits. Fig. 1 shows a test group for SET measurement. There are 256 ring oscillators (ROs), and they are target circuits for SET. In the SET measurement mode, SEL1 is set to low voltage to stop oscillation. To make full use of the limited beam time and obtain larger number of SETs, we wanted to place as many target circuits as possible while preventing SET pulse diminishing due to pulse width shrinking. For this purpose, 9-stage inverter chain was selected as the target circuit. We simplified the measurement circuit to maximize the ratio of the target circuits so that it can only count the number of SET pulses.

An SET pulse occurred in a target circuit is given to an asynchronous 1-bit counter, where the 1-bit counter is triplicated and the output is voted for SEU masking. During irradiation experiment, the FF values are scanned out to know how many SETs occurred. Besides, even if the counters and frequency divider are triplicated, errors can accumulate in FFs during the test. For preventing such error accumulation, we periodically reset FFs in the counters and frequency divider.

The test chip includes 60 test groups, and then there are 138,240 inverters in a single test chip. The test chip was fabricated with 65nm SOTB and bulk technologies with eight metal layers from the same Graphic Data System (GDS) data. A major difference between SOTB and bulk devices is the existence of BOX layer under the channel region.

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TABLE I: Number of measured SETs.

	# of SETs	Irradiation time	# of inverters	SET rate
SOTB	0	12.9h	6,635,520	<0.06
Bulk	39	12.9h	2,211,840	7.02

We mounted 16 test chips on a board as shown in Fig. 2, and six boards, four of which include SOTB chips and two of which include bulk chips, were placed on the neutron beam track as shown in Fig. 3. A pattern generator and logic analyzer were used for generating the input signals and recording the output signals of the chips. In the irradiation test, 48 of 64 SOTB chips and 16 of 32 bulk CMOS chips were measured since some chips had poor connection to the logic analyzer and the chip outputs were not recorded. The supply voltage was set to 0.5V.

The neutron beam in Research Center for Nuclear Physics (RCNP) at Osaka University, whose spectrum is similar to that at the terrestrial environment, was irradiated to the test chips. The average flux density of neutrons was $2.46\times10^{9}\text{cm}^{-2}\text{h}^{-1}$. Reference [9] reported neutron flux of Tokyo City at sea-level is about $12\text{cm}^{-2}\text{h}^{-1}$, and hence the acceleration rate was 2.05×10^{8}. The test chips were irradiated in 12.9 hours in total with an incident angle of 90 degree.

B. Test result

During the irradiation test, 39 SETs were observed in 16 bulk chips while no SET in 48 SOTB chips. The number of SETs and its SER rate are listed in Table I. We calculated the maximum SET rate of SOTB by supposing that an error was observed in the irradiation experiment. The location of SET occurrences in the bulk chips was analyzed. The distribution of SET occurrence within test group is shown in Fig.4, and the distribution within chip is shown in Fig.5. We can see the SET occurrence is random in space as we expected.

C. Credibility of SET data

In this irradiation test, the number of SETs was small. For making sure the measured SETs are true SETs instead of pseudo SETs that are caused by SEUs in 1-bit counters, we estimated prospective count of the pseudo SETs. The 1-bit

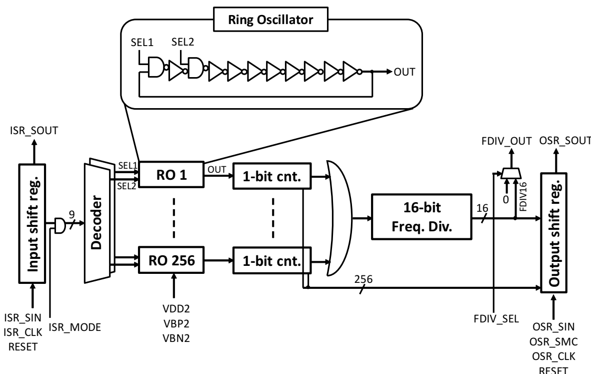

Fig. 1: One test group for SET measurement.

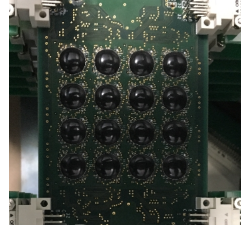

Fig. 2: Chip Board Used in Irradiation Test.

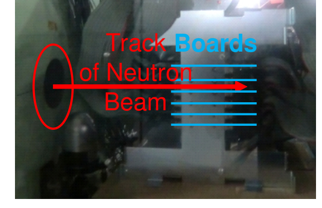

Fig. 3: Experiment Setup.

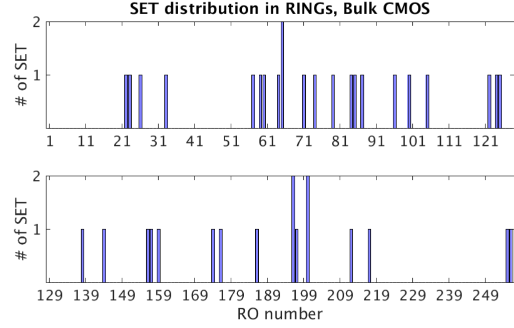

Fig. 4: Distribution of SET occurrence within test group. Each bar corresponds to a RO.

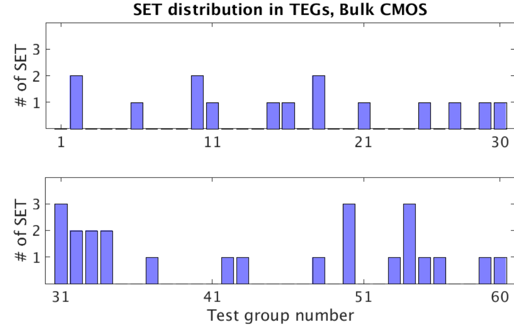

Fig. 5: Distribution of SET occurrence within chip. Each bar corresponds to a test group.

counter consists of 3 FFs and a voter. A pseudo SET occurs when two FFs have upset during the reset interval, and hence the probability of pseudo SET occurrence during reset interval T_{reset}, P_{pSET}, is expressed as

$$P_{pSET} = 3\cdot P_{FF}^2\cdot(1-P_{FF}) + 1\cdot P_{FF}^3, \tag{1}$$

where P_{FF} is the probability of SEU occurrence during T_{reset}, and it is expressed as the product of T_{reset} and SER_{FF}, SER of a FF.

Considering the total irradiation time T_{total} and the number of counters in the measured chips $N_{counter}$, the expected number of the pseudo SETs E_{pSET} is calculated as

$$E_{pSET} = P_{pSET}\times N_{counter}\times\frac{T_{total}}{T_{reset}}. \tag{2}$$

In our irradiation experiment, N_{count} was 24,576, and T_{reset} was 3 hours. Using the SER_{FF}, which will be explained in

TABLE II: SER data for SOTB circuits.

Voltage [V]	0.4	0.5	0.6	0.8	1.0	1.2
SET [FIT/Mbit]		(0.06)			(0.06)	
SBU [FIT/Mbit]	650	(508)			147	
MCU [FIT/Mbit]	2.8	(2.3)			0.8	
FF [FIT/Mbit]	29.5	(26.8)	26.2	16.2	(14.0)	11.0

TABLE III: SER data for bulk circuits.

Voltage [V]	0.4	0.5	0.6	0.8	1.0	1.2
SET [FIT/Mbit]		7.02			(7.02)	
SBU [FIT/Mbit]	8250	(6490)			1950	
MCU [FIT/Mbit]	404	(385)			303	
FF [FIT/Mbit]		(1400)	1150	650	620	360

the next section, the expected number of pseudo SET was 2.1. The pseudo SETs were expected to be 5% of the measured SETs. Therefore, we conclude that the measured SETs can be treated as true SETs in the following analysis.

III. Discussion on chip-level SER

A. Data preparation

For estimating chip-level SER, this section prepares necessary SER data. The SRAM SER in the same SOTB and bulk technologies was measured in our previous work [7] and the data of SBU (single bit upset) and MCU (multiple cell upset) in [7] is used for chip-level SER estimation. The FF SER in the same SOTB and bulk technologies was measured by Koboyashi et al., and the data in [6] is used. The data used in the chip-level SER estimation is listed in Tables II and III.

In this work, we estimate chip-level SER at 0.5 and 1.0V, and some data is missing. For obtaining missing data, we carried out curve fitting assuming $SER = a \cdot \exp(b \cdot V)$, where a and b are fitting parameters and V is the supply voltage. Using the obtained functions, we derived the data at 0.5V. Such derived data is listed with parenthesis in Tables II and III. Unfortunately, we have the SET SER at 0.5V only, and hence we cannot use curve fitting. We thus assumed the SET rates at 0.5V and 1.0V were the same. Measuring the SET voltage dependence is one of our future works.

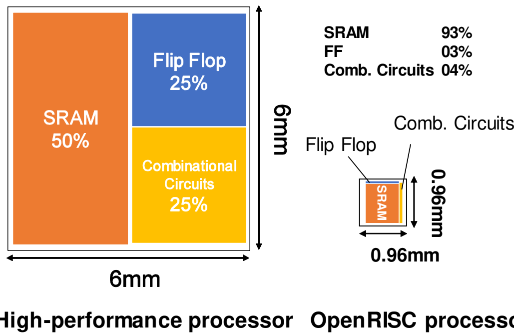

Fig. 6: Structure of high-performance and OpenRISC processor.

TABLE IV: Chip-level SER without ECC [FIT/Chip].

		0.5V	1.0 V
high-perf. processor	SOTB	6.0×10^3	1.8×10^3
	Bulk	8.2×10^4	2.7×10^4
embedded processor	SOTB	286.9	83.2
	Bulk	3.9×10^3	1.3×10^3

TABLE V: Contributions of SRAM, FF and combinational circuit to chip-level SER without ECC.

		SRAM		Comb.	FF
		MCU	SBU	SET	SEU
high-perf. processor	SOTB@0.5V	0.45%	99.28%	0.00%	0.27%
	SOTB@1.0V	0.51%	98.97%	<0.04%	0.49%
	Bulk@0.5V	5.54%	93.38%	0.04%	1.04%
	Bulk@1.0V	13.25%	85.57%	< 0.12%	1.06%
embedded processor	SOTB@0.5V	0.45%	99.53%	0.00%	0.02%
	SOTB@1.0V	0.51%	99.44%	0.00%	0.04%
	Bulk@0.5V	5.60%	94.31%	0.01%	0.09%
	Bulk@1.0V	13.40%	85.99%	< 0.02%	0.09%

In addition, for chip-level SER estimation, the cell numbers of an assumed high-performance processor and a representative embedded processor, OpenRISC 1200, were considered as the evaluation target in this paper. Fig. 6 shows the structure of high-performance processor with large amount of cache memory, larger register files and deeper pipelines, where 50% core area is occupied by SRAM, 25% is occupied by FF and the remaining 25% is occupied by combinational circuit. The core area is 36 mm^2. In our experiments, the sizes of 6T SRAM and FF cell were 0.56μm$\times$2.00μm and 1.80μm$\times$7.80μm, respectively. The combination circuit was assumed to be filled of inverters, where the area of an inverter was 1.8μm$\times$0.52μm. The capacity of SRAM was 11.79Mbit, and the numbers of FFs and inverters were 0.61M and 5.02M, respectively. As for OpenRISC 1200, the SRAM size for cache is 0.56Mbit. To estimate the number of cells, we synthesized the RTL files with a standard cell library. The number of FFs is 24k and the number combinational cells is 1.10M. The chip size and area portions of OpenRISC 1200 are also shown in Fig. 6.

Chip-level SER SER_{chip} is calculated as

$$SER_{chip} = (SER_{SBU} + SER_{MCU}) \times N_{SRAM} + SER_{SEU} \times N_{FF} + SER_{SET} \times N_{INV} \quad (3)$$

where N_{SRAM} is the number of SRAM bits in a chip, and N_{FF} and N_{INV} are the number of FFs and inverters in a chip. To estimate the maximum contribution of SET to chip-level SER, logical, temporal or electrical maskings are not considered in this calculation.

B. Estimation result and discussion

The calculated chip-level SER is listed in Table IV. The overall SERs of SOTB chip are 12.6X and 14.6X lower than those of bulk chip at 0.5V and 1.0V, respectively. Table V also shows a common tendency for both processors that soft

error in SRAM dominates in the total chip-level SER. In SOTB chip, more than 99% errors occur in SRAM, and other FF SEU and SET are negligible. Similarly, about 99% errors occur in SRAM in bulk chip.

Next, we apply ECC (error-correcting code) to SRAM. In this case, all SBUs are corrected by ECC. On the other hand, we assumed all MCUs were not corrected although some of MCU could be corrected even with SEC-ECC (single error correction ECC). The chip-level SER with ECC is listed in Table VI. In high-performance processor of SOTB, the chip-level SER was reduced by two orders magnitude while it was reduced by one order of magnitude in bulk chip. This is because the MCU SER is much lower than the SBU SER in SOTB chip. Consequently, the SERs of SOTB chip are 125X and 219X lower than those of bulk chip at 0.5V and 1.0V, respectively. ECC gives the same effect on embedded processors.

Table VII shows the decomposition of chip-level SER. With ECC, the proportions of FF and combinational circuits are different between the embedded and high-performance processors of SOTB while MCU in SRAMs still dominates in bulk processors. In high-performance processor of SOTB, the contribution of FF is large and reaches 48% at 1.0V while that in embedded contributes to only 6% at most. As for contribution of SET, Table VII suggests that SET is negligible for both the high-performance and embedded processors.

IV. Conclusion

In this paper, the chip-level neutron-induced SER of SOTB and bulk circuits at 0.5V and 1.0V and the contributions of SRAM, FF and combinational circuit to the chip-level SER were investigated. Combining the measured SET rate with previously reported SERs, chip-level SER of processors made of SOTB and bulk CMOS were calculated. Without ECC, 99% errors occur in SRAM in both SOTB and bulk chips and in both embedded and high-performance processors. With ECC, the contribution of FF in SOTB high-performance processor was 48% at 1.0V, whereas the contribution of combinational circuits was still less than 3%. The SET ratio to FF SEU in our evaluation ranges from 3.85% to 22.22%, where no temporal masking is considered. Taking into account the temporal masking, our result is consistent with the simulation based result with a maximum ratio of 2% in [10]. Therefore, radiation-hard FF SEU is helpful for SOTB high-performance processors while SET is negligible for both the processors. On the other hand, with ECC, the MCU portion is larger in the embedded processor than the high-performance processor and it exceeds 90%. In addition to the large contribution of SER of SBUs in SRAM without ECC, the priority of soft error mitigation should be given to SRAM from the viewpoint of chip-level SER in both high-performance and embedded processors.

Acknowledgment

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TABLE VI: Chip-level SER with ECC [FIT/Chip].

		0.5V	1.0V
high-perf. processor	SOTB	43.5	17.8
	Bulk	5.4×10^3	3.9×10^3
embedded processor	SOTB	1.3	0.5
	Bulk	220.1	171.6

TABLE VII: Contributions of SRAM, FF and combinational circuit to chip-level SER with ECC.

		SRAM		Comb.	FF
		MCU	SBU	SET	SEU
high-perf. processor	SOTB@0.5V	61.20%	–	1.46%	37.34%
	SOTB@1.0V	49.12%	–	$<$ 3.54%	47.34%
	Bulk@0.5V	83.67%	–	0.60%	15.73%
	Bulk@1.0V	91.82%	–	$<$ 0.84%	7.34%
embedded processor	SOTB@0.5V	94.97%	–	0.29%	4.74%
	SOTB@1.0V	91.89%	–	$<$0.86%	7.25%
	Bulk@0.5V	98.40%	–	0.09%	1.51%
	Bulk@1.0V	99.23%	–	$<$ 0.12%	0.65%

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