50x20 Crossbar Switch Block (CSB) with Two-Varistors (a-Si/SiN/a-Si) selected Complementary Atom Switch for a highly-dense Reconfigurable Logic

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***Abstract*—** A large scale, 50x20 crossbar switch block (CSB) is newly developed for a nonvolatile, highly-dense reconfigurable logic. A compact two-varistors selected complementary atom switch (a.k.a. via-switch) is placed at each cross-point, in which the two control lines connected to the varistors can realize the multiple fan-outs without select transistors. The improved a-Si/SiN/a-Si varistor with a novel triple layered SiN shows superior nonlinearity (NL) of $1.1x10^5$ with J_{max}=1.63MA/cm^2 while keeping very low static power of 0.2μW for the CSB. The developed CSB is also applicable for nonvolatile configuration memory for look up tables (LUTs) as well as routing switches used in low power reconfigurable logic.

I. Introduction

In IoT era, a huge number of devices will connect to networks through wireless communications. Field programmable gate array (FPGA) is one of the candidates for IoT device because of its high performance, reconfigurability and short turn-around time (TAT). However, reducing power consumption is essential for the IoT applications to save the buttery life [1]. In the previous work, we have demonstrated complementary atom switch (CAS)-based FPGA, in which the CAS is used both for crossbar switch and configuration memory of look up table (LUT) (Fig. 1) [2]. Totally, the energy efficiency is improved by 61% as compared to the conventional SRAM-based FPGA [3]. Thus, the improvement of energy-delay product of FPGA using nonvolatile devices becomes of great interest [4-7].

The CAS is composed of two compact bipolar-resistive-change elements with nonvolatility, namely atom switch. The atom switch turns to ON or OFF by forming or annihilating a conductive Cu bridge in polymer solid-electrolyte (PSE) [8], where a select transistor enables to program (set/reset) each CAS (1T-1CAS) [9]. However, the select (programming) transistors occupy the large area in a chip even though the CAS itself is very small. In order to eliminate the select transistors, we have developed DCAS for further reducing the chip area [10]. To be in succession, the two-varistors selected CAS (2V-1CAS, a.k.a. via-switch) with the foot print of 18F^2 has also proposed for realizing the multiple fan-outs (FOs) (multiple cross-point programming per column or row) of the CSBs, where the nitrogen-modulated a-Si/SiN/a-Si varistor is introduced [11, 12]. It is estimated that the 2V-1CAS gives further 75% area-reduction to the conventional 1T-1CAS FPGA (Fig. 2). However, for realizing the estimated performance of the 2V-1CAS-FPGA, nonlinearity (NL) of the varistor needs to be further improved not only for suppressing the sneak current during the programming, but also reducing a static power consumption during the operation.

In this study, to improve the varistor's NL, a triple layered SiN stack varistor sandwiched by a-Si layers is newly proposed. And to ensure the cross-point selectivity by the two varistors, a 50x20 CSB with 2V-1CAS at each cross-point is fabricated. The programmability and signal transfer via multiple-FOs of the CSBs and memory configuration for LUTs are successfully demonstrated (Fig. 3).

II. Improvement of Varistor's Performance

First, the relationship between NL and the static power of the CSB is discussed. Figure 4(a) shows the measured current-voltage (I-V) curve of atom switch and the required I-V curve of the varistor. The atom switch turns to ON-state at 2V and turns to OFF-state at -2V. To program the atom switch, the varistor is desired to have the slightly higher leakage than that of the atom switch, the bidirectional current flow and high NL at ±2V. When the CSB with 2V-1CAS is programmed for multiple-FOs, the leak current could be flown through two varistors and one OFF-state atom switch. Here, The NL is defined as ON/OFF current ratio between ON-state at 2V and OFF-state at 0.25V [11]. Figure 4(b) shows the simulated static power of the 50x20 CSB at operating voltage (V_{DD}=0.5V) as a function of NL with three different configurations of the CSB. The static power depends on the configuration, namely the numbers of multiple-FOs. The higher NL and OFF resistance (R_{off}) than 10^5 and 50MΩ are desirable to reduce the static power of the CSBs for every configuration.

To improve NL, a-Si/SiN/a-Si varistor with a triple layered SiN stack is newly proposed. The SiN stack is deposited by PECVD and the nitrogen content of the SiN film is controlled by changing SiH_4 gas flow. The different SiN films having the nitrogen content from 47 to 51atom% are obtained (Fig. 5). In the case of single layered SiN varistors, it is difficult to improve NL even if the thickness and nitrogen content of SiN are precisely tuned (Fig. 6). The triple layered SiN stack consists of a thin N-rich (high nitrogen content of 51%) SiN sandwiched between two N-poor (low nitrogen content of 49%) SiN layers and shows the high NL over 10^5. It is supposed that the tunneling current under high voltage is enhanced by using thin SiN and the leakage current under low voltage is kept low both by the N-rich SiN and the high barrier height (BH) among a-Si/N-poor SiN (Fig.7) [13].

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Next, the developed a-Si/SiN/a-Si varistor is integrated on a Cu line (M1) in a 65nm-node BEOL on a 300mm wafer. In Fig. 8(a), the bottom Ru-alloy electrode and varistor stack of TiN/a-Si/SiN/a-Si/TiN layers are deposited on Cu through contact hole directly. Figure 8(b) shows the current density–voltage curve of the integrated varistor, which exhibits NL of $1.1x10^5$, R_{off} of 270MΩ at 0.25V and maximum current density (J_{max}) of 1.63MA/cm^2. Figure 9 indicates good in-plane ON/OFF current distribution (62 chips) of integrated varistors. The NL shows ~10^5. In Fig. 10, the performances of developed varistors are compared with those of conventional varistors in our previous studies [10, 11]. It is obvious that the both of J_{max} and NL of the developed varistor are superior to those of the previous nitrogen-modulated SiN varistors [11]. The small temperature dependence of the ON and OFF current is originated from the small activation energies (E_a) of 0.032eV of the ON-state and 0.037eV of the OFF-state, respectively (Fig. 11). This result supports the tunneling conduction model of the varistor as shown in Fig.7. Since the E_a of OFF resistance of atom switch is also small about 0.2eV [8], the developed varistor performance is suitable for applications at high temperatures. Figure 12 shows the endurance characteristic of the varistors. The high ON/OFF current ratio is confirmed for 1000 cycles, which are enough for the FPGA application.

III. Demonstration of 50x20 CSB

Figure 13 shows the device structure and process flow for fabricating the 2V-1CAS stack using dual-hard mask (DHM) etching process. The buffer, PSE and Ru-alloy (CAS) are deposited on the hole, followed by TiN/a-Si-/SiN/a-Si/TiN varistor stacking. The DHM process enables to transfer the 2V-1CAS pattern on the stack [11]. Three masks are added to fabricate the 2V-1CAS. Figure 14 shows the cross-sectional SEM and TEM images of the fabricated device. The CSB featuring 2V-1CAS is truly integrated between two layered Cu interconnects. Figure 15 shows the I-V characteristics of single side of the integrated 2V-1CAS. By applying the positive voltage to T1 with keeping C2 grounded (Fig. 3), the Cu bridge is formed in the PSE and the atom switch turns to ON-state. In contrast, by applying negative voltage to T1, the Cu bridge is annihilated and the atom switch turns to OFF-state. The set and reset voltages are slightly increased due to voltage drop in the varistor. After the set programming of the atom switch, the low current at the low voltage around 0.25V indicates the OFF current of the varistor, which is well consistent with the characteristic of the single varistor shown in Fig. 8.

Before demonstrating the large scale CSB, the programming and signal transfer performances for the multiple-FOs are evaluated by using a small 4x4 CSB. After four switches are programmed, the current map is measured, indicating that all switches are accurately programmed (Fig. 16(a)). Then, to confirm the multiple-FOs functionality, the input signal of 0.5V is applied to the input port of IN1 and the output signals are detected from the output ports of OUT1 and OUT2 (Fig. 16(b)). Without waveform degradation, the signal transfer is confirmed. To check the cross-point characteristics during the programing, the ON/OFF characteristics between T1 and T2, and the leak current between C1 and C2 are measured (Fig. 16(c)). Large electrical separation between the two varistors and the high ON/OFF current ratio of the CAS are confirmed. In the 4x4 CSB, the increment of leak current with increasing the number of the multiple-FOs is experimentally confirmed (Fig. 17), which is well consistent with our estimation as shown in Fig. 4(b).

Figure 18 shows the layout of 50x20 CSB and three dimensional (3D) images of SEM using the focused ion beam technique. In this work, to demonstrate 2V-1CAS CSB, two layered 65nm-node Cu interconnects are used. Figure 19 shows optical microscope images of the 50x20 CSB using 2V-1CAS. To demonstrate the multiple-FOs in the CSB, six CASs are programmed along the two column lines (column 4 and 9 (Fig. 20(a)). After programming, we input signal waves to IN4 and IN9 and detect output signals from all output ports. As a result, the accurate signal transfers are confirmed with small cross-talk (Fig. 20(b)). Thus, the large scale CSB with 2V-1CAS is successfully demonstrated.

Finally, to check the feasibility of replacing the SRAM-based configuration memory of LUT with the 2V-1CAS crossbar switch, a configuration of 4-input XOR gate is programmed by using 16x2 crossbar array with the 2V-1CAS (Fig. 21(a)). One signal input port is connected to V_{DD} (0.5V) and the other to ground. The programmed XOR configuration can be loaded to the output ports without a sense amplifier (Fig. 21(b)).The large scale CSB with 2V-1CAS (via-switch) is a strong candidate for realizing for low-power and low-cost, nonvolatile reconfigurable logic.

IV. Conclusion

For the first time, a large scale, 50x20 crossbar switch block (CSB) is successfully demonstrated by using integrated two varistors with complementary atom switch (2V-1CAS) structure in Cu BEOL with multiple-FOs. The newly proposed triple layered a-Si/SiN stack/a-Si varistor improves the NL and OFF resistance of more than 10^5 and 50MΩ, respectively, which can be applied to not only routing switch but also configuration memory for LUTs of low-power FPGA.

Acknowledgment

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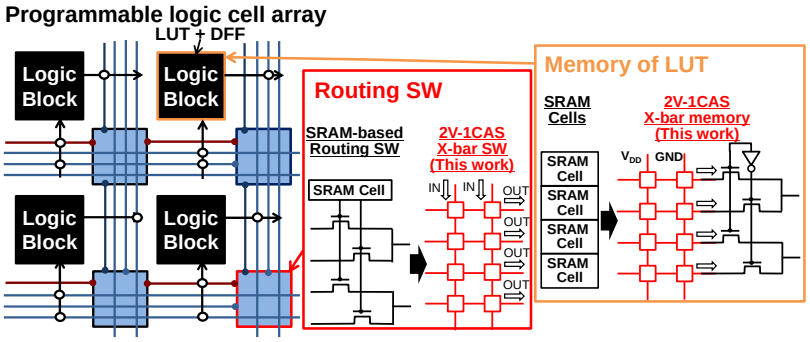

Fig.1. Schematic diagram of programmable logic. SRAM-based routing switch and configuration memory of LUTs are replaced by crossbar switch block (CSB) with two-varistors selected complementary atom switch (2V-1CAS).

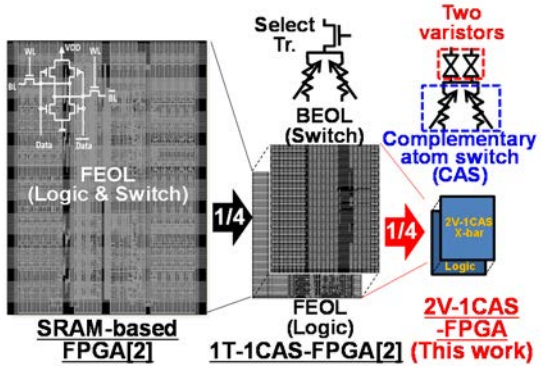

Fig.2. Comparison of novel 2V-1CAS-FPGA with conventional FPGA using SRAM-based switch [2]. By replacing select transistors with varistors, chip size reduction is estimated to be more than 90% for 2V-1CAS-FPGA compared with SRAM-based FPGA.

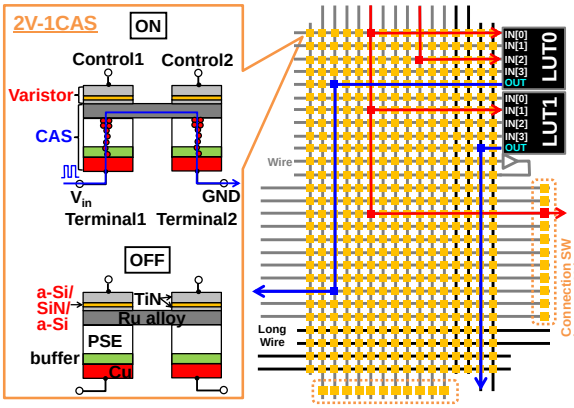

Fig.3. Schematic views of device structure of 2V-1CAS [11] and large scale CSB using 2V-1CAS. 2V-1CAS structure attains small foot print and multiple-FOs without select transistor.

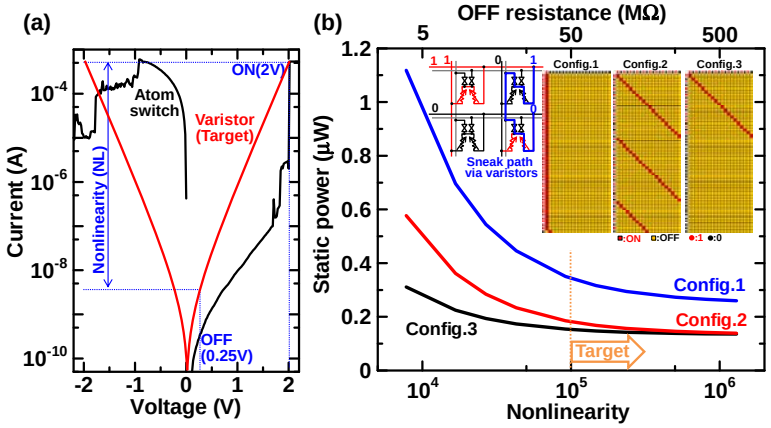

Fig.4. (a) Schematic view of measured I-V curve of atom switch and required I-V curve of varistor for 2V-1CAS crossbar application. (b) Simulated relationship between static power of 50x20 CSB and NL of varistor at three different configurations. ON current is supposed to be 500μA for extracting NL.

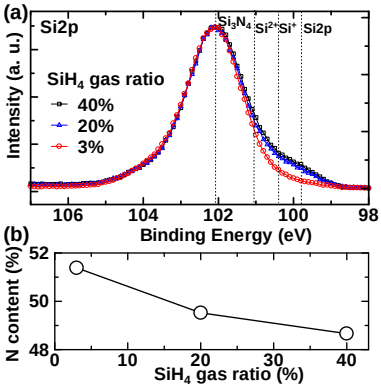

Fig.5. (a) Si 2p XPS spectra of SiN with SiH_4 gas ratio. (b) Nitrogen content in SiN with various SiH_4 gas flow.

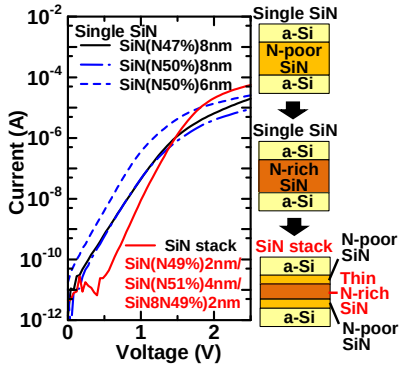

Fig.6. I-V characteristics of a-Si/SiN/a-Si films. Different SiN stacks are compared.

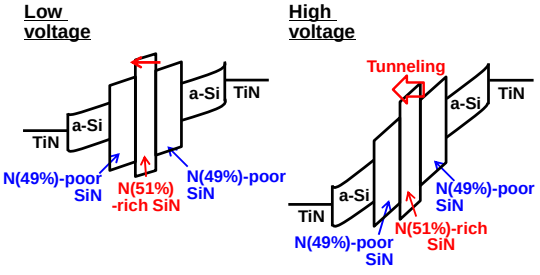

Fig.7. Conduction model under applying low or high voltage. Triple layered SiN stack consists of N-rich thin SiN and N-poor SiN. SiN stack keeps high OFF resistance and enhances ON current.

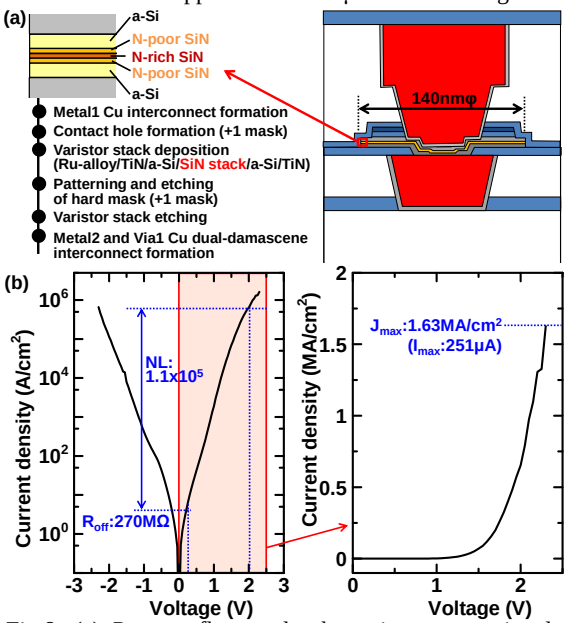

Fig.8. (a) Process flow and schematic cross-sectional illustrations of varistor without CAS. (b) Log and linear Y-scale current density–voltage characteristics of integrated varistor using triple layered SiN stack with N-rich thin SiN.

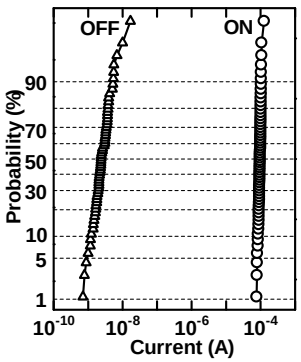

Fig.9. Distributions of ON and OFF current of varistor in 300mm wafer. NL is ~10^5.

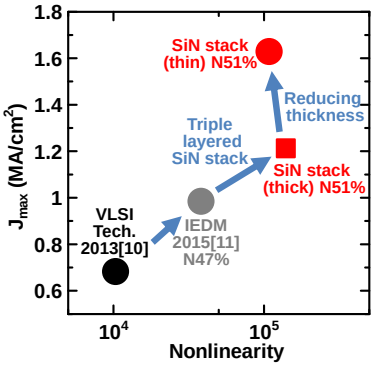

Fig.10. Benchmark of relationship between J_{max} and NL of varistors for CAS.

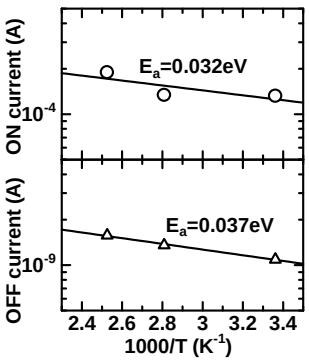

Fig.11. Temperature dependence of ON and OFF current of varistor. Activation energies (E_a) show around 0.03eV.

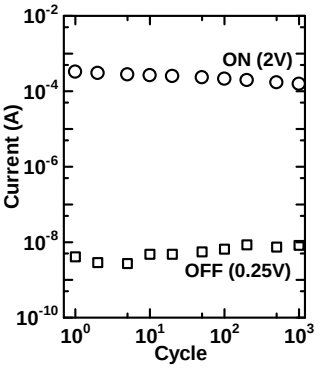

Fig.12. ON/OFF current characteristics of varistor when voltage is applied for 10^3 cycles.

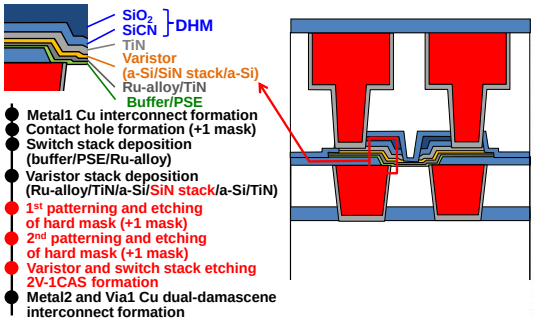

Fig.13. Schematic cross-sectional illustrations of integrated 2V-1CAS stack using dual-hard mask (DHM) and process flow [11].

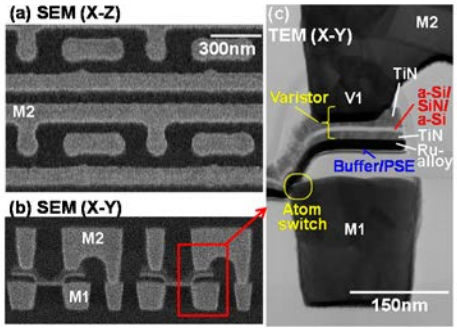

Fig.14. (a) Planar (M2) and (b)(c) cross-sectional images of 2V-1CAS integrated in 65nm-node Cu-BEOL.

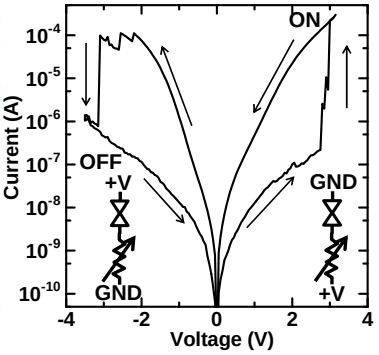

Fig.15. Set/reset characteristics of single side of 2V-1CAS.

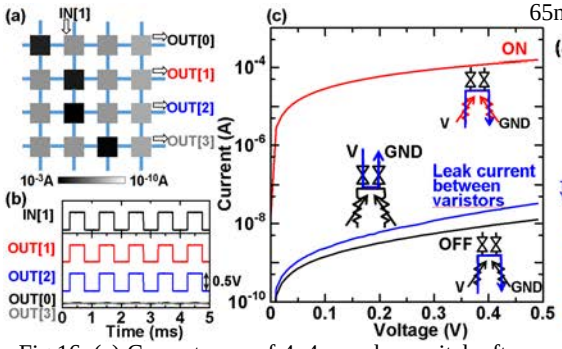

Fig.16. (a) Current map of 4x4 crossbar switch after programming. (b) Outputs of OUT0–3 when signal applies to IN1. (c) ON and OFF-state characteristics of 2V-CAS with leak current between varistors.

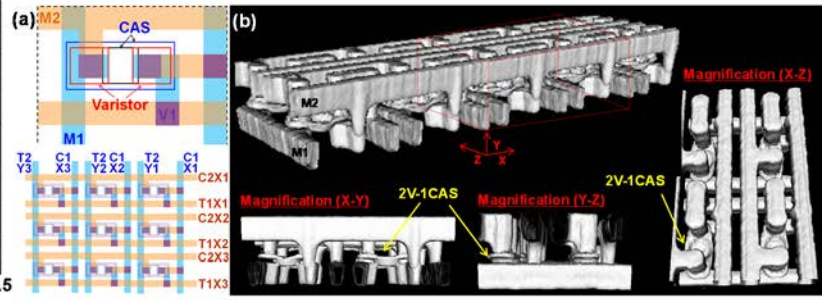

Fig.18. (a) Schematic illustrations of CSB design of 2V-1CAS. 2V-1CASs are embedded in two layered Cu interconnects. (b) 3D-SEM images of a part of integrated 50x20 crossbar switch.

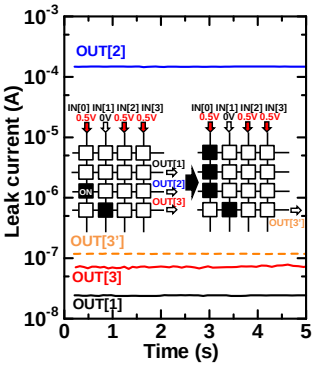

Fig.17. Leak current from OUT3 after adding two multiple-FOs.

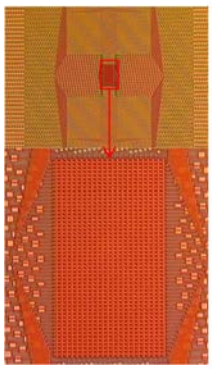

Fig.19. Optical microscope images of 50x20 CSB with 2V-1CAS.

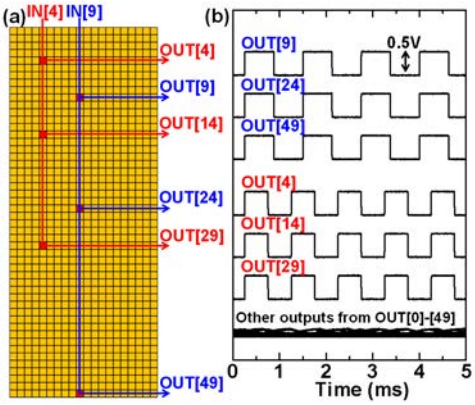

Fig.20. (a) Programming configuration of 50x20 crossbar switch with 2V-1CAS. (b) Outputs of OUT0-49 when signal applies to IN4 and IN9.

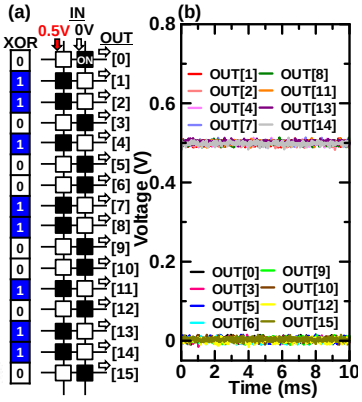

Fig.21. (a) XOR-configuration for LUT using 2V-1CAS. (b) Outputs of OUT0-15. Each signal port is connected to V_{DD} or ground.