A Novel Two-Varistors (a-Si/SiN/a-Si) selected Complementary Atom Switch (2V-1CAS) for Nonvolatile Crossbar Switch with Multiple Fan-outs

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Abstract

A nonvolatile and compact switch realizing multiple fan-outs of a crossbar switch for programmable logic devices (PLDs) has been newly developed by using two-varistors selected complementary atom switch (2V-1CAS). The two control lines connected to the varistors realize the accurate programming of each cross-point without select transistors. The novel nitrogen-modulated, TiN/a-Si/SiN/a-Si/TiN varistor shows superior nonlinear (NL) characteristic of ~10^5, which are successfully stacked on the top of CAS with dual-hard mask (DHM) process. The developed 2V-1CAS ($18F^2$) gives a promising switch block (SB) used for energy-efficient, nonvolatile PLDs.

Introduction

A CMOS scaling is now experiencing serious roadblocks, and in near future, the scaling will certainly face a physical limit of the device dimension at the nanometer-regime. A new flexibly programmable switch in Cu-back-end-of-the-line (Cu-BEOL) is strongly desired for enhancing chip performance and decreasing chip cost without CMOS scaling [1]. As one of the practical application-based demands, low-capacitive and single-stage programmable switch is mandatory for reducing dynamic power of programmable logic devices (PLDs) used in IoT era.

In the previous work, we introduced low-capacitive complementary atom switch (CAS)-based crossbar switch, in which the cell area is dramatically reduced as compared to an SRAM-based crossbar switch (Fig. 1) [1-3]. In reality, the reduction of the capacitance in the routing path due to a shortened wire length and smaller capacitance of the CAS contributes to 61% reduction in active power consumption compared with the SRAM-based one. Figure 2 shows the device structure, operation principle and current-voltage (I-V) characteristics of the CAS. The CAS, composed of two bipolar-resistive-change elements, namely atom switch (Fig. 2(a)), has improved OFF-state lifetime with low voltage programming. The atom switch turns to ON or OFF by forming or annihilating a conductive Cu bridge in polymer solid-electrolyte (PSE) (Fig. 2(b)) [4], where a select transistor is used for programming each CAS. However, the transistors occupy the large area in a chip even though the CAS itself is very small. To pursue higher area-efficiency, a bidirectional diode using TaO stacked on the CAS (DCAS) was proposed [5], but the DCAS suffers from a functional limitation of single fan-out (FO) in the crossbar.

In this work, to realize small size and high functionality (multiple-FOs) of the crossbar switch, we have newly proposed two-varistors selected CAS (2V-1CAS) structure using a novel a-Si/SiN/a-Si varistor. The heterogeneous structure of a-Si/SiN/a-Si causes nitrogen moderated region in SiN, resulting in a high nonlinearity (NL). The switch can be truly integrated in Cu-BEOL without transistors. Since the 2V-1CAS has two independent control terminals, the multiple cross-points in the row or column can be selected without using the select transistors.

Novel a-Si/SiN/a-Si varistor

Figure 3 shows the crossbar switch using 2V-1CAS in comparison with conventional 1T-1CAS [3] or DCAS (1D-1CAS) [5]. Since the two varistors of 2V-1CAS are connected to independent control lines, respectively, the CASs can be programmed individually, resulting in multiple-FOs. When the crossbar switch with 2V-1CAS is programmed for multiple-FOs, the sneak current could be flown through two varistors and one OFF-state atom switch. To keep total series resistance higher than 100MΩ at operation voltage (V_{DD}=1V) for preventing the sneak current, the resistance of the varistor should be over 25MΩ at 0.25V (Fig. 4(a)). Therefore, an ideal nonlinearity (NL) characteristic of the varistor is defined as more than 10^4 between the OFF-state at 0.25V and the ON-state at 2V, as shown in Fig. 4(b).

To satisfy the high NL characteristics more than 10^4, the nitrogen-modulated a-Si/SiN/a-Si stack is newly proposed. The amorphous SiN and a-Si layers are deposited by plasma-enhanced chemical vapor deposition (PE-CVD) at low temperature. No peak is detected in in-plane X-ray diffraction spectra of SiN and a-Si layers, indicating that both layers are amorphous (Fig. 5). As shown in Fig. 6, the each single layer I-V characteristic shows poor NL performance. To improve the NL performance, we propose a new technique to use the a-Si layer as a barrier height control (BHC) layer. In Fig.7, the varistor stack of a-Si(5nm)/SiN(8nm)/a-Si(5nm) gives larger NL of 9.6×10^4 in comparison with the single SiN layers of 8nm and 15nm. The NL performance is optimized by changing the thickness of a-Si and SiN layers in Fig. 8. The combination of a-Si(5nm) and SiN(8nm) shows the best NL performance.

The depth profile of the a-Si/SiN/a-Si reveals that the nitrogen concentration is modulated continuously at the interface between a-Si and SiN layers. Figure 9 shows depth profiles of N, Ti and Si composition ratio in TiN/SiN(10nm) stack or TiN/a-Si(5nm)/SiN(10nm) stack from X-ray photoelectron spectroscopy (XPS) analysis. In the TiN/a-Si(5nm)/SiN(10nm) stack (Fig. 9(b)), N composition ratio of SiN reduces with approaching to the interface between SiN and a-Si in comparison with TiN/SiN(10nm) stack (Fig. 9(a)). In Fig. 10, the XPS spectrum of Si2p after 16 sputtering cycles includes peaks attributed to Si-rich SiN (Si^{+} and Si^{2+}). Namely, a Si-rich region is formed at the interface between SiN and a-Si. The nitrogen-modulated varistor stack has the Si-rich SiN layer between SiN and a-Si layers. From the XPS analysis, we propose a conduction model under applying low or high voltage (Fig. 11). When the low voltage is applied to the stack (in operation-mode), the small current flows due to the barrier height of a-Si and SiN. When the high voltage is applied to the stack (in programming-mode), the large tunnel current flows through the SiN layer since the Si-rich SiN layer has many trap sites. We also optimized the electrode material, and concluded that the TiN electrode is suitable for the developed varistor (Fig. 12).

2V-1CAS integration in Cu BEOL

First, the a-Si/SiN/a-Si varistor is fabricated on a Cu line (M1) in a 65nm-node Cu BEOL. In the case of only varistor, the Ru-alloy electrode and TiN/a-Si/SiN/a-Si/TiN layers are deposited on Cu through contact hole directly. Figure 13 shows the I-V curve of the integrated a-Si/SiN/a-Si varistor, which exhibits NL of 3.8 x 10^4 (between 0.25V and 2V) and maximum current density J_{max} of 0.73MA/cm^2 at 2V. The NL and J_{max} of TaO diode in DCAS were 8.0 x 10^3 and 0.6MA/cm^2, respectively [5]. Thus, the NL performance for CAS is improved by using the new a-Si/SiN/a-Si varistor. Second, the 2V-1CAS operation is demonstrated using integrated device in the Cu BEOL. The 2V-1CAS is fabricated on the edge of two Cu lines (M1). Figure 14 shows the process flow for fabricating 2V-1CAS stack using dual-hard mask (DHM). The buffer and PSE layers are deposited on Cu through contact hole, and Ru-alloy top electrode is deposited. During the PSE deposition, the buffer-metal prevents the Cu electrode from oxidizing and changes to metal oxides. These metal oxides work as a part of the solid-electrolyte [6, 7]. Then, the TiN/a-Si/SiN/a-Si/TiN layers are deposited on the CAS stack. The 2V-1CAS stack is dry-etched by using the DHM process of SiCN/SiO_2. The DHM process enables to transfer the 2V-1CAS pattern on the stack without any plasma damages on the varistor and CAS (Fig. 15). To form the pattern of varistor region, a part of SiO_2-HM is etched by using the first mask. After that, to form the pattern of switch stack region included the varistor region, the residual SiO_2-HM is etched by using the second mask. The SiCN-HM protects the 2V-1CAS stack from O_2-ashing damage. After the etching of 2V-1CAS stack using the metal etcher, the top electrode of varistor (TiN) is etched except for the varistor region, and the top electrode of CAS (Ru-alloy) remains on both of CAS and varistor regions. The 2V-1CAS can be integrated with very small foot print of $18F^2$.

Figure 16 shows the I-V characteristics of 2V-1CAS assuming the crossbar switch operation. By applying the voltage to Terminal 1 (T1) or Control 2 (C2) and another is grounded, the Set and Reset voltages are slightly increased due to voltage drop in varistor. The atom switch changes to the ON-state around 2.5V and the programming current compliance (CC) is successfully achieved by the stacked varistor. The Set and Reset programming of the atom switch through the varistor is confirmed. In the 2V-1CAS programing, the electrical connection/disconnection between T1 and Terminal 2 (T2) in the 2V-1CAS is demonstrated in Fig. 17(a). In the ON-state, high current between T1 and T2 is observed, which can be used for signal transfer. The ON/OFF current ratio of the CAS is 4.6 x 10^5. Figure 17(b) shows the leakage current between T1 and Control 1 (C1) or C2. The electrical separation through the varistor before/after the programming is also demonstrated. Table I summarizes the developed 2V-1CAS for crossbar switch application in comparison with 1T-1CAS and DCAS. Since 2V-1CAS structure achieves both of compactness and multiple-FOs, the 2V-1CAS is a strong candidate for realizing the compact switch block (SB) for energy-efficient, nonvolatile programmable logic.

Conclusion

The novel a-Si/SiN/a-Si varistor is developed for two varistors with complementary atom switch (2V-1CAS) crossbar switch block (SB). The nitrogen modulation technique realizes the superior NL characteristic of $\sim 10^5$, which can be used for programming each cross-point without a select transistor. The developed 2V-1CAS successfully integrated in the Cu BEOL with dual-hard mask (DHM), resulting in the compact and low capacitive crossbar SB with multiple-FOs.

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References

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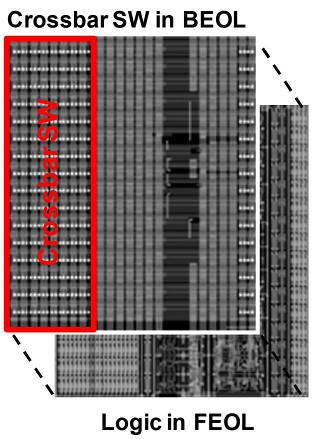


Fig.1 Schematic of programmable logic device with crossbar switch using complementary atom switch (CAS) with select transistor (1T-1CAS) [2].

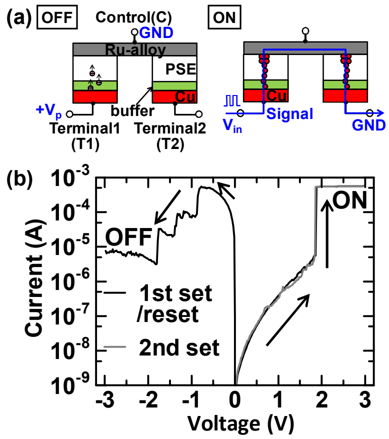


Fig.2 (a) Schematic operation of CAS composed of Control (C), Terminal 1 (T1), and Terminal 2 (T2). (b) Current-voltage (I-V) characteristics of single-side of CAS, which show forming-free operation.

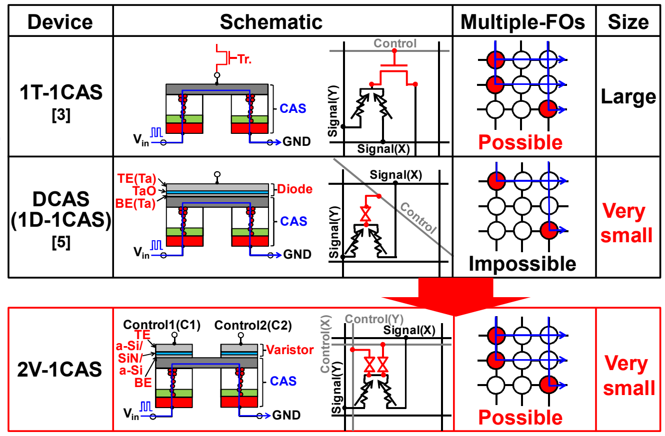


Fig.3 Comparison of novel two-varistors selected CAS (2V-1CAS) with conventional 1T-1CAS [3] or diode selected CAS (DCAS) [5]. 2V-1CAS structure realizes small foot print and multiple-FOs without select transistor.

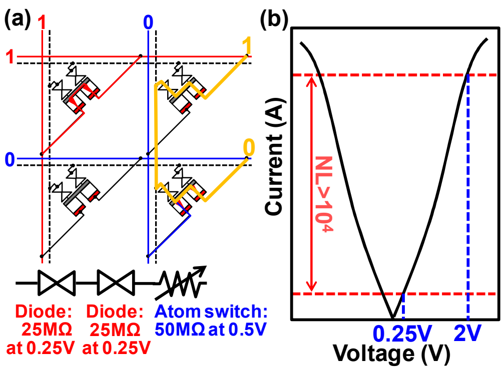


Fig.4 (a) Schematic view of sneak path in crossbar switch using 2V-1CAS at operation. Sneak current flows through two varistors and one atom switch during signal transfer. (b) Ideal varistor performance for 2V-1CAS crossbar application. Nonlinearity of more than 10^4 is desirable.

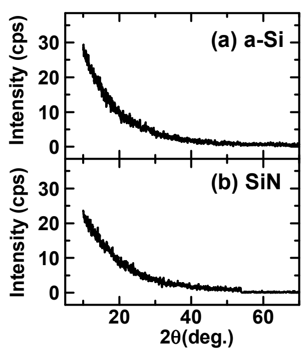


Fig.5 In-plane XRD spectra of (a) a-Si or (b) SiN. Both XRD spectra show amorphous.

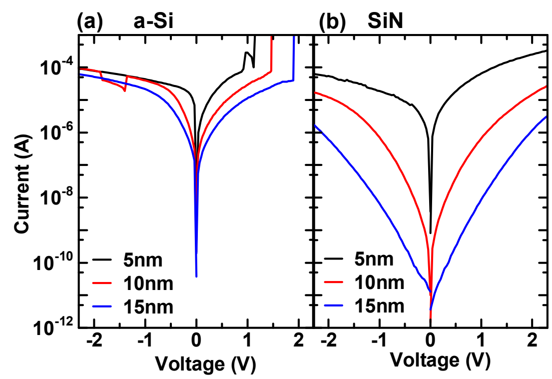


Fig.6 I-V characteristics of (a) a-Si and (b) SiN films for varistor layer. SiN or a-Si layers are deposited on TiN electrode.

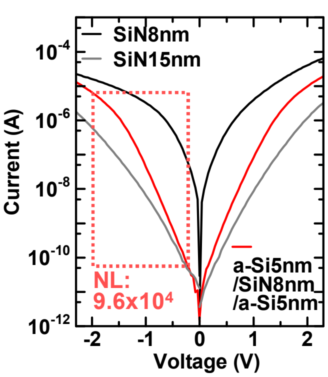


Fig.7 Comparison of I-V characteristics of varistor using single SiN or a-Si/SiN/a-Si stack. Nonlinearity (NL) of a-Si/SiN/a-Si stack shows 9.6×10^4.

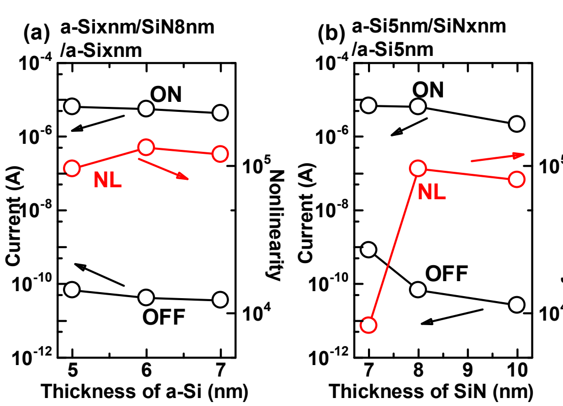


Fig.8 Thickness of (a) a-Si or (b) SiN dependence of ON current at -2V, OFF current at -0.25V and NL. NL depends on the thickness of SiN in comparison with a-Si.

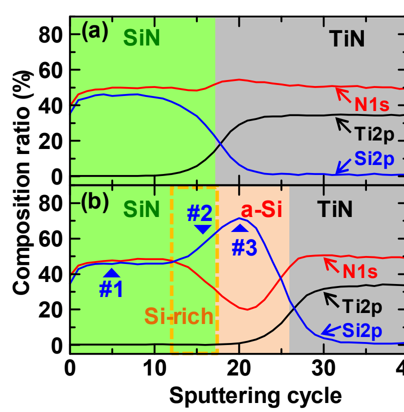


Fig.9 Depth profiles of N, Ti and Si composition ratio in (a) TiN/SiN(10nm) or (b) TiN/a-Si(5nm)/SiN(10nm) from XPS analysis. Tilt angle of analyzer is 30°.

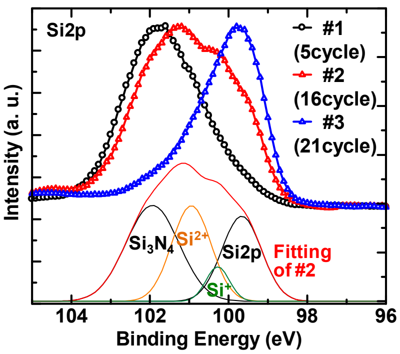


Fig.10 XPS spectra at #1 (5 cycle), #2 (16 cycle) and #3 (21 cycle) in Fig. 9(b). Interface between a-Si/SiN (#2) shows peaks attributed to Si-rich SiN (Si^{+} and Si^{2+}).

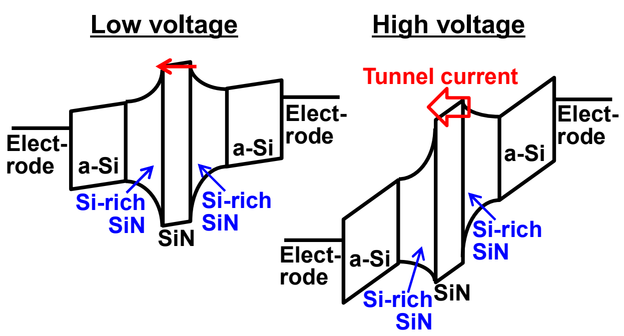


Fig.11 Schematic conduction model under applying low or high voltage. Si-rich SiN layers at a-Si/SiN interface work for enhancing the ON-current under high voltage.

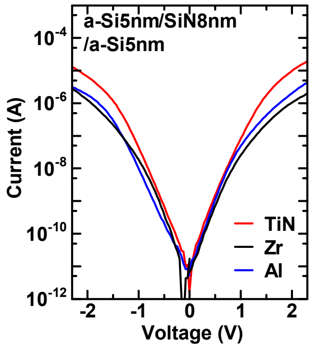


Fig.12 Electrode material dependence of I-V characteristics. TiN is suitable for varistor.

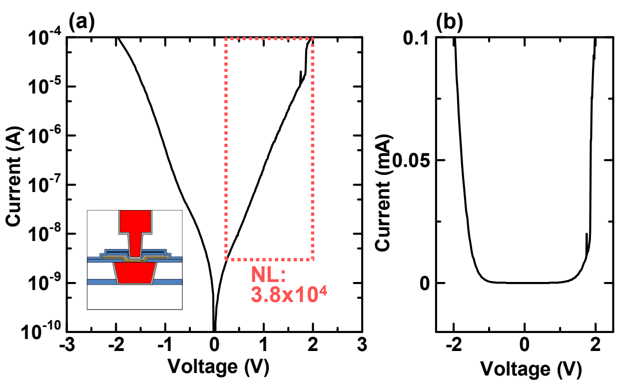


Fig.13 I-V characteristics of integrated a-Si/SiN/a-Si varistor without CAS. (a) Log Y-scale graph with cross-sectional illustration of varistor. (b) Linear Y-scale graph.

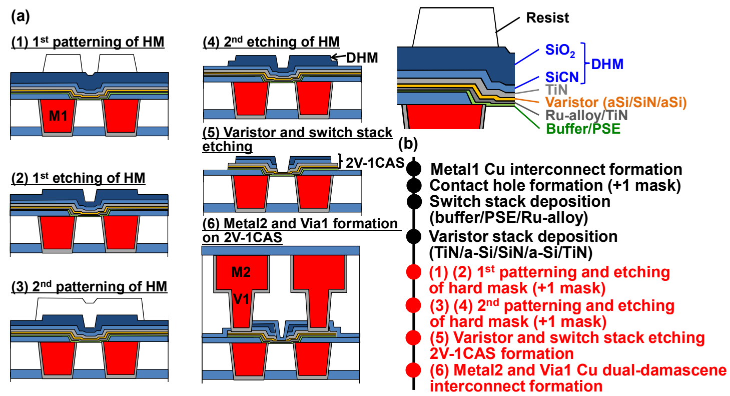


Fig.14 (a) Schematic cross-sectional illustrations of process flow for fabricating 2V-1CAS stack using dual-hard mask (DHM). (b) Process flow of 2V-1CAS embedded in 65nm-node BEOL.

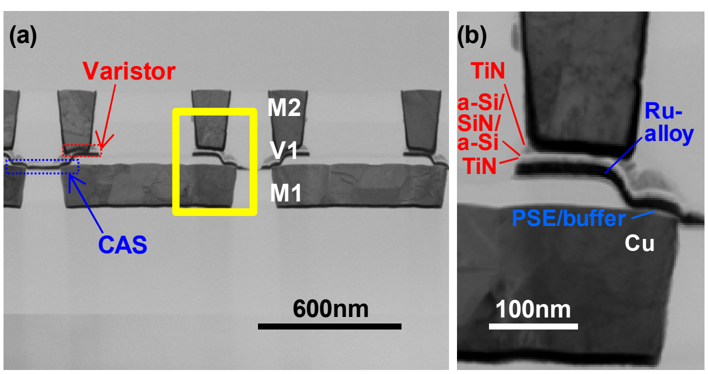


Fig.15 Cross-sectional TEM images of 2V-1CAS integrated in 65nm-node Cu-BEOL. (a) Low and (b) high magnification views.

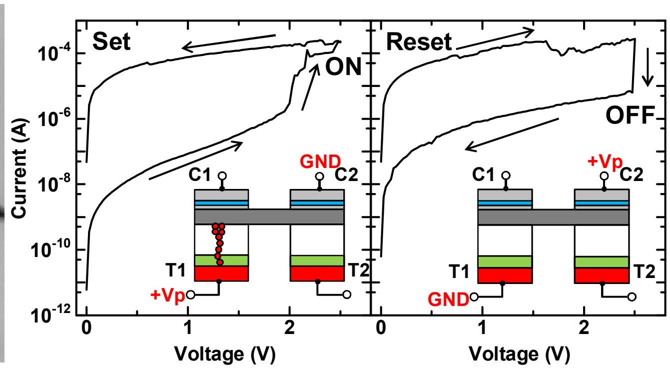


Fig.16 Set/reset characteristics of 2V-1CAS by applying voltage to T1 or Control 2 (C2) and another is grounded. Set/reset voltages are slightly increased due to voltage drop in varistor.

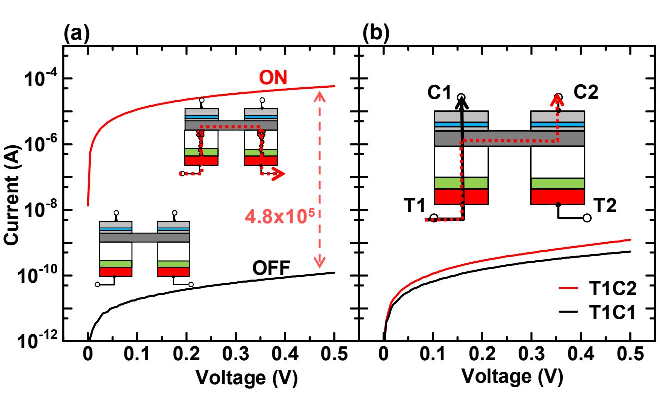
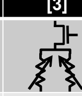
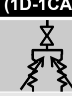


Fig.17 (a) ON and OFF-state characteristics of 2V-1CAS. ON/OFF current ratio is 4.8×10^{5}. (b) OFF-state leakage current between T1 and Control 1 (C1) or C2.

Table I. Device summary.

	1T-1CAS [3]	DCAS [5] (1D-1CAS)	This work (2V-1CAS)
Schematic			
Current limitation device	Tr.	Metal oxide diode (TaO)	N-modulated varistor (a-Si/SiN/a-Si)
J_{max}	-	0.6MA/cm²	0.73MA/cm²
NL(2V/0.25V)	-	8.0x10³	3.8x10⁴
Area	Large	Very small	Very small
Multiple-FOs	Possible	Impossible	Possible