

Real-time On-chip Supply Voltage Sensor and Its Application to Trace-based Timing Error Localization

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Abstract—This paper presents an all-digital on-chip supply voltage sensor that captures one-shot voltage fluctuation every clock cycle. The proposed sensor was implemented on ASIC in 65nm process and FPGA. The obtained voltage resolution was 3.9mV and 29mV, respectively. This sensor is suitable for providing voltage information to trace-based error localization system. We experimentally show that the proposed sensor contributes to the facilitation of error localization.

Keywords—supply voltage sensor, timing error, fault localization, trace buffer

I. INTRODUCTION

In the past decades, the integration density of integrated circuits (ICs) has grown exponentially, which brings amazing performance improvement and explodes IC usages. In pursuing the performance of a circuit implemented on a chip, the design margin should be minimized to exploit the inherent performance of VLSI/FPGA chips. However, in such a situation, electrical timing faults sometimes happen. Once an electrical timing fault appears, time-consuming hardware debugging and validation must be carried out. Here, an electrical timing fault is a bug that arises even though the circuit is logically correct, and it is infrequently caused by dynamic events such as fluctuation of supply voltage and temperature. The electrical timing fault arises as a bit flip in a certain clock cycle, and is likely to occur in paths with small timing slacks. However, it arises only under a certain situation and its reproduction is difficult, and hence it is hard to debug the electrical timing fault.

There are many works that embed a sensor on a chip and use sensing results for run-time performance guarantees [1]–[5]. For power integrity verification, there are many proposals of on-chip noise sensors used for power grid analysis [6]–[9] and correlation analysis with timing failures [10]–[12]. On the other hand, for FPGAs, temperature is often measured by measuring ring oscillator frequency (such as [13]). The ring oscillator frequency also includes supply voltage information [14]. However, the ring oscillator tells us the average voltage while it is running, and cannot snap short-time voltage drops that cause electrical timing failures. Improved ring oscillator based sensors have been proposed in [15], [16]. However, they require repetitive noise production since they work as a sampling oscilloscope, and hence they cannot be used for detecting one-shot voltage drops. Thus, a sensor which can sense voltage fluctuation every clock cycle and can be integrated on VLSI/FPGA is highly demanded to obtain

helpful information for the debug of the electrical timing failure. In addition, such a sensor is also useful for detecting a suspicious operation and re-executing the operation similarly to [4]. Motivated by this, we developed a real-time supply voltage sensor which could be implemented both on VLSI and FPGA, and its performance on FPGA is reported in [17]. However, the performance on ASIC has not been presented.

In this work, we focus on power supply noise as a primary cause of electrical timing faults and propose a timing fault localization system with a supply voltage sensor which can perform one-shot and every-cycle sensing. The proposed sensor can provide clock-cycle-accurate voltage variation for detecting and debugging electrical timing faults and its performance on voltage resolution is demonstrated with 65nm test chip measurement. Also, the effectiveness of the proposed system is experimentally evaluated through simulations with an embedded processor running under power supply noise.

The rest of this paper is organized as follows. Section II explains the background of trace-based fault localization. Section III describes the structure and operation of the proposed sensor and measurement results of the sensor. Section IV outlines the proposed fault localization system and discusses the required performance. Section V shows experimental results for evaluating the proposed system. Concluding remarks are given in Section VI.

II. BACKGROUND

Trace buffer [18], which records circuit signals and status at every clock cycle, is widely used for electrical timing fault localization. By analyzing recorded information, electrical timing faults are localized. On the other hand, trace buffer involves additional area overhead and then area reduction of the trace buffer is highly desirable. To make the best use of the limited amount of trace buffer, trace buffer is overwriting old records and stops the recording once a suspicious event occurs [19]. When a trigger signal for stopping the recording is generated immediately after a fault occurs, the necessary depth of the trace buffer is small, and fault localization is efficiently carried out. Thus, the quality of the trigger generation is very important for both the area overhead and fault localization efficiency. In a previous research, logical events such as deadlock and segmentation fault on a processor are used as triggers [20]. With this method, however, the electrical timing faults can be recorded only when the fault influence appears as a logical event and it may take a long time for appearance. For

improving the quality of trigger signal, direct observation of dynamic events, which is the cause of electrical timing faults, could be helpful.

III. SUPPLY VOLTAGE SENSOR

This section first explains the structure and operation of the proposed sensor, and then shows measurement results.

A. Sensor Structure and Operation

Figure 1 depicts the proposed real-time supply voltage sensor that captures supply voltage every clock cycle consisting of a delay chain and a time-to-digital converter (TDC). Flip-flops (FFs) in the TDC are connected in parallel. A clock signal is guided to the delay chain and the clock line. The first positive edge (E1) and negative edge (E2) are given to the clock line and the delay chain, and the edges propagate through the delay chain. When the next positive edge (E3) is delivered to CLK terminal of FFs, the stage outputs of the delay chain are latched into the FFs. Here, N_{passed} , which is the number of FFs which E1 passed through, depends on the supply voltage because the propagation delay of each delay element in the delay chain is dependent on the supply voltage. The similar edge detection circuit is used in critical path replica [21]. The similar structure is used as a voltage noise sensor in some papers [11], [12], [22] published after our preliminary work [17]. An important point here is that all the circuit components are digital standard cells, and hence the proposed sensor is easy to implement and process portable. The proposed sensor can be implemented even on an FPGA [17].

We prepare a table indicating a relation between N_{passed} and the supply voltage beforehand. In the sensing, N_{passed} measured at each clock cycle is converted into the supply voltage by looking up the table. This table construction can eliminate process variation. Dynamic temperature fluctuation could give an offset between the actual supply voltage and the estimated voltage, but it should be noted that the impact of temperature on gate delay for super-threshold operation is quite limited [23] and more importantly the relation that larger N_{passed} represents higher supply voltage is unchanged. The similar discussion is valid for aging effects as well.

B. Measurement Results of proposed supply voltage sensor

We implemented the proposed sensor with 256-stage TDC on a 65-nm test chip. A chip photo is shown in Fig. 2. The chip size is 4.2 mm \times 2.1 mm. The sensor occupies 0.138% of the test chip. The other area is occupied by an embedded microprocessor.

We varied the supply voltage from 0.9 V to 1.4 V by 10 mV and evaluated N_{passed} . Figure 3 shows the voltage resolution of the proposed supply voltage sensor, which corresponds to the slope, is 3.9 mV. The proposed sensor gives precise noise information at every clock cycle. We can also see that the proposed sensor has a good linearity in a wide range of supply voltage. To validate the measurement result, we calculated

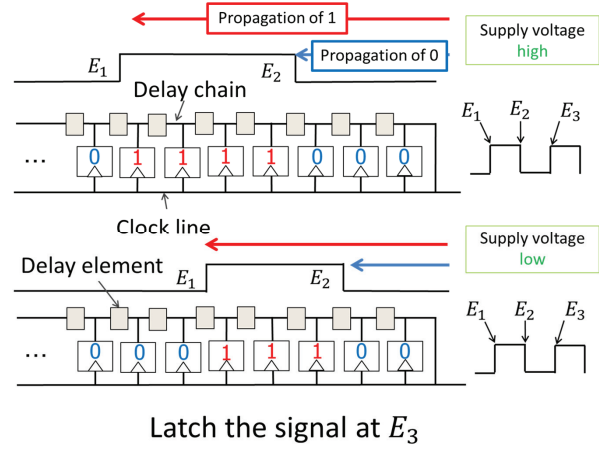


Fig. 1. Proposed real-time supply voltage sensor and its operation.

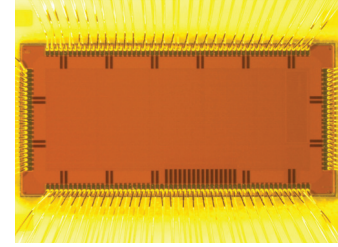


Fig. 2. Test chip.

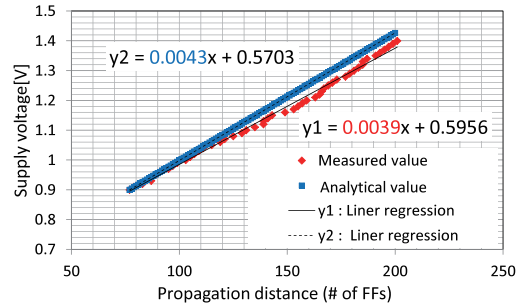


Fig. 3. Measured values and analytic estimates of proposed sensor.

the analytic estimate of the voltage resolution, which is given by [17]

$$\frac{1}{2} \left[\left\{ (V_{dd} - V_{th})^\alpha + \frac{2\beta}{T} \right\}^{\frac{1}{\alpha}} - (V_{dd} - V_{th}) \right]. \quad (1)$$

Here, $\alpha = 1$, $\beta = 3.0 \times 10^{-10}$, $V_{th} = 0.4$ and $T = \frac{1}{140 \times 10^6}$. The analytic estimates of Eq. (1) are well correlated with the measurement results in Fig. 3.

We also implemented the proposed sensor on an FPGA, where this implementation was reported in [17]. We used a custom Stratix III device board as a DUT (device under test) board. The proposed sensor implemented on the FPGA has 29mV voltage resolution. The proposed supply voltage sensor was used to sense the voltage fluctuation in a processor running, and the measurement result of the proposed sensor

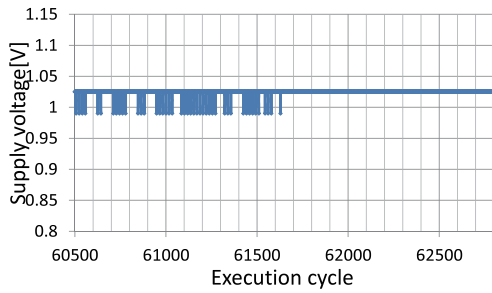


Fig. 4. Measured supply voltage fluctuation.

was compared with that of off-chip A/D converter on the DUT board. In this experiment, we used MIPS R3000 processor and CRC32 program was executed on the processor. Given 1.0V as an external supply voltage and 139.7 MHz as a clock frequency, the voltage sensing result of Fig. 4 was obtained. This result shows that the proposed sensor can observe the dynamic voltage fluctuation induced by processor running.

IV. TRACE-BASED FAULT LOCALIZATION SYSTEM WITH SUPPLY VOLTAGE SENSOR

The proposed trace-based fault localization system, which aims to facilitate the localization of electrical timing failures, consists of trace buffer, trigger generator and supply voltage sensor as shown in Fig. 5. In this system, the supply voltage measured by the sensor is given to the trigger generator and is used in the trigger generation logic as input signals. The measured voltage is also sent to the trace buffer and can be recorded as a clue of fault localization.

The following subsections explain the role and requirement of each component composing the fault localization system.

A. Trace buffer

Trace buffer aims to store the information which is useful for localizing electrical timing faults. Such useful information includes, for example, program counter and executed instruction. Both the width (number of recorded signals) and depth (recording length) of the trace buffer must be carefully minimized for area overhead reduction while the fault localization efficiency is maintained.

B. Trigger generator

As described earlier, the trigger signals stop recording to the trace buffer when events which might be relevant to fault occurrence. The quality of the trigger signal is evaluated as two metrics.

- Latency : Latency is defined as the time interval between timing fault occurrence and trigger activation. Shorter latency is desirable in terms of both trace buffer depth and localization facilitation.
- Number of trace analyses : Number of trace analyses corresponds to the number of traces to check if a timing fault is included until a trace captures the target timing

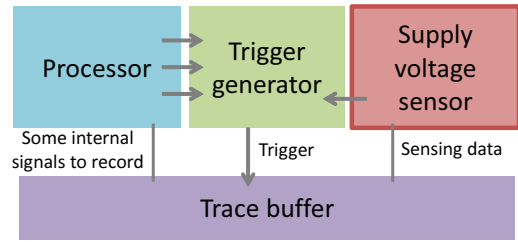


Fig. 5. Structure of the proposed fault localization system.

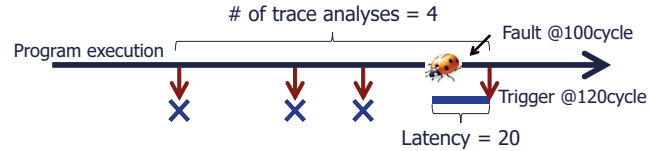


Fig. 6. Example of trigger quality metrics.

fault. Smaller number of trace analyses is desirable, since the fault localization can be completed in a shorter time.

Figure 6 exemplifies these two metrics. In this example, before capturing the fault in the trace buffer, the trace analyses are performed four times, and then the number of trace analyses is four. The latency from the fault occurrence and trigger generation is 20 clock cycles.

C. Supply voltage sensor

The supply voltage sensor is responsible for providing supply voltage information to the trigger generator and trace buffer. An electrical timing failure caused by supply voltage drops arises as a bit flip at a certain clock cycle. In order to investigate the correlation between supply voltage drops and timing failures, the supply voltage sensor should be able to measure cycle-by-cycle supply voltage fluctuation. In addition, the measured voltage information should be readily available for trigger generation. The proposed sensor presented in the previous section satisfies these requirements, and hence it is used for the fault localization system. Note that, in this paper, the output of the supply voltage sensor is supposed to be used for fault localization, but the sensor output can be also used to generate a retry signal suggesting a suspicious operation to re-execute [4].

A design issue is how many sensors are necessary and how they are placed. Related works can be found in, for example, [21], [24]. However, for the purpose of timing error localization, it has not been studied. We need to consider both spatial supply noise variation and critical path distribution. Addressing this issue is one of our future works.

V. FAULT LOCALIZATION PERFORMANCE

This section evaluates the fault localization performance in terms of the latency and the number of trace analyses.

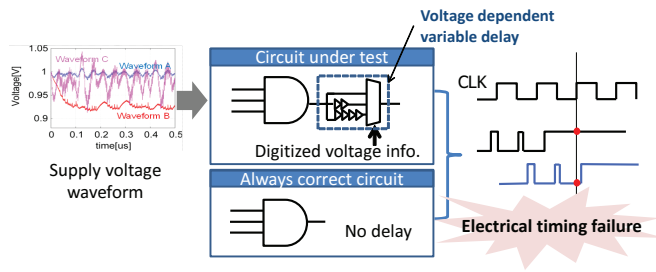


Fig. 7. Noise-aware logic simulation framework.

A. Evaluation environment

We compare fault localization performance between the proposed systems with and without the supply voltage sensor (Fig. 8). To reproduce noise-induced timing faults in a processor, we have implemented a simulation framework that can consider dynamic power supply noise in gate-level logic simulation (Fig. 7). The dependence of gate delay on supply voltage is expressed by a delay element whose delay is controlled by digital signals representing supply voltage, where this delay element is described in RTL. By attaching this delay element to every gate, we can reproduce voltage-dependent gate delay. In addition, we can dynamically change the gate delay by changing the digital signals that represents supply voltage. This simulation framework also simulates the RTL processor design concurrently and compares all the values in sequential elements every clock cycle, which tells us the exact location of the first timing fault. Here, the first timing fault means that we focus on the first timing fault occurred in a program running on the processor, and the second and later faults are not considered in the experiments.

We used TOSHIBA MeP processor as a CUT. This processor can recognize logical fault events such as hardware interrupt, zero division, non-existent instruction, etc. In addition, invalid memory access is included in logical fault events in this experiment. Three benchmark programs from MiBenchmark [25] (SHA1, CRC32, dijkstra) were used in this evaluation. As supply voltage fluctuations, we generated noise waveforms based on random walk, where the minimum and maximum voltages were set to 0.8V and 1.0V. Figure 9 shows an example of simulation results which include an electrical timing fault occurrence, and the occurrence time and supply voltage value at that time are presented in the figure. The electrical timing fault occurred when the voltage dropped to a low value of 0.823V.

B. Evaluation results

Using a data set consisting of programs to run on the processor and various noise waveforms, we evaluated the efficiency improvement in fault localization thanks to the supply voltage sensor. As a first step, in this work we chose a trigger setting whose activation condition was given by threshold value of supply voltage AND instruction executing in the CUT.

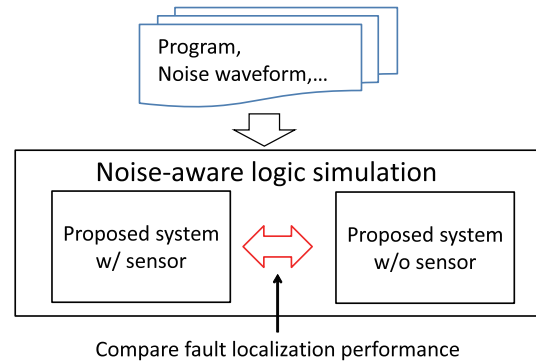


Fig. 8. Evaluation outline.

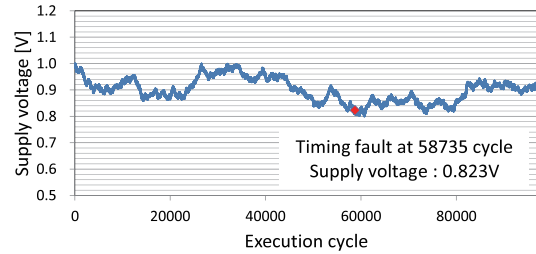


Fig. 9. An example of simulation result (dijkstra).

To have a better trigger setting, we selected instructions that were supposed to activate timing-critical paths. This instruction selection was carried out as follows. First, from the post-layout slack report generated by a P&R tool, the most timing-critical 20 paths were selected. Then, we performed a logic simulation at a frequency which was high enough to produce timing faults. Through this simulation, we identified top four instructions that produced the most timing faults in the selected 20 paths. For example, four instructions (ret, lw, sw, jmp) were selected from dijkstra program.

We evaluated the latency and the number of trace analyses under the trigger setting conditions in Table I. We gave six voltage trigger conditions. In the table, N/A means that trigger was not activated in the condition. As the voltage threshold value becomes lower, the number of trigger activations decreases. The instruction executions at higher supply voltage are less likely to cause timing faults, and these executions can be eliminated with the voltage threshold condition. In other results with different programs, the number of trigger activations follows a similar trend. As for the latency, we can see small values in the table. The smallest number is 2 in the case of "sw" instruction. In this test case, if we first try "sw" instruction, we can perform fault localization with very shallow trace buffer and the number of trace analyses can be reduced from 4,502 to 183 thanks to the supply voltage sensor. Thus, the proposed system with supply voltage sensor is effective for fault localization.

On the other hand, in this experiment, we did not observe any logical events which were relevant to fault occurrence in all three programs. This means that the trigger activation based on the suspicious logical events was not useful and no trigger

TABLE I
AN EXAMPLE OF THE TRIGGER EVALUATION (DIJKSTRA).

Voltage Condition	Instruction Condition							
	ret		lw		sw		jmp	
	# of trace analyses	Latency	# of trace analyses	Latency	# of trace analyses	Latency	# of trace analyses	Latency
Any	461	26	10,439	52	4,502	2	318	140
≤0.96 V	354	26	8,886	52	3,754	2	262	140
≤0.92 V	237	26	6,075	52	2,583	2	179	140
≤0.88 V	121	26	2,386	52	1,196	2	95	140
≤0.84 V	36	26	232	52	183	2	15	140
≤0.80 V	0	N/A	0	N/A	0	1,977	0	N/A

signals were generated. In this case, the fault localization must be carried out without any clues. To localize faults, we need to repeat logging by sweeping the timing of the log stopping from the beginning or end of the program until the trace buffer captures the timing fault. For example, supposing that trace buffer depth is 16, the number of trace analyses is 3671 (=58735/16) in the case of Fig. 9. On the other hand, with the trigger setting of "sw" and " ≤ 0.84 V", it becomes 183. The number of trace analyses is reduced to 1/20 in this example.

C. Effective trigger sweeping

In the fault localization process, we need to repeat trace buffer analyses with different trigger settings until the trace buffer captures the timing fault. When we set the trigger condition as voltage threshold AND instruction, we have two policies in the sweeping priority.

- Fix the instruction and change the voltage threshold first.
- Fix the voltage threshold and change the instruction first.

With these policies, we calculated the number of trace analyses before the trace buffer captured the timing fault.

In this evaluation, we used the result of dijkstra program as an example for the calculation. We swept the voltage threshold from the lowest value. The order of instructions applied to the trigger condition was "ret, lw, sw, jmp". This instruction order is decided by the frequency of timing violation in the preliminary evaluation mentioned before. Table II shows the total number of the trigger activation while dijkstra program was running. The number of trace analyses were calculated with Tables I and II.

We assume two cases of trace buffer depth, 100 and 2. First, the trace buffer depth is 100. The numbers of trace analyses are 38 with policy (a) and 41 with policy (b), and they are comparable. Next, let us consider the situation that trace buffer depth is 2. Then, the numbers of the trace analyses become 56,879 with policy (a) and 2,090 with policy (b). In this case policy (b) is superior, i.e. we should change instruction condition first before raising the voltage threshold.

VI. CONCLUSION

In this work, we proposed a timing fault localization system with a supply voltage sensor which can provide voltage variation every clock cycle for detecting and debugging electrical

TABLE II
TOTAL NUMBER OF TRIGGER ACTIVATION THROUGHOUT THE PROGRAM EXECUTION (DIJKSTRA).

Voltage Condition	Instruction Condition			
	ret	lw	sw	jmp
Any	793	17,503	7,642	551
≤0.96	686	15,950	6,894	495
≤0.92	520	12,365	5,362	383
≤0.88	280	6,685	3,105	234
≤0.84	61	1,839	941	70
≤0.80	0	0	0	0

timing faults. The performance of the sensor was evaluated on an FPGA and a 65-nm test chip. The measured voltage resolution on test chip was 4mV. Given the supply voltage sensor, we evaluate the effectiveness of the proposed timing fault localization system. Experimental results show that the supply voltage observed by the proposed sensor can produce clues of timing fault and improve the efficiency of the timing fault localization. This work evaluated the primitive trigger conditions only, and our future work will evaluate more complex trigger conditions with a number of test programs.

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