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Modeling the Effect of Global Layout Pattern on Wire Width Variation for On-the-Fly Etching Process Modification

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SUMMARY As the technology of VLSI manufacturing process continues to shrink, it becomes a challenging problem to generate layout patterns that can satisfy performance and manufacturability requirements. Wire width variation is one of the main issues that have a large impact on chip performance and yield loss. Particularly, etching process is the last and most influential process to wire width variation, and hence models for predicting etching induced variation have been proposed. However, they do not consider an effect of global layout variation. This work proposes a prediction model of etching induced wire width variation which takes into account global layout pattern variation. We also present a wire width adjustment method that modifies etching process on the fly according to the critical dimension loss estimated by the proposed prediction model and wire space measurement just before etching process. Experimental results show that the proposed model achieved good performance in prediction, and demonstrated that the potential reduction of the gap between the target wire width and actual wire width thanks to the proposed on-the-fly etching process modification was 68.9% on an average.
key words: *etching, manufacturability, modeling variability*

1. Introduction

As VLSI process node continues to shrink, the systematic manufacturing variation is becoming significant and its impact on performance and yield loss is increasing prominently. Wire width and height variation is one of such systematic variations, and it is gaining its importance because wire delay contribution to the total delay is increasing [1]. Wire width and wire height control is a key factor to achieve high performance and yield enhancement.

Chip fabrication includes manufacturing test which judges whether a chip has defects or not, and the manufacturing test occupies a considerable portion of chip fabrication cost [2]. To reduce the test cost, wafer level screening is often used in manufacturing test [3]. In this screening, a common test structure is placed on scribe lines in a wafer (Fig. 1) and electrical characteristics of the test structure are measured before all individual chips on the wafer are tested. If an outlier value is found in the measurement of the common test structure, the wafer is discarded. It is because the number of faulty chips on such a wafer is empirically much larger than those on other wafers.

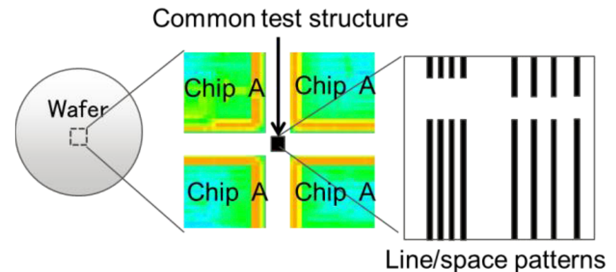

Fig. 1 Common test structure on a wafer.

For checking the result of wiring processes, wire resistance is often measured in the wafer level screening. If the systematic variation of wire resistance originated from only process conditions and local test structure layout, there should be no resistance difference regardless of the chip layout on a wafer. However, a certain difference in wire resistance value was observed in the measurement data of the test structure with various chip layouts. This means that the process forming wire metal pattern is affected by global layout which consists of the surrounding layout in a certain range around the test structure.

Lithography, etching, and chemical mechanical planarization (CMP) are main manufacturing processes that shape copper metal wire. Lithography is a process printing chip layout patterns on a wafer. In recent sub-wavelength technologies, diffraction phenomenon causes wire shape distortion and consequent wire width variation. To cope with the wire shape distortion, resolution enhancement techniques (RET), such as optical proximity correction (OPC), sub-resolution assist features (SRAF) and phase shift mask (PSM), are widely used [4]–[6]. Etching is a process to remove materials from the surface of a wafer according to the printed photoresist pattern and dig interconnect trench. This process affects the profile of trench, in which high aspect ratio with straight sidewall structure is usually required [7]–[9]. CMP is a process to remove redundant metal which was deposited in electro-chemical plating (ECP) process, and it planarizes the upper surface of wire metal. Proper CMP process contributes to wafer surface uniformity and reduces wire height variation [10]–[13].

CMP process, however, leaves a certain amount of wire height variation depending on global layout pattern.

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To mitigate the wire height variation, some CMP prediction methods and optimization methods have been proposed [12]–[14]. Etching process also affects wire height non-uniformity originating from trench depth variation, but its impact is small thanks to etch stop layer (ESL) technique which prevents over-etching [15]. On the other hand, wire width variation depends on lithography and etching processes. Both the processes are affected by global layout pattern as well as local test pattern [6], [9], [16]. Here, local layout pattern is defined as a wire of interest and its adjacent objects, and global layout pattern is defined as features abstracted from a wire of interest and its surrounding layout within a certain range. Lithography simulation can predict the shape of interconnect accurately, but it is too costly for full chip analysis. Thus, several heuristic prediction methods whose execution time is acceptable are proposed [16]–[18].

To achieve desired wire widths in fabrication, etching process prediction is more important than lithography process prediction. This is because the variation occurred in lithography process can be compensated by adjusting successive etching process parameters, such as gas flow, wafer temperature, and etching time as long as etching process can be correctly simulated. For such a purpose, there are some methods that predict etching induced wire width variation in consideration of local layout pattern [19]–[24]. However, these do not take into account global layout pattern. Another approach is a feedback control through an iteration of fabrication, measurement and process modification [25], [26], but it takes a longer time and costs wafer loss before the process is stabilized.

Aiming to mitigate wire width variation, we developed a prediction model of etching induced wire width variation that considers global layout variation. In addition, we propose a method that adjusts wire width through on-the-fly etching process modification.

Contributions of this work include the followings:

- This is the first work to develop a model that predicts etching induced wire width variation taking into account an effect of global layout pattern variation. To achieve high accuracy, we calibrate model parameters with measured data of industrial chips.
- We proposed a wire width adjustment method with the prediction model. This adjustment method can reduce the wire width variation by compensating lithography and prospective etching induced variations with instant etching process alternation.
- We assessed the accuracy of the prediction model and effectiveness of the proposed adjustment method with industrial chips.

The rest of this paper is organized as follows: Sect. 2 reviews etching process and defines the wire width variation problem occurring in etching process. In Sect. 3, we introduce a prediction model for wire width variation and explain how to adjust wire width using the prediction model. Section 4 presents experimental results. Finally, Sect. 5 concludes this paper.

2. Overview of Etching Process

This section reviews etching process. In the fabrication process of ultra large integrated circuits, reactive-ion etching (RIE) is widely used [7], [9]. Figure 2 illustrates an RIE system. RIE is a kind of dry etching method using gas glow discharge plasma, where the plasma is maintained with RF power. The plasma dissociates and ionizes feed gases (e.g. C_xF_y for SiO_2 etching) in a vacuum system and generates free radicals and positive ions as etch species, which react with the material of the wafer surface.

Free radicals are main reactive species of etching process. Radicals, which are electrically activated neutral species, are diffused and adsorbed on the wafer surface, and they finally react with the wafer surface materials.

Energetic gas ions are other key species of etching mechanism. A wafer is located on a cathode electrode and acquires negative charge because electron mobility is higher than ion mobility. Positive ions drift toward the wafer and they collide with materials on the wafer surface. Some ions react with the materials chemically, and others cause physical sputtering.

Synergism of ion bombardment and chemical reaction give a high etching rate [27], which is an advantage of RIE process. The etching rate of the wafer exposed to ion and radical fluxes simultaneously is much higher than that of the wafer exposed to each flux separately. Ion bombardment helps remove reaction product of wafer surface and accelerates another surface reaction of free radicals, which results in the higher etching rate.

In etching process, there are two important factors to control wire trench profile. The first is selectivity, which is the etching rate ratio of a target material to other materials. In chip fabrication, wafer surface is covered by photoresist pattern, and ESL at the bottom of trench prevents over-etching. To remove only the exposed potions of SiO_2 prop-

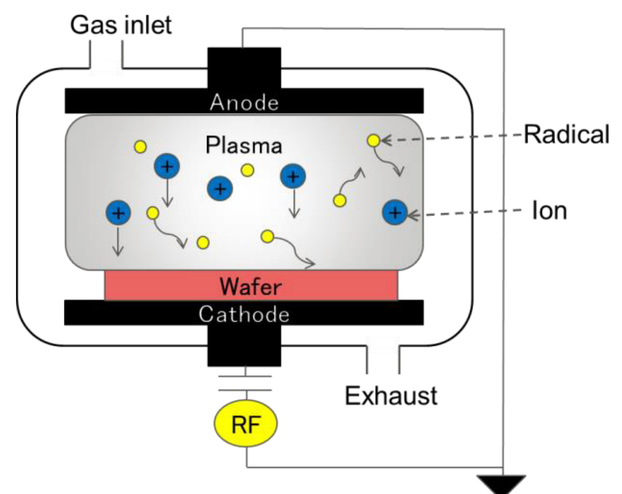

Fig. 2 Overview of RIE system.

erly, high selectivity to both photoresist and ESL materials is required. Radical etching is generally more selective than ion etching because physical sputtering in ion etching process is less dependent on the materials. Secondly, anisotropy determines the shape of wire trench. Anisotropy is the directionality of etching process, and it is opposed to isotropy. Anisotropic and isotropic etching is illustrated in Fig. 3. Ion etching process is highly anisotropic because ion flux has a direction vertical to the wafer surface. Radical etching, on the other hand, is an isotropic process because free radical is electrically neutral and has the same etching rate in every direction.

In RIE process, highly anisotropic etching is accomplished thanks to sidewall protection mechanism (Fig. 4) [9], [28]. SiO_2 and photoresist materials output both volatile gaseous reaction products and solid polymer reaction products. The polymer products redeposit on the surface and form a polymer film layer. This polymer film plays an important role as an inhibitor to protect the surface from radical etching. Note that only sidewalls of the trench are covered by the polymer film because they are not exposed to ion bombardment which can remove the polymer deposition. Thus, sidewalls are protected from etching, and RIE process becomes more anisotropic.

The sidewall protection mechanism has a great effect on the wire width variation because the horizontal etching rate heavily depends on the thickness of the sidewall polymer film. This mechanism can be related to many parameters, such as the amount of free radicals, the ratio of etchable area and photoresist area, and etching rate. An important point here is that those parameters are affected by global layout variation [8], [9]. This work focuses on the sidewall protection mechanism as a major factor of wire width variation in etching process and studies the modeling of wire width variation originating from this mechanism.

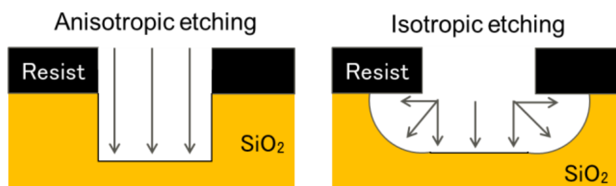

Fig. 3 Anisotropic and isotropic etching.

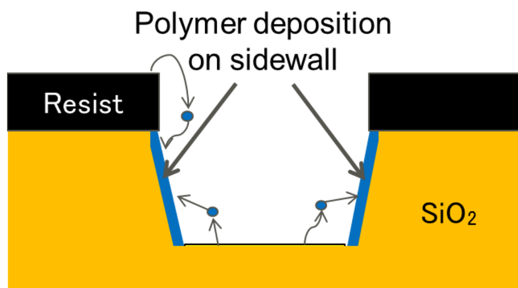

Fig. 4 Sidewall protection.

3. Prediction and Mitigation of Wire Width Variation

This section proposes a prediction model of wire width variation, which can be applicable to a variety of chip layouts on a wafer. To achieve high accuracy of the model, the proposed model calibrates its model parameters using the measured data of various industrial chips. This section also describes a method to mitigate wire width variation with on-the-fly etching process modification.

3.1 Definitions

In the manufacturing process used in this study, a common test structure is placed at a fixed location on a wafer for monitoring wire width variation. Wire widths of test patterns in the structure are measured twice; before and after etching process. The former measured value is called development inspection critical dimension (DICD) and the latter is called final inspection critical dimension (FICD). Here, we define a parameter "etching bias" Δw as the difference between DICD and FICD, and a parameter "Critical Dimension (CD) loss" g as the difference between target wire width w_t and FICD.

$$\Delta w = FICD - DICD, \tag{1}$$

$$g = FICD - w_t. \tag{2}$$

Figure 5 shows the relationship between DICD, FICD and target wire width. To obtain a wire profile with no CD loss ($g = 0$), etching bias Δw should be equal to the difference between target wire width and DICD ($\Delta w = w_t - \text{DICD}$). On the other hand, DICD varies wafer by wafer due to lithography process. If we can tune the etching process to satisfy $\Delta w = w_t - \text{DICD}$ for every wafer, the CD loss can be minimized.

The proposed wire width adjustment method, which will be explained in Sect. 3.3, alters etching process to satisfy $\Delta w = w_t - \text{DICD}$ aiming at $g = 0$. Here, DICD can be obtained by measuring the common test structure on the wafer before the etching process. The target wire width w_t is also available. On the other hand, it is difficult to obtain

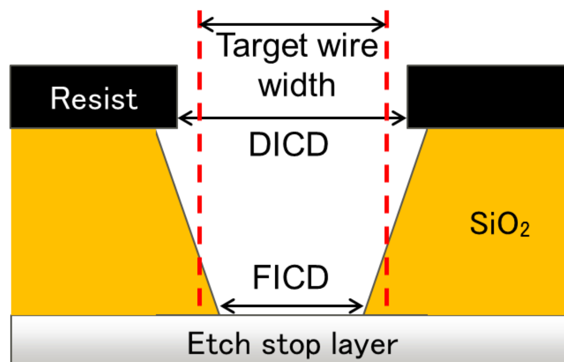

Fig. 5 Relationship between DICD, FICD and target wire width.

the tuned etching process that satisfies $\Delta w = w_t - \mathrm{DICD}$ directly. Therefore, we first estimate the CD loss if normal etching process is performed. Then, the etching process is slightly modified to eliminate the estimated CD loss, and the modified process is applied to the wafer. Note that every manufacturer empirically knows how much trench width would change when the etching process is modified. However, there are no models that estimate the absolute value of Δw that varies depending on global layout pattern. We thus developed a model for estimating Δw in case of normal etching process. This developed model will be explained in the next subsection.

3.2 Proposed Prediction Model

The proposed model predicts etching bias Δw that occurs depending on global layout pattern. The proposed model is derived from four qualitative properties below.

a. Etching bias is proportional to the thickness of sidewall polymer film.
The polymer film deposited on sidewalls prevents the sidewalls from being etched by isotropic free radical etching. Therefore, the thicker the film grows, the smaller the trench width, i.e. the wire width, becomes.

b. Thickness of sidewall polymer film is affected by the ratio of etchable area to the total area.
The sidewall polymer is composed of the products from substrate material (e.g. $Si_xH_yF_z$) and from photoresist material (e.g. $C_xH_yF_z$) [9]. On the other hand, the redeposition rate to the surface and etching prevention strength are different between these materials [29]. Due to that, the etchable wire area (substrate material) to the total area (substrate and photoresist materials) has an influence on the thickness of the sidewall polymer film and the consequent etching prevention ability.

c. Thickness of sidewall polymer film is also affected by the total edge length.
Here, edge length is defined as the wire perimeter. Supposing the amount of generated polymer materials is fixed, the polymer film becomes thicker when the total sidewall area in which the polymer materials are redeposited is small. Besides, the sidewall area is the product of the edge length and the trench depth, and hence to the sidewall area is proportional to the edge length.

d. Parameters are calculated in the area within the range of effective length.
We assume that reaction products scattered from a certain point is redeposited within a fixed range from that point. This is reasonable since the reaction products tend to be redeposited before they are diffused distantly. As a result, the reaction products and the sidewall area out of the range have little effect on the redeposition process at the point of interest. To deal with this assumption, we introduce a parameter called "effective length."

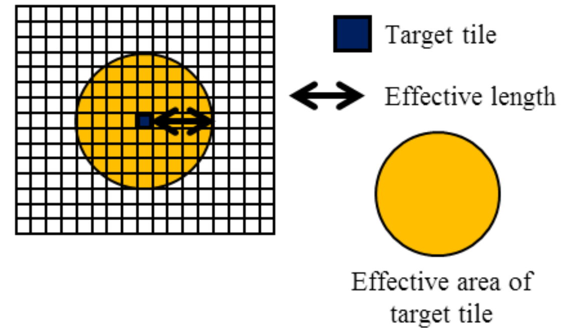

Fig. 6 Region for parameter $\bar{m}$ calculation.

According to the above qualitative properties, we propose a prediction model:

$$\Delta w = \alpha \cdot \overline{m}, \tag{3}$$

$$m = d^{\beta} \cdot e^{\gamma}, \tag{4}$$

where Δw is the etching bias at a point of interest and $\bar{m}$ is the average of multiplication parameter m within the effective length L. d is local wire area density, e is local total edge length, and α, β, and γ are calibration parameters. Parameter α, β, γ, and effective length L are calibrated using etching bias data of industrial chips measurement.

The average computation in Eq. (3) includes numerical integration. To efficiently compute Eq. (3), a whole chip is discretized into small tiles and related parameters are extracted and recorded for each tile, which helps reduce the size of database and calculation cost. Namely, layout parameters necessary for the prediction of wire width variation, i.e. d and e, are extracted for every tile from the original chip data. Consequently, wire width variation is predicted for each tile.

Figure 6 illustrates $\bar{m}$ calculation with discretized tiles. Using effective length L, we compute $\bar{m}$ of the target tile as an average of parameters m of the tiles within the range of effective length from the target tile.

3.3 On-The-Fly Wire Width Adjustment via Etching Process Modification

Given the prediction model presented in the previous subsection, we can now predict wire width variation that occurs depending on global layout pattern. We next explain how CD loss can be mitigated using the prediction model.

Figure 7 shows the procedure of wire width modification. Now, we have a new wafer whose lithography process is completed but whose successive etching process is not completed. This successive etching process is modified based on the CD loss estimated by the proposed prediction model of etching bias and measured DICD of the common test structure on the wafer after lithography process. This etching process modification is performed for every wire layer.

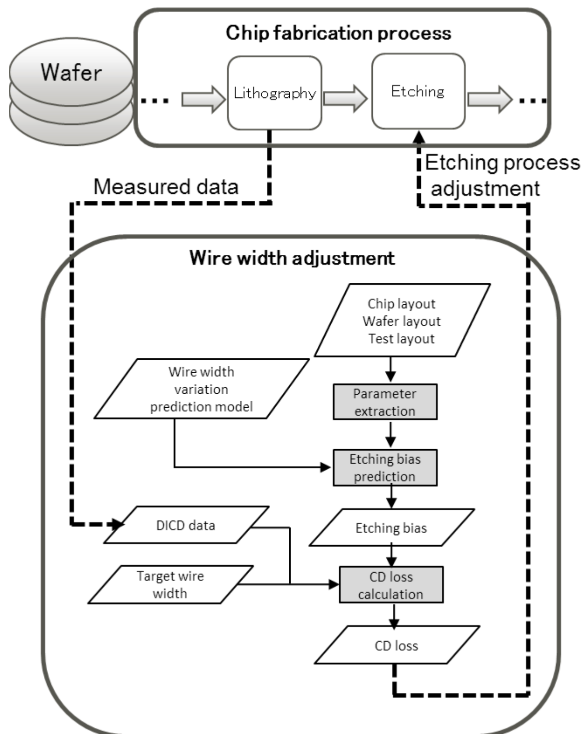

Fig. 7 Procedure of on-the-fly wire width adjustment via etching process modification.

Firstly, parameters d and e are extracted from the layout data. Here, the target tile is the tile in which the common test structure is located, and layout parameters of each tile within the range of effective length are extracted using layout data of chip, wafer and common test structure. Then, etching bias Δw is calculated with these parameters and the proposed prediction model of Eqs. (3) and (4). Note that the prediction model has been already calibrated with calibration data. Next, CD loss g of target tile is calculated with this prediction result of Δw, measured DICD and target wire width w_t using Eqs. (1) and (2). In this way, we can predict CD loss g of the test pattern in case that normal etching process is applied. Then, we adjust etching process such as etching time or gas flow rate, to eliminate the estimated CD loss of the test pattern. This adjusted etching process is applied to the wafer.

4. Experimental Results

We first present experimental results to validate the accuracy of the proposed model. We obtained 36 etching bias data which came from 8 chip designs for model parameter calibration. In addition, we used other 29 etching bias data from 7 chip designs to validate the efficiency of the proposed model to unknown data. Note that each wafer was covered by one of the 15 (= 8+7) chip designs and one etching bias data corresponds to a wire layer of each chip design. Each etching bias data is an average of the values measured with multiple wafers. Calibration parameters α, β, γ and effective length L in the proposed model were calibrated with these data to minimize the root mean square value between measured data and estimated value. The tile size has an impact on a trade-off relation between computational cost and estimation accuracy. In this work, the tile size was set to $10 \times 10\,\mu$m. This size was much smaller than effective length L of $2000\,\mu$m, which will be investigated later, and numerical integration for $\bar{m}$ is be expected to be reasonably accurate.

Table 1 Details of calibration/validation chip designs.

Chip name	Chip size (mm)	# of layers	# of wafers	Average wire density (%)
Calibration chip designs				
A	21.3x20.8	4	133	26.3 - 33.1
B	7.8x7.8	4	52	30.1 - 42.6
C	13.3x10.0	4	37	25.5 - 54.4
D	8.0x6.4	4	445	31.3 - 43.0
E	8.5x8.5	4	67	31.1 - 50.5
F	7.8x8.4	5	56	35.3 - 45.1
G	9.4x9.4	6	42	26.4 - 32.2
H	9.8x8.8	5	12	34.9 - 46.5
Validation chip designs				
I	9.9x9.9	4	200	32.7 - 46.5
J	6.9x8.2	4	40	29.8 - 42.6
K	6.9x6.9	4	30	30.6 - 43.5
L	9.0x6.0	4	96	29.0 - 41.4
M	7.9x8.1	4	72	29.2 - 41.0
N	18.2x18.1	4	18	24.9 - 39.7
O	12.1x11.0	5	14	35.2 - 46.1

Table 1 shows an overview of all chip data. All the chips were manufactured with the same 65 nm technology node. Each layer of a chip has different average wire density values. “Average wire density” column denotes upper and lower bounds of these values. For all the wafers listed in Table 1, FICD and DICD of the common test structure were measured. This measurement data was used for calibration and validation purposes. Note that another calibration is needed if technology node is changed. In this paper, we use the coefficient of determination R^2 as a metric to evaluate the accuracy of the prediction model.

Figure 8 shows the accuracy of the model after the calibration process. Horizontal and vertical axes indicate estimated etching bias and measured etching bias, respectively. This result shows that FICD value is smaller than DICD in the technology node used for this experiment since etching bias values are negative. R^2 value was 0.71 and this model achieved good performance in prediction.

Besides, calibration parameters α, β, and γ were -0.0934, -0.259, and -0.341 respectively. This calibration result indicates that, if wire area density d, i.e. the etchable area within effective length, increases, etching bias Δw increases and therefore FICD value increases. This means that the ability of sidewall etching prevention degrades as the rate of polymer products from substrate material to total sidewall layer component becomes higher. The calibration result also shows that an increase in edge length e results

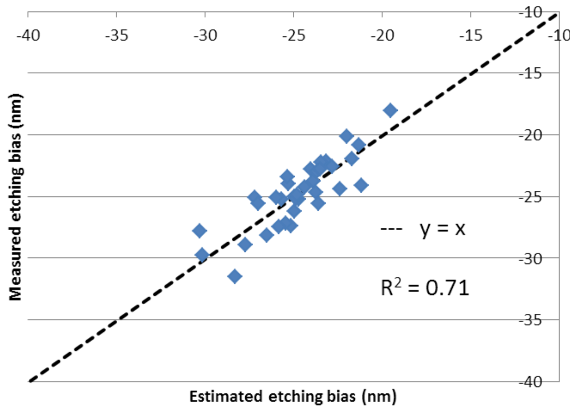

Fig. 8 Estimated etching bias vs. measured etching bias for calibration data.

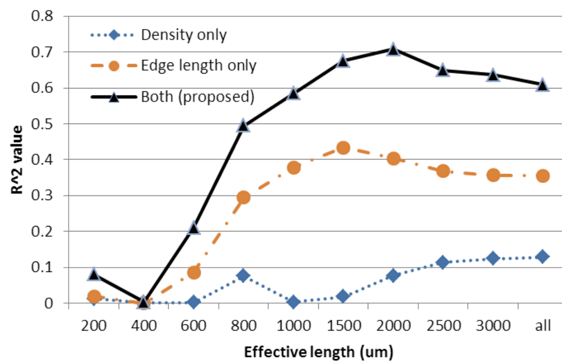

Fig. 9 Model calibration results with various effective lengths.

in an increase in both etching bias Δw and FICD. This is because sidewall thickness is inversely proportional to the sidewall area and affects the protection mechanism from isotropic etching.

Figure 9 shows R^2 index with various effective length values. "All" in x-axis means that the calibration was carried out supposing the effective length L was infinity. In this experiment, we performed the calibration for three models.

- M1: Proposed (Eq. (4)); both density and edge length are considered.
- M2: Density only ($m = d^{\beta}$); only density is considered.
- M3: Edge length only ($m = e^{\gamma}$); only edge length is considered.

We first examine the result of the proposed model (M1). The best performance was obtained in the case that L was 2000 μm. The edge bias was affected by the layout in a circle whose radius is 2000 μm, and the layout pattern in such a large area must be considered for the edge bias estimation. The effective length of 2000 μm was used for other experiments throughout this paper. We next compare the results of M1, M2 and M3. We can see that M1 attained the highest R^2, which clarifies that both density and edge length affect the etching bias mechanism. The figure also shows that the edge length e had a stronger impact on etching bias than density d.

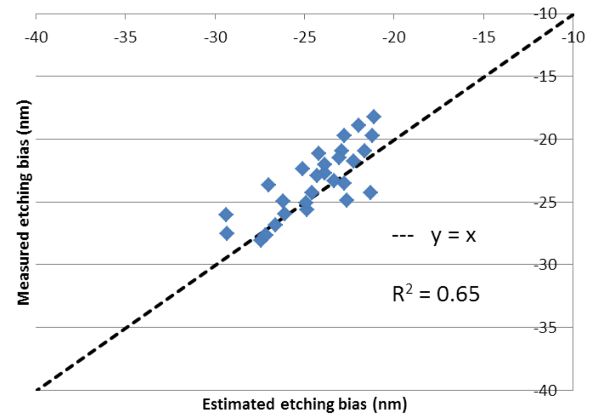

Fig. 10 Estimated etching bias vs. measured etching bias for validation data.

Table 2 CD loss value of validation chips.

	Original data (nm)	Proposed method (nm)	Improvement (%)
RMS	6.0	1.9	68.9
sigma	2.8	1.7	40.9

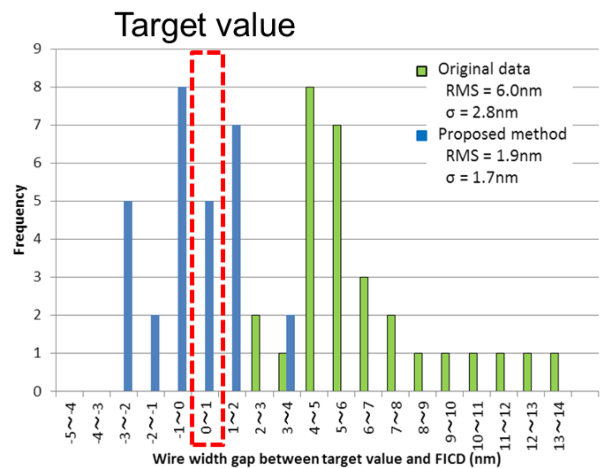

Fig. 11 CD loss distribution of validation chips.

Figure 10 shows the prediction results for the validation chip data. R^2 value of 0.65 was obtained, which confirmed that the proposed model maintained high accuracy even when unknown data was given.

Finally, we estimate how much the CD loss can be potentially reduced by the proposed on-the-fly wire width adjustment. In this evaluation, we assumed that the CD loss estimated using the proposed prediction model could be completely eliminated by etching process modification. Therefore, the CD loss reduction presented in the following corresponds to the maximum value in a case that the etching process modification to increase/decrease Δw is perfect. Table 2 shows root mean square (RMS) values and sigma values of CD loss with and without the proposed wire width adjustment. Here, the etching bias data of validation chips was used. Figure 11 shows the CD loss distributions. When

the proposed wire width adjustment was applied, RMS of CD loss was 1.87 nm and sigma value was 1.66 nm. Compared with the result without adjustment, we could reduce RMS of CD loss by 68.9% and sigma of CD loss by 40.9%. The CD loss distribution moved toward zero and the spread became tighter.

5. Conclusion

In this paper, we proposed a model that predicted wire width variation occurring depending on global layout pattern variation. We also presented a wire width adjustment method that tuned the etching process on the fly using the proposed prediction model and the measured DICD of the common test structure on the wafer. Experiments showed that the proposed model achieved good performance in prediction, and we could reduce the CD loss between the target wire width and FICD value by 68.9% on an average.

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