Characterizing Alpha- and Neutron-Induced SEU and MCU on SOTB and Bulk 0.4-V SRAMs

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***Abstract*—We experimentally characterized and compared the soft error rates of 65-nm bulk and silicon on thin buried oxide (SOTB) SRAMs by conducting accelerated alpha and neutron irradiation tests. Measurement results show that an SOTB SRAM has better soft error immunity than a bulk SRAM. In particular, the number of 2-bit multiple cell upsets (MCUs) of SOTB SRAM was smaller by two orders of magnitude than that of bulk SRAM, and the number of 3-bit or larger MCUs decreased further. In addition, the reverse body bias (RBB) reduced the soft error rate of SOTB SRAM to two-thirds of zero body bias (ZBB). To investigate this dependence on body bias, we evaluated the sensitive cross sectional area for ZBB and RBB with 3D technology computer aided design device simulations. The simulation results show that the RBB decreases the sensitive cross-sectional area of an SOTB device for small linear energy transfer (LET) ions, which is consistent with the measured dependence on body bias.**

***Index Terms*—Alpha particle, body bias, bulk, multiple cell upset, neutron, silicon on insulator (SOI), single event upset, soft error, thin buried oxide.**

I. Introduction

SILICON ON INSULATOR (SOI) is a promising device to mitigate the elevating power consumption of large-scale integration (LSI) since SOI is suitable for lower-voltage operation compared to conventional bulk devices [1]. Especially, fully depleted SOI (FD-SOI), whose channel region is thinner and more depleted than conventional partially depleted SOI (PD-SOI), has been developed to achieve lower voltage operation [2]. Moreover, a silicon on thin buried oxide (SOTB) device (as depicted in Fig. 1), which is a FD-SOI device, has better threshold voltage (V_{th}) controllability with body biasing by thinning the insulator layer (buried oxide; BOX) under the channel region [6], [7]. The thickness of the BOX layer in SOTB devices is 10-nm while other SOI devices often have BOX layers thicker than 100–nm [8], [9], [10]. The SOTB device is designed for pursuing 0.4-V operation while maintaining its speed performance with aggressive body biasing. Ishibashi *et al.* exploited these SOTB characteristics for implementing an extremely energy efficient CPU [11].

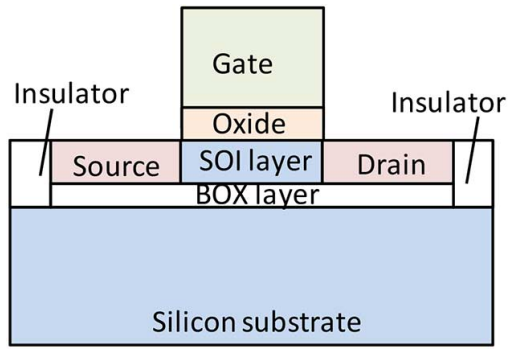

Fig. 1. Cross section of SOTB transistor.

Alpha-and neutron-induced soft errors become a primary reliability issue in terrestrial environments [12]. When pursuing low-voltage operation, the soft error rate (SER) increases as supply voltage decreases because critical charge, which is the charge threshold to cause a soft error, decreases [13]. For body biasing, it has been reported that alpha-induced SER at low voltage is less affected by body voltage in bulk complementary metal-oxide-semiconductor (CMOS) technology [14]. On the other hand, it is generally said that SOI devices are more robust than conventional bulk devices because the sensitive volume, in which charge generation causes a soft error, is small [8], [15], [16]. In particular, the radiation effects on FD-SOI devices have been studied in terms of single-event effects and the total doze effect for alpha, neutron, heavy ion and gamma irradiation [3], [4], [5].

However, SOTB devices have very thin BOX layers ($\sim$ 10 nm) for improving V_{th} controllability with the body bias [7], [17]. In other words, SOTB devices have weaker isolation between the SOI layer and substrate than conventional SOI devices, and the potential variation in the substrate affects the transistor characteristics through the capacitive coupling between the silicon substrate and SOI layer, which might make SOTB devices have larger sensitive volume than conventional SOI devices.

We need to clarify whether SOTB devices at 0.4–V operation have sufficiently low soft error sensitivity since the sensitivity of such devices to radiation has not been evaluated. For this purpose, Kobayashi *et al.* recently reported that SOTB flip-flop was robust compared to bulk flip-flop, and the SER of popular transmission gate based flip-flop with SOTB devices was 1/15 times lower than that of bulk devices [18]. On the other hand, in recent

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system-on-a-chip (SoC) and microprocessors, most of the silicon area is consumed by SRAM, and SRAM SER dominantly determines the chip-level SER. Therefore, before putting SOTB devices to practical use, the soft error immunity of SRAM must be characterized.

First, we experimentally characterized and compared the soft error immunity of bulk and SOTB SRAMs by conducting accelerated alpha and neutron irradiation tests. Bulk and SOTB test chips, which included 6T SRAM macros, were fabricated from the same layout data in a 65-nm CMOS technology. Experimental results show that the number of measured single-event upsets (SEU) on the SOTB SRAM at 0.4 V was 5.0 and 4.4 times larger than that at 1.0 V in alpha and neutron irradiation tests, respectively. On the other hand, the number of SEUs at 0.4 V on the SOTB SRAM was 0.22 and 0.08 times smaller than that on the bulk SRAM at 0.4 V, which confirms that the soft error immunity of the SOTB SRAM is superior to that of the bulk SRAM. We also confirmed that the number of measured multiple cell upsets (MCU) on the SOTB SRAM at 0.4 V was two orders of magnitude smaller than that on the bulk SRAM. Furthermore, we observed that reverse body bias (RBB) reduced the alpha- and neutron-SERs of the SOTB SRAM. Second, we investigated the dependence of the SER on body bias observed in the SOTB SRAM through 3D technology computer aided design (TCAD) device simulation. The simulation results showed that the sensitive region of the RBB was smaller than that of zero body bias (ZBB) for ions with smaller linear energy transfer (LET), which is consistent with the measured dependency of SER on body bias.

The rest of this paper is organized as follows. Section II describes the experimental setup for irradiation tests. Section III shows the measurement results of the alpha and neutron irradiation tests on SOTB and bulk SRAMs. Section IV presents TCAD device simulations to investigate the SER dependence on body voltage, and Section V gives concluding remarks.

II. Test Setup

Two test chips of SOTB and bulk devices were fabricated in a 65-nm CMOS technology with eight metal layers from the same Graphic Data System (GDS) data. A major difference between SOTB and bulk devices is the existence of the BOX layer under the channel region. Fig. 2 shows a micrograph of the SOTB test chip. The die size is about 36 mm^2. Both test chips include 24 SRAM macros, and each SRAM macro consists of a memory array, which includes traditional 6T SRAM cells, read/write circuitry, control unit, and data/address shift registers. Fig. 3 shows the layout of the 6T SRAM cell designed according to the logic design rule. The bit-cell dimensions are 0.56 μm $\times$ 2.6 μm. For reference, the bit-cell dimensions of a SRAM cell designed in the same 65-nm technology according to the SRAM design rule is 0.54 μm^2 [7]. In both SOTB and bulk SRAMs, the SRAM area is covered by a deep N-well. Then, the P-well in the SRAM area is isolated from the P-substrate. Therefore, the N-well and P-well voltages can be controlled independent of the supply and ground voltages.

We evaluated the SER during hold operation. As the supply voltage decreases, the SRAM cells start failing to hold their

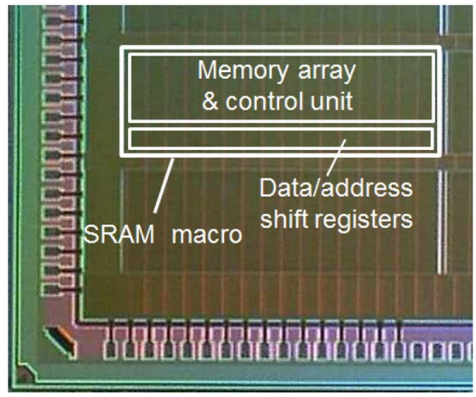

Fig. 2. Micrograph of 65-nm SOTB SRAM.

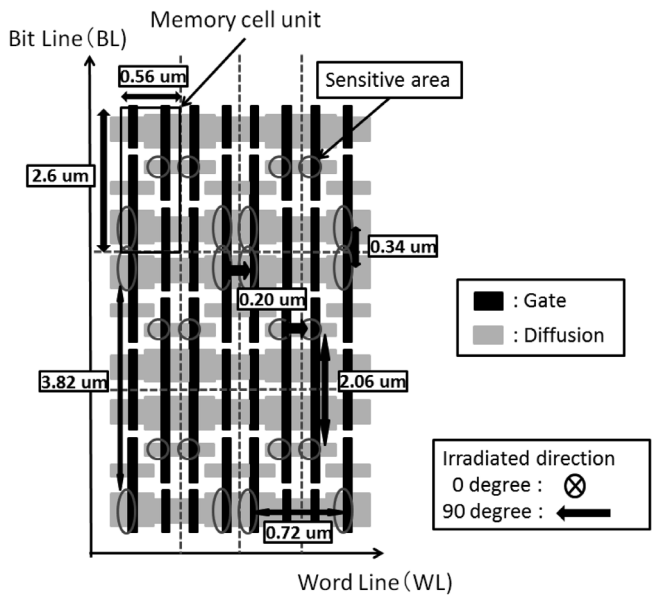

Fig. 3. Layout of 6T SRAM cells.

TABLE I
Supply and Body Voltages for Hold Operation Tests and Number of Failure Bits Per Chip

Supply voltage	Body voltage	# of failure bits	
		Bulk	SOTB
0.40 V	ZBB	429	79
0.40 V	RBB	367	123

values due to the V_{th} imbalance between the P-channel MOS (PMOS) and N-channel MOS (NMOS) transistors. This V_{th} imbalance is induced due to within-die process variation. Therefore, their impact on SRAM cells increases as the supply voltage approaches V_{th} [6]. To distinguish such failure bits from soft errors, hold operation was first tested for every SRAM cell. The failure bits were excluded from the soft error evaluation. Table I lists the sets of supply and body voltages at which the hold operation tests were conducted and the number of failure bits per chip. Here, the number of memory cells in a chip was about 7 million. The number of failure bits in the SOTB SRAM was smaller, but the difference was 3 to 5X and it was not very significant.

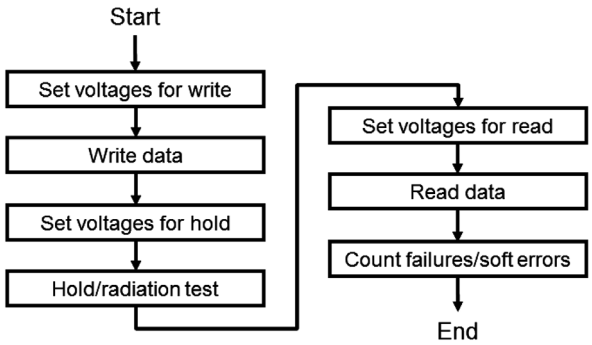

Fig. 4. Flow of hold and accelerated alpha and neutron tests.

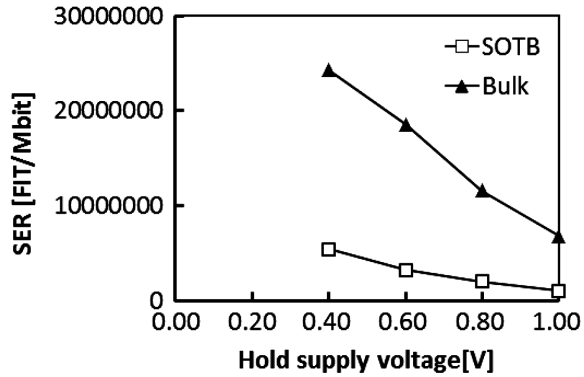

Fig. 5. Measured alpha-induced SEU versus supply voltage.

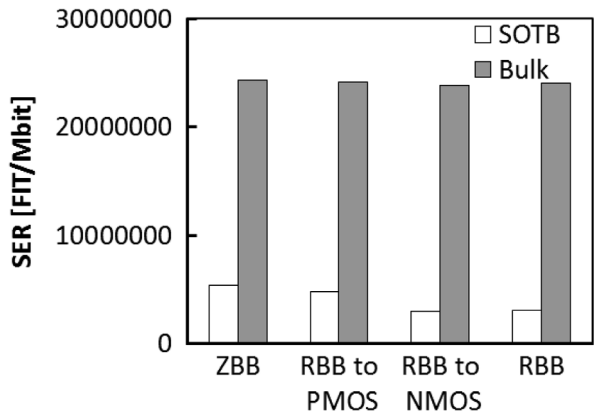

Fig. 6. Measured alpha-induced SEU vs. body biasing at 0.4 V supply voltage.

Fig. 4 illustrates the flow of both hold and irradiation tests. In this flow, the supply and body voltages are first set for write operation. The SRAM memories are initialized by writing a data pattern for the test through the data/address shift registers. Then, the supply and body voltages are changed to those for hold operation and the SRAM is turned into a hold operation. For the irradiation test, alpha or neutron irradiation is carried out during this hold operation. After that, the voltages are set back for read operation, and the data stored in the SRAM is read through the shift registers. Finally, the number of failure bits or upsets is counted outside the test chip. The hold test procedure is carried out for two situations; zero is stored in the SRAM, and one is stored in the SRAM. By repeating this test flow without irradiation, failure bits for hold operation are identified. These failure bits are eliminated in the next irradiation test. Note that the transitions of the supply and body voltages from write operation to hold operation and from hold operation to read operation are carried out with a large time interval at sufficiently small voltage steps to prevent voltage overshoot/undershoot from causing unexpected failures. For the irradiation tests, only the pattern of all 0 data was used due to the limited beam time. SER evaluation for other data patterns is included in our future work.

III. Measurement Results

A. Alpha Test

An accelerated alpha irradiation test was conducted using an Americium-241 foil with a flux was 7.83×10^9 cm^{-2}h^{-1}. This flux value does not include the solid angle correction. The foil was put above the test chip within 1.8 mm for 200 s of hold operation. The number of consecutive SEUs at the same bit in 200 s irradiation was sufficiently small, and they were probabilistically eliminated using Poisson distribution. The error of irradiation duration caused by manually putting on and taking off the alpha foil was smaller than 1%. When irradiating directly ionizing particles, such as alpha particles, the total ionizing dose, which permanently degrades the device characteristics due to the deposition of particles in the insulator, may damage semiconductor devices. However, in this experiment, the increase in the number of failure bits and leakage current was not observed in any of the cases, and the effect of total ionizing dose was not considered.

Fig. 5 shows the measurement results of the accelerated alpha test with voltage scaling and ZBB. The vertical axis represents the number of measured SEUs per bit per second. Clearly, both devices became sensitive to radiation and the number of SEUs increased as the voltage was lowered. The number of measured SEUs on the SOTB SRAM at 0.4–V supply voltage was 5.0 times larger than that at 1.0–V supply voltage. The number of SEUs on the SOTB SRAM at 0.4 V was 0.22 times smaller than that on bulk SRAM at 0.4–V supply voltage. The SOTB SRAM was more robust than the bulk SRAM.

Fig. 6 shows the dependency of measured SEUs on body biasing at 0.4–V supply voltage. Under RBB conditions, a $-0.5-$ V body bias was applied to the PMOS, NMOS, and those of both SRAMs. In all cases, the SOTB SRAM was more robust against radiation than the bulk SRAM. Similar to other reported results of alpha-induced SER [14], the SEU rate of the bulk SRAM was less sensitive to body biasing. On the other hand, the SEU rate of the SOTB SRAM was reduced by 35% with 0.5 V RBB. In particular, the RBB to the NMOS was effective in reducing the SER, which suggests that NMOS contributes to SEU.

B. Neutron Test

The accelerated neutron irradiation test was conducted at the Research Center for Nuclear Physics (RCNP) at Osaka University using an accelerated spallation neutron beam. The average flux density of the neutron beam was 2.46×10^9 cm^{-2}h^{-1}. In this test, the six test boards, each of which had 16 test chips, were placed in series on the beam track, so that 64 SOTB test chips (about 452 Mb) and 32 bulk test chips (about 226 Mb)

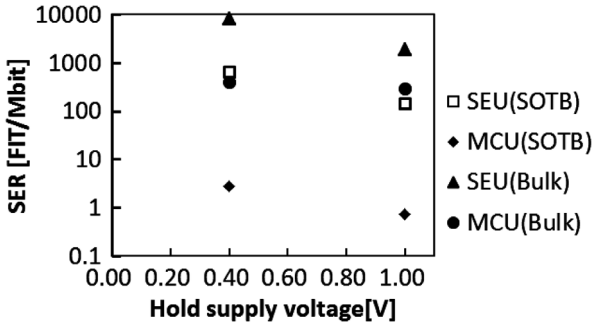

Fig. 7. Measured neutron-induced SEU and MCU vs. supply voltage.

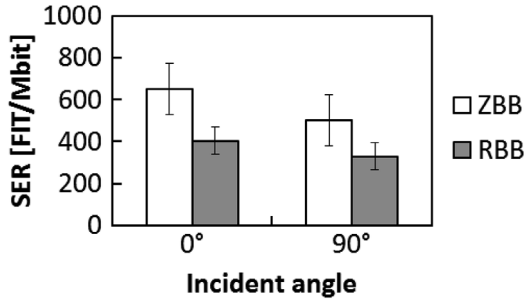

Fig. 8. Measured SBU rates of SOTB SRAM at 0.4 V.

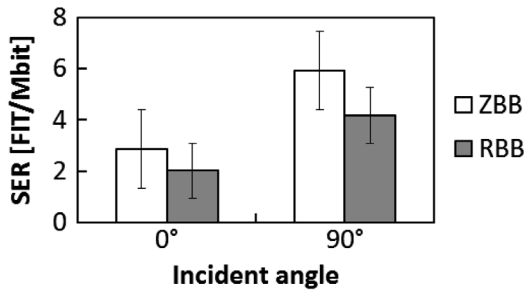

Fig. 9. Measured MCU rates of SOTB SRAM at 0.4 V.

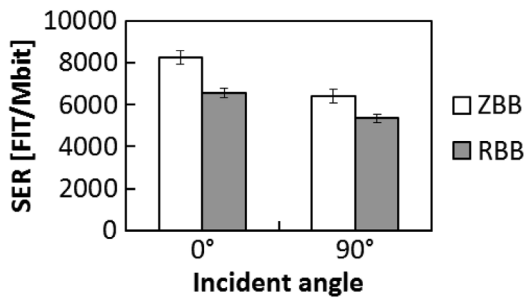

Fig. 10. Measured SBU rates of bulk SRAM at 0.4 V.

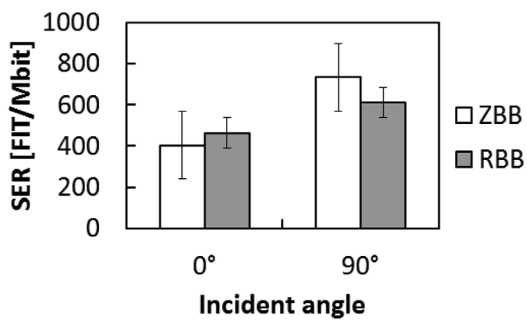

Fig. 11. Measured MCU rates of bulk SRAM at 0.4 V.

could be tested simultaneously. The incident angle of the neutron beam to the test boards was 0° or 90°, as is illustrated in Fig. 3. The hold operation was set to 600 s. We observed some outliers in the obtained data. Such outliers were eliminated using the Smirnov-Grubbs test [19].

Fig. 7 shows the measurement results of the accelerated neutron test with voltage scaling and ZBB. The incident angle of the beam was 0°. Each error bar indicates the standard deviation of the obtained upsets. Note that our definition of MCU states that two or more simultaneous upsets are in vertically, horizontally, and/or diagonally adjacent bits. The number of measured SEUs on the SOTB SRAM at 0.4-V supply voltage was 4.4 times larger than that at 1.0–V supply voltage, while the number of SEUs on the SOTB SRAM at 0.4 V was 0.08 times smaller than that on the bulk SRAM at 0.4–V supply voltage. The number of SEUs on the SOTB SRAM at 0.4–V operation was roughly equivalent to that on the bulk device at 1.0 V. On the other hand, the number of measured MCUs on the SOTB SRAM was two orders of magnitude smaller than that on the bulk SRAM. This tendency between the SOTB and bulk SRAM is consistent with previous results [20] in which FD-SOI and bulk devices were compared at a nominal voltage.

We now focus on 0.4–V operations. Fig. 8 shows the SBU rates of the SOTB SRAM, and the rates are presented separately in terms of the incident angles and ZBB/RBB. The SBU rate was higher at the incident angle of 0°. For body biasing, we can see the tendency of RBB reducing the SBU rate, and its reduction ratios at 0° and 90° were 38% and 34%, respectively. Fig. 9 shows the MCU rates of the SOTB SRAM. Contrary to the SBU rate, the MCU rate was higher at the incident angle of 90°. Harada *et al.* [21] investigated the MCU angular dependency through measurement and simulation. The measured MCU patterns were explained by the fact that secondary ions contributing to MCU tend to emit forward and upset the memory cells along the neutron beam. This measurement result was consistent with a Monte-Carlo simulation performed with the Particle and Heavy Ion Transport code System (PHITS) [22] and a sensitive volume model [23]. Tipton *et al.* [24] also explained the angular dependency by using a simulation in which the forward emission of secondary ions leads to secondary ions hitting multiple sensitive nodes in the case of irradiation at a large incident angle. When the incident angle is 90°, the secondary ions emitted forward by nuclear reaction travel parallel to the chip surface, and more likely pass through multiple sensitive volumes for upsets. Also, RBB reduces the MCU rate by 30% at both 0° and 90°. These SER reductions by RBB were investigated through TCAD device simulation, which will be discussed in Section IV.

Similarly, Figs. 10 and 11 show the SBU and MCU rates of the bulk SRAM. The SBU rate was higher at the incident angle of 0° while the MCU rate was higher at 90°, which is similar to the results of the SOTB SRAM. The RBB reduced the SBU rates, but the impact of the RBB on MCU was not clear.

Fig. 12 shows the MCU rates for each number of simultaneous bit flips in the SOTB and bulk SRAMs at the incident

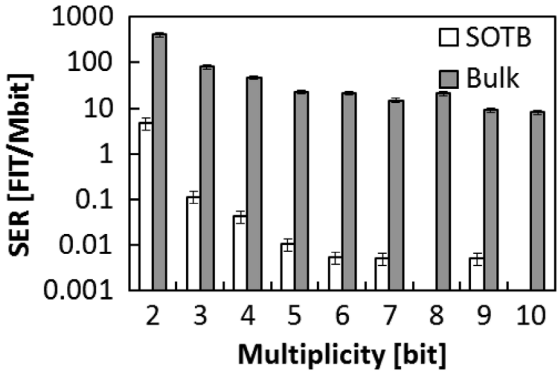

Fig. 12. Measured neutron-induced MCU rate as function of number of bit flips in the SOTB and bulk SRAMs (0.4 V, 0°).

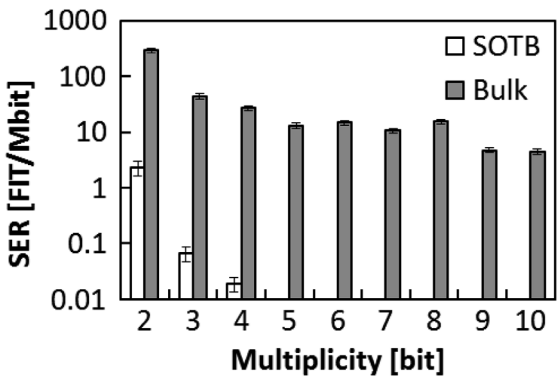

Fig. 13. Measured neutron-induced MCU rate as function of number of bit flips in the SOTB and bulk SRAMs (0.4 V, 90°).

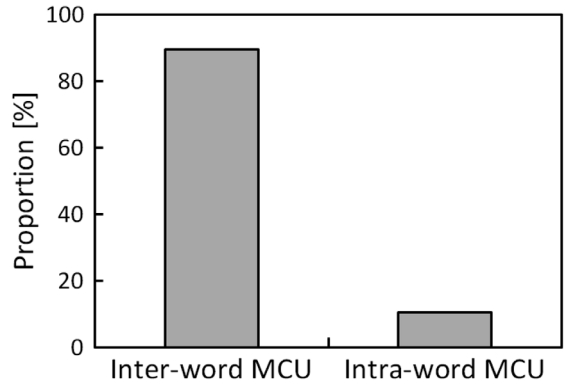

Fig. 14. Proportions of intra- and inter-word MCU events at incident angle of 0°.

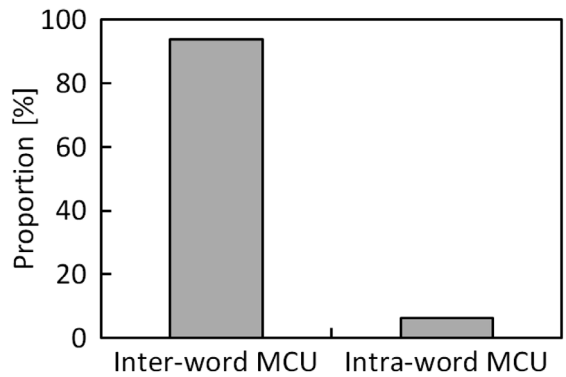

Fig. 15. Proportions of intra- and inter-word MCU events at incident angle of 90°.

angle of 0°. As the number of bit flips increased, the number of measured MCUs quickly decreased in the SOTB SRAM, while it slowly decreased in the bulk SRAM. Even the MCU rate of simultaneous 10-bit flips in the bulk SRAM was higher than the MCU rate of 2-bit flips in the SOTB SRAM. In terms of MCU, SOTB is superior to bulk since MOS transistors do not share a well in SOTB and charge sharing and parasitic bipolar action do not occur. Note that even in bulk SRAMs, 0.4–V operation is supposed to make the parasitic bipolar action less active. Fig. 13 shows the result at the incident angle of 90°. In this case, 9-bit MCU occurred even in the SOTB SRAM, while its rate was more than three orders of magnitude lower than that of the bulk SRAM. As explained above, the forward-emitted secondary ions tend to pass through multiple sensitive volumes; hence, larger MCUs were observed at the incident angle of 90°.

On the other hand, most of the MCU spatial patterns spanned in the direction of the word line, and the proportion of MCUs that spread within a word, which is hereafter called intra-word MCU, was low. We classified the MCU events into two categories. The first category includes MCUs that induce a single bit flip within a word, in other words, multiple words had a single bit upset. We call the MCU in this category an inter-word MCU. The second category includes intra-word MCUs that induce two bit flips in a word. Note that three or more bit flips in a word were not observed in our irradiation experiments. Fig. 14 shows the proportion of the inter-word MCU events and intra-word MCU events at the incident angles of 0°. We can see that 90.9% of the MCUs were inter-word MCUs that induced a single bit upset within a word. This is because the minimum distance between the sensitive areas within the word is 0.34 μm and is 1.7 times larger than that across the words; 0.20 μm, as depicted in Fig. 3. A secondary ion more likely passed through the sensitive areas across the words. Also, such inter-word MCUs can be eliminated by single-error-correction (SEC) error correction code (ECC). When we apply SEC ECC to an SOTB SRAM, the multiple bit upset (MBU) rate, which represents the rate of the errors that cannot be eliminated by SEC ECC, becomes 0.091 times smaller than the MCU rate. Even without bit-interleaving, which involves performance overhead, an SOTB SRAM with SEC ECC can attain high reliability. Fig. 15 shows the proportion at 90°. In this case, the beam direction is parallel to the word line; hence, the proportion of intra-word MCU events decreases and is 0.055.

IV. Device Simulation for Investigating SER Dependence on Body Bias

The measurement results in the previous section showed that the alpha- and neutron-induced SER on the SOTB SRAM with a 0.5-V RBB was roughly two thirds that with a ZBB. To investigate this SER dependence on body bias further, we conducted device simulations.

We constructed a 3D model of a 0.52 μm-wide 65–nm long SOTB NMOS transistor, which corresponds to one of the NMOSs comprising the cross-coupled inverters in a 6T SRAM

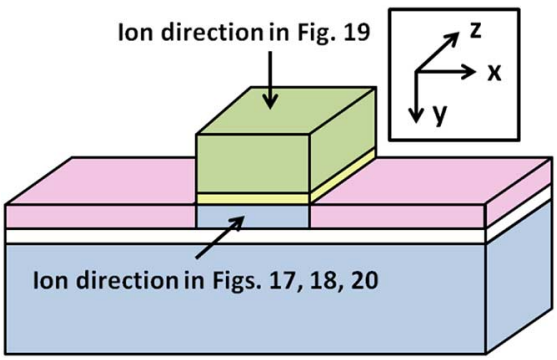

Fig. 16. Directions of ion injection.

cell. The lengths of the source and drain regions were 0.2 and 0.16 μm, respectively. The distance between the transistor and well contact was 0.77 μm. This model had a 10-nm thick SOI layer and 12-nm thick BOX layer. The depth of the STI was 0.4 μm. This NMOS device was then connected to the other five transistors included in the SRAM cell at the circuit simulation level, and the transient behavior of an SRAM cell against an ion passage was simulated with a mixed mode option of a commercial TCAD simulator (Sentaurus of Synopsys). The ohmic contact option was selected as the boundary condition. To reproduce the measurement condition, the supply voltage was set to 0.4 V and the body voltage was set to zero or -0.5 V.

The density of charge generation followed a Gaussian distribution with a standard deviation of 30 nm [25]. The LET was varied from 0.001 to 0.1 pC/μm. Fig. 16 illustrates the directions of the ion injection. First, the ions were injected in the direction of the gate width, i.e., parallel to the z-axis. To identify the sensitive region, we swept the location of the ion injection in the x-y plane with a step of 10 nm. The ion range was 1 μm, which was larger than the NMOS width.

Fig. 17 illustrates the sensitive regions obtained from device simulations of 0.5-V RBB and ZBB. The dark gray points represent the locations at which the injected ions caused a bit flip, and the light gray points correspond to the locations causing no bit flips. First, we compared the RBB and ZBB results for a LET of 0.003 pC/μm. In this case, the NMOS with ZBB had a larger sensitive region than the NMOS with RBB, which indicates that SOTB NMOS with ZBB is more sensitive to ions with small LET than that with RBB. As the LET becomes higher, the sensitive region becomes larger in both ZBB and RBB cases. Also, the sensitive region extends more to the drain region than to the source region, which is more significant in ZBB than in RBB.

Fig. 18 shows the relation between the area of the sensitive region and LET. The area of the sensitive region follows a logarithmic function of the LET since the x-axis is log-scale, the y-axis is linear, and the relation between the area of the sensitive region and LET is almost linear. We can see that the RBB slope in Fig. 18 is larger than that of ZBB, and the two lines cross over at the point of 0.00833 pC/μm. Below this LET, the sensitive region of RBB is smaller than that of ZBB. The x-intercept of RBB, which corresponds to the minimum LET that can cause SEU, is 0.00273 pC/μm while that of ZBB is 0.00212 pC/μm.

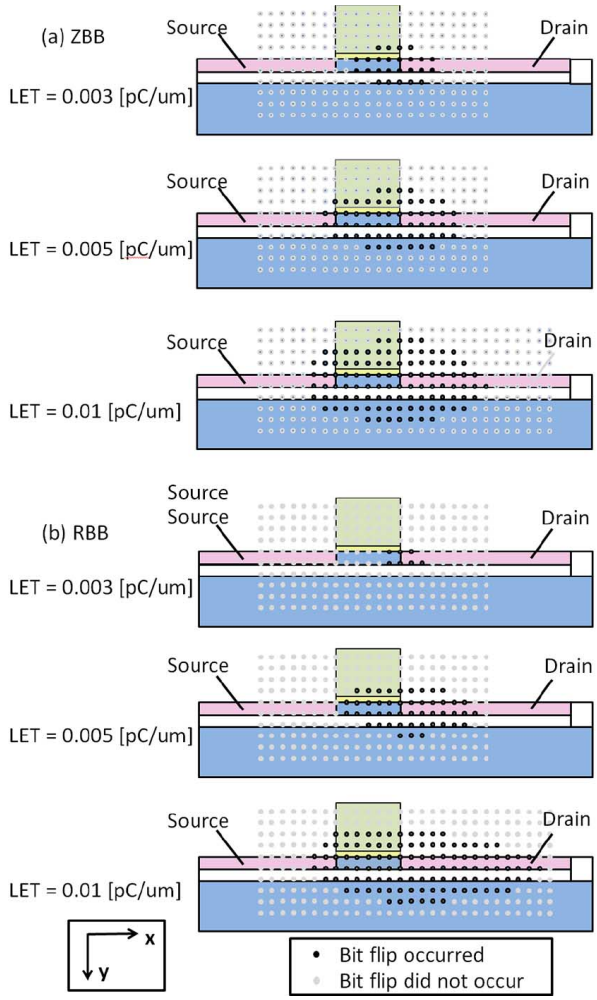

Fig. 17. Sensitive regional area of (a) ZBB and (b) RBB. Ions were injected in z-axis direction.

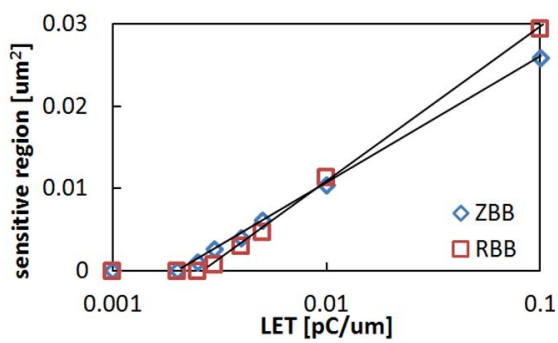

Fig. 18. Relation between area of sensitive region and LET. Ions were injected in z-axis direction.

Next we conducted TCAD simulations for ions injected at the incident angle of 0°, i.e., in parallel to the y-axis in Fig. 16. The injection location was swept in the x-z plane. Fig. 19 shows the relation between the area of the sensitive region and LET for an incident radiation angle. Except for the ion direction, the simulation setup was the same as for the results shown previously in Figs. 17 and 18. The LET value to cause an upset was larger than that in Fig. 18 since the travel distance of the ion within the

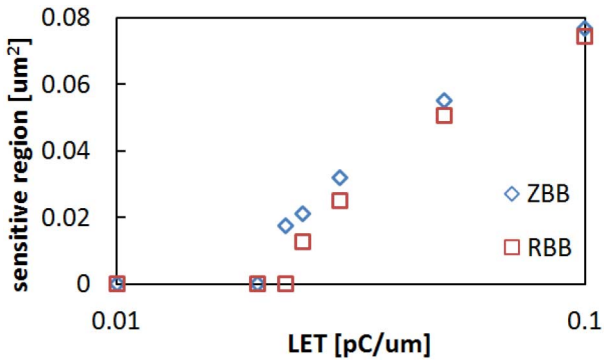

Fig. 19. Relation between area of sensitive region and LET for ions injected at incident angle of 0°, i.e., parallel to y-axis.

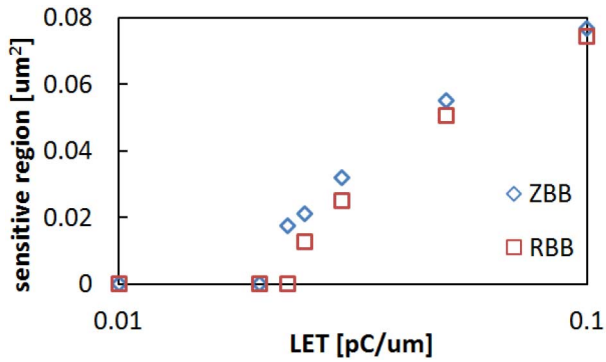

Fig. 20. Sensitive region when charge generation was artificially dense (ZBB). Ions were injected in z-axis direction.

SOI layer was smaller and the charge deposited within the SOI layer by the same LET ions was smaller.

By using the program of the stopping and range of ions in matter (SRIM)[26], we estimated the LET of an alpha particle that passed through the SOI layer assuming that the alpha particle with 5.5 MeV energy penetrated the test chip parallel to the y-axis. This situation corresponds to the alpha irradiation test. This LET value was estimated to be 0.00564 pC/μm, and the area of the sensitive region for the LET of 0.00564 pC/μm in Fig. 19 was zero for both ZBB and RBB. On the other hand, the alpha particles were not necessarily emitted from the alpha source parallel to the y-axis, and some particles penetrated the device under test (DUT) diagonally. In this case, the alpha particles travelled longer and lost their energies before reaching the SOI layer. In addition, due to a certain thickness of the alpha source layer, the energy of the emitted alpha particles was smaller than 5.5 MeV. Such alpha particles with lower energy had higher LET. The LET became maximum at 0.0144 pC/μm when the energy of the alpha particle was 500 keV. Even for the alpha particles with the maximum LET of 0.0144 pC/μm, the RBB had a smaller sensitive region, as shown in Fig. 19; hence, the measured SER of the RBB was lower than that of ZBB in the previous section. As for the ion injection parallel to the z-axis, the RBB had a larger sensitive region for an LET of 0.00833 pC/μm and higher, and some alpha particles were thought to have a higher LET than 0.00833 pC/μm. However, in the alpha irradiation test, the alpha source was put immediately above the DUT. The distance between the alpha source and DUT was less than 2 mm, while the chip size was 6 mm $\times$ 6 mm and the alpha source size was 10 mm $\times$ 10 mm. In this case, none or very few alpha particles were thought to travel parallel to the z-axis, and consequently the contribution of such alpha particles to the SER was limited.

Finally, to clarify the difference between SOTB and bulk device, we conducted an artificial TCAD simulation. In this simulation, for the SOTB device, we injected ions that generated charges very densely on the ion track. More concretely, the density of the charge generation followed a Gaussian distribution with a standard deviation of 1 nm. Note that this density of charge generation was artificial and did not correspond to any ions that actually exist. Fig. 20 shows that the sensitive region in the SOTB device was restricted in the 12-nm thick SOI layer. This observation is consistent with previous studies [8], [15], [16], and the SOTB also had a sensitive volume limited to the SOI layer. The charge deposited in the SOI layer was amplified using a parasitic bipolar transistor and the amplified charge was collected at the drain [16]. On the other hand, the sensitive volume spanned deeply in the bulk device [16], and the depth of the sensitive volume was 0.6 μm in a 65-nm CMOS technology [21], for example. The deposited charge was collected at the drain by drift and diffusion [27], [28], [29].

V. Conclusion

We investigated the soft error immunity of an SOTB SRAM compared with a bulk SRAM for 0.4-V operation. The measurement results under alpha and neutron irradiation show that the soft error immunity of the SOTB device was superior to that of the bulk device. In particular, the MCU rate and its distribution of multiplicity were quite different. The 2-bit MCU rate of the SOTB SRAM was lower than that of the bulk SRAM by two orders of magnitude, and the difference in the rate of 3-bit and larger MCUs was larger than two orders of magnitude. We also confirmed that most of the MCUs were inter-word MCUs and one-tenth of the MCUs were intra-word MCUs that could not be eliminated by SEC ECC. Another observation was that RBB reduced the SER to two-thirds in the SOTB SRAM. To investigate the dependence on body bias, we carried out device simulations. The simulation results show that RBB reduced the sensitive cross-sectional region for the ions with small LET, which could explain the measured body bias dependence. Throughout our experiments, we revealed that the SOTB SRAM is more robust even at 0.4 V compared to the bulk SRAM at 1.0 V, and SOTB devices are suitable for low voltage circuit design due to not only higher controllability of V_{th} but also higher soft error immunity.

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