Soft Error Immune Latch Design for 20 nm bulk CMOS

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***Abstract* — This paper discusses soft error immune latch (SEILA) design aiming to prevent soft errors originating from charge collection to multiple nodes. We first designed 28 nm SEILA with double height cell (DHC) and evaluated its SEU rate through neutron irradiation test. The SEU rate is at the same level with 65 nm DHC-SEILA. Next, for enhancing the soft error mitigation efficiency, we designed SEILA with triple height cell (THC) in 20 nm. The 20 nm THC-SEILA achieves 14 times lower SEU rate than 28 nm DHC-SEILA. The area overhead compared to a normal latch is 140 % in the 20 nm THC-SEILA.**

I. INTRODUCTION

For high-end microprocessors, single event upset (SEU) in sequential elements such as latches is a critical issue more than that in SRAM because it is difficult to apply error correction code (ECC) to the latches in logic circuits. Redundancy-based radiation-hard latches having more than two storage nodes are developed for mitigating SEU in sequential elements [1]–[8]. The data stored in these latches cannot be corrupted by the charge collection to a single node. The data, however, can be corrupted when the generated charge is collected to multiple nodes. There are four possible mechanisms of charge collection to multiple nodes (CCM) as shown in Table I [9]. In any mechanism of the four, the occurrence probability of CCM depends on the distance between the two drain areas connected to SEU sensitive nodes. The CCM occurrence probability increases as the distance between the sensitive areas decreases, and this distance decrease is accompanied with transistor size shrinking, i.e. process technology advance.

In this work, we designed soft error robust latches in 28 nm and 20 nm technologies with soft error immune latch (SEILA) [10],[11] technique, which is a soft error mitigation technique through layout and circuit optimization in redundant circuits. We first designed 28 nm SEILA with double height cell (DHC) and evaluated its SEU rate through neutron irradiation test. The SEU rate is at the same level with 65 nm DHC-SEILA. Next, for enhancing the soft error mitigation efficiency, we designed SEILA with triple height cell (THC) in 20 nm. The 20 nm THC-SEILA achieves 14 times lower neutron-induced SEU rate than the 28 nm DHC-SEILA, and the alpha-induced SEU rate is less than 1 FIT/Mbit with 90% statistically probability for 0.001 alpha/hour/cm^2.

The rest of this paper is organized as follows. Section II explains CCM mitigation techniques adopted in SEILA. Section III presents irradiation test results and SEU mitigation efficiency of 28 nm SEILA, and Section IV shows those of 20 nm SEILA. Finally, Section V concludes this paper.

Table I. Four MCU possible mechanism.

Symbol	Name
(A)	Successive hits by one ion
(B)	Multi hits by multiple ions
(C)	Charge drift/diffusion (charge sharing)
(D)	parasitic bipolar action (PBA)

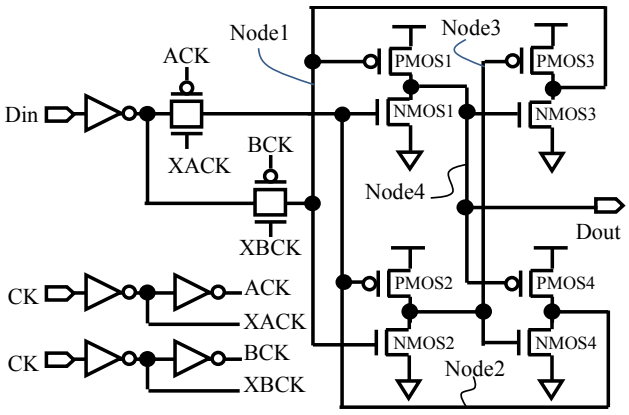

Figure 1. SEILA schematic.

II. SEILA

Figure 1 shows the schematic of SEILA which is proposed in [10]. SEILA employs the dual inter-lock cell (DICE) type circuit for storage in which a voltage variation on one node cannot corrupt the storage data [3]. However, the storage structure in the conventional DICE type circuit cannot prevent SEU from being caused by CCM and single event transient in local clock (SETLC). To overcome these problems, SEILA includes two implementation techniques for enhancing the mitigation efficiency; multiple height cell (MHC) and dual clock buffer (DCB). MHC technique, which enables layout optimization, is introduced for suppressing CCM. DCB is applied for mitigating SETLC. This paper focuses on the prevention of CCM induced error and discusses layout optimization using MHC technique. DCB will not be discussed further in this paper, but it is applied to the SEILAs designed in this paper.

When the charge is collected to the drain areas of a PMOS and an NMOS which are connected each other, the node voltage does not change much [12]. From the NMOS point of view, the drain of such a PMOS can be regarded as a cancelling area. The PMOS drain and NMOS drain collect holes and electrons, respectively, and the holes and electrons

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are canceled out due to the connection between the PMOS drain and NMOS drain. On the other hand, from the PMOS point of view, the NMOS drain can be regarded as the cancelling area.

The impact of CCM due to (A) and (C) in Table I can be suppressed by placing the cancelling area between the two critical areas. In this placement, when an ion passes through the two critical areas, the ion must go through the cancelling area as well. In addition, when the charge is shared by the two critical areas, the charge must be also shared by the cancelling area. For enabling such a placement, the layout of SEILA was designed as MHC, i.e. double height cell (DHC) or triple height cell (THC) as shown in Figure 2. The layout flexibility introduced by the increased cell height makes it possible to exploit the cancelling effect for SEU reduction.

The area for the transistor placement is not different between MHC and single height cell (SHC), though the aspect ratio is changed as shown in Figure 2. Compared to DHC, THC is expected to attain higher mitigation efficiency due to the following reason. In DHC designed with PMOS center placement, all the PMOSs are included in an N-well area, and NMOS cannot be located between the PMOSs. In DHC designed with NMOS center placement, PMOS cannot be located between the NMOSs. These mean that NMOS/PMOS cancelling area cannot be located between critical areas in the DHC designed with PMOS/NMOS center placement, respectively. On the other hand, THC enables both PMOS and NMOS canceling areas to be placed between corresponding critical areas. A drawback of the THC cell is routing congestion because of the narrow width, which may increase the cell area.

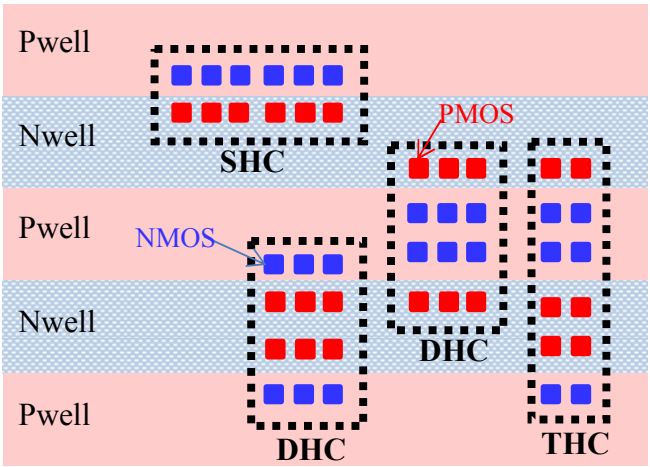

Figure 2. Layouts of SHC, DHC and THC.

III. SEU MITIGATION EFFICIENCY OF 28 NM DHC-SEILA

We designed a SEILA with DHC in 28 nm technology referring to the previous design [10] and evaluated SEU rate through neutron irradiation test. The neutron irradiation test was performed on the device under tests (DUTs) including the SEILAs with spallation neutron beam at research center for nuclear physics (RCNP) in Osaka University. The average flux of neutron beam whose energy was higher than 10 MeV was 2.01 billion neutron/hour/cm^2, and the irradiation time was 60 hours. Figure 3 shows the timing chart of the test procedure. During the write phase, a 10 MHz clock signal was given to write the data patterns in the latches. Then, the SEILAs were kept in hold operation for 15 minutes, and the stored values were read out. The supply voltage was 0.75V in read/write phases and 0.7, 0.85 and 0.9V in hold phase. The hold duration is over 1,000 times longer than the read/write durations, and hence the measured upset counts can be regarded as the upset counts during the hold operation.

The SEU rate in the 28 nm DHC-SEILA is at the same level with that of the 65 nm DHC-SEILA [10] as show in Figure 4. This means that the layout technique using DHC is still active in 28 nm. Here, the sensitive area in 28 nm is smaller than in 65 nm, but the distance between the critical areas in 28 nm is shorter than in 65 nm. As a result, the SEU rates are at the same level in the 65 nm and 28 nm DHC-SEILA.

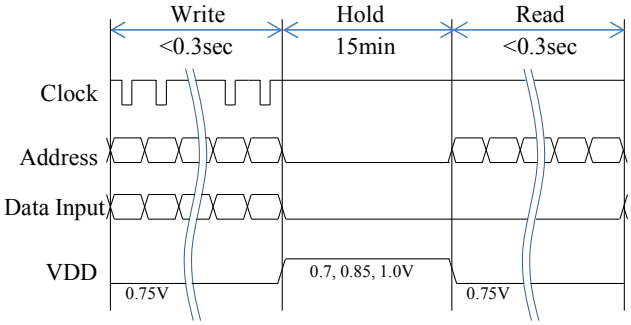

Figure 3. Test timing chart for the 28 nm DUT of irradiation tests.

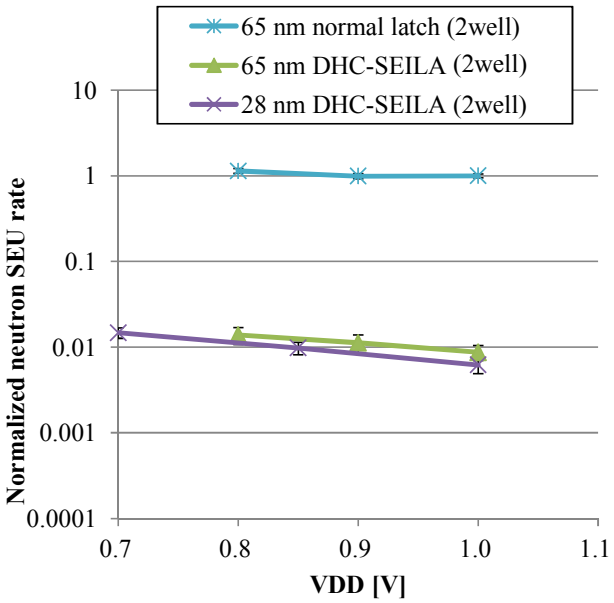

Figure 4. SEU rate in 65 nm normal latch [10], 65 nm DHC-SEILA [10], and 28 nm DHC-SEILA. These SEU rates are the average values of the rates for DATA0 and DATA1. All latches in this figure are manufactured with double-well process (without DNW). The SEU rates are normalized with SEU rate in 65 nm normal latch at 1.0V. Error bars represent 90% statistical confidence level.

On the other hand, compared to a processor chip fabricated in 65 nm technology, more than 5× transistors are integrated on a microprocessor chip in 28 nm technology [13], [14]. This indicates that the SEU prevention by the DHC-SEILA in 28 nm processors cannot keep the same level of chip-level reliability. If the DHC-SEILA would be used for the next 20 nm processor, further reliability degradation was supposed to be anticipated since CCM would occur more frequently due to geometry shrinking and the number of transistors in a processor would increase.

The result of the 28 nm DHC-SEILA is examined in detail. Figure 5 shows the SEU rates in the 28 nm DHC-SEILA for DATA0 and DATA1. SEU was observed only for DATA0 and no SEU was observed for DATA1. On the other hand, the distance between the critical nodes was 0.15 and 0.21 um for DATA0 and DATA1, respectively. This result clarified the importance of the distance on SEU prevention.

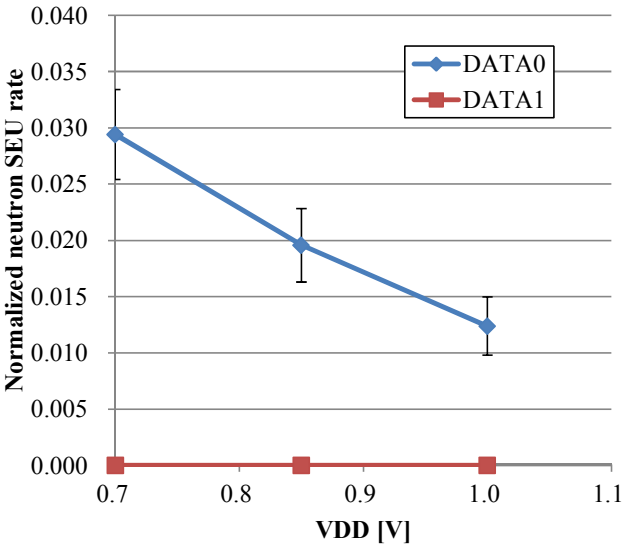

Figure 5. SEU rates in 28 nm DHC-SEILA of double-well for DATA0 and DATA1. The SEU rates are normalized with SEU rate in 65 nm normal latch at 1.0V. Error bars represent 90% statistical confidence level.

IV. SEU MITIGATION EFFICIENCY ON 20 NM DHC-SEILA

To cope with the increase in the number of latches on a chip due to the technology scaling from 28 nm to 20 nm, further robustness improvement is required for SEILA. Motivated by this, 20 nm SEILA was designed with THC. THC is expected to provide higher mitigation efficiency than DHC because of following reasons;

- Larger distance can be obtained.
- The critical transistor pairs can be located in different wells.
- The cancelling transistors can be placed between the critical transistor pairs.

In the developed THC-SEILA, all the critical pairs of PMOSs and NMOSs are not included in the same well area, and the canceling area is located between the paired critical areas. On the other hand, some critical pairs in the DHC-SEILAs are included in the same well, and the cancelling area is not located between the critical pair. This transistor location is one of reasons of SEU occurrence in the DHC-SEILAs observed in the previous section. In addition, well-contacts located in the cell area of the 20 nm THC-SEILA for attenuating PBA-induced CCM, which is (D) in Table I. The cell size of the designed THC-SEILA is about 2.4 times as large as that of a 20 nm normal latch, and three metal layers are used for interconnection inside the cell, while two metal layers are used in normal latches.

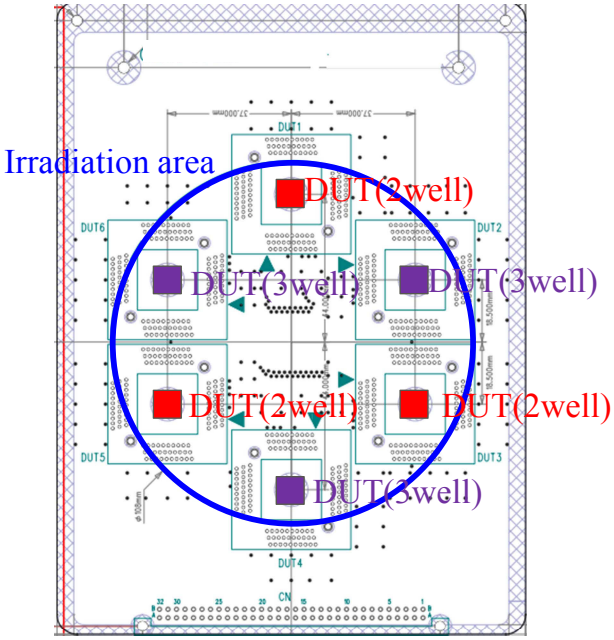

Figure 6. Board configuration of the 20 nm DUT for irradiation tests.

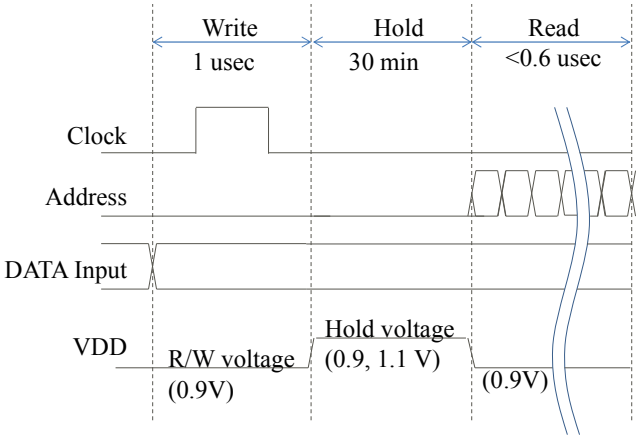

Figure 7. Test timing chart of the 20 nm DUT for irradiation tests.

Neutron irradiation test was performed with the spallation neutron beam at RCNP for 108 hours. The DUT includes two types of 20 nm THC-SEILAs which are with and without the well-contact in the cell. About 8 Mb and 6 Mb of the SEILAs with and without well-contacts are included in the DUT. The DUTs were assembled on plastic packages with wire bonding. The five DUT boards were irradiated, and each DUT board has three DUTs with DNW and three DUTs without DNW as shown in Figure 6. The DNW is placed under the latches and logic area, not under the I/O area. The N-well and P-well are

connected to VDD and GND in both the DUTs irrelevant to DNW existence. Figure 7 shows the timing chart of the test procedure. In the write phase, we set data to all latches in the DUTs with one clock signal. Then, the latches were kept in hold operation for 30 minutes, and the stored values were read out. The supply voltage was 0.9V in the read/write phases and 0.9 and 1.1V in the hold phase. The hold duration is over 10,000 times longer than the read/write durations, and hence the measured upset counts can be regarded as the upset counts during the hold operation.

The neutron induced SEU rate of the 20 nm THC-SEILA is 14 times lower than those of the 28 nm and 65 nm DHC-SEILA as shown in Figure 8. By exploiting the layout flexibility thanks to THC, higher prevention efficiency of CCM induced SEU is attained. On the other hand, compared to a processor chip fabricated in 65 nm technology, more than 6× transistors are integrated on a microprocessor chip in 20 nm technology [13], [15]. This indicates that the SEU prevention by the THC-SEILA in 20 nm processors improves the chip-level reliability from the 65 nm processors. The SEU rate of the THC-SEILA was kept low in both double- and tipple-well, while the SEU rate with triple-well is a little higher than that with double-well.

The result is examined in detail focusing on the difference of the well configuration and the contribution of the well-contacts in the cell. Figures 9 and 10 show the SEU rates in the 20 nm THC-SEILA for DATA0 and DATA1 with and without well-contacts in the cell. The error bars in this figure represent 90% statistical confidence level.

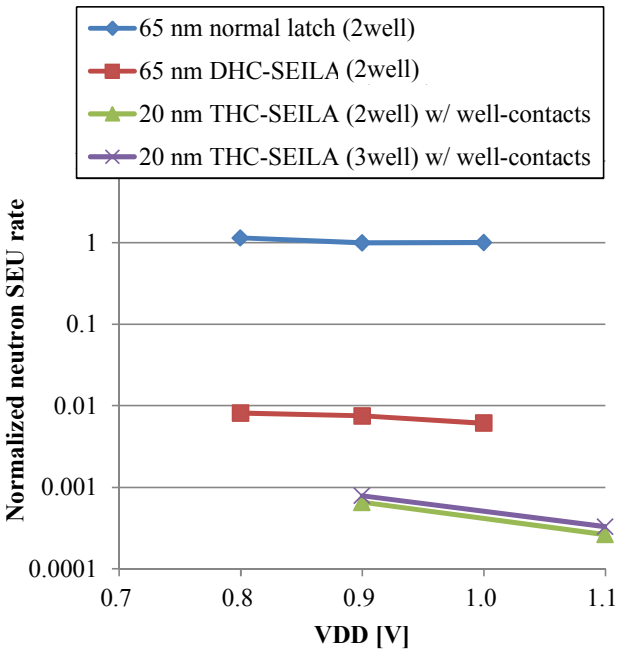

Figure 8. SEU rates in 20 nm THC-SEILA of double- and triple-well. The SEU rates are the average values of the rates for DATA0 and DATA1. The SEU rates are normalized with SEU rate in 65 nm normal latch at 1.0V. Error bars represent 90% statistical confidence level.

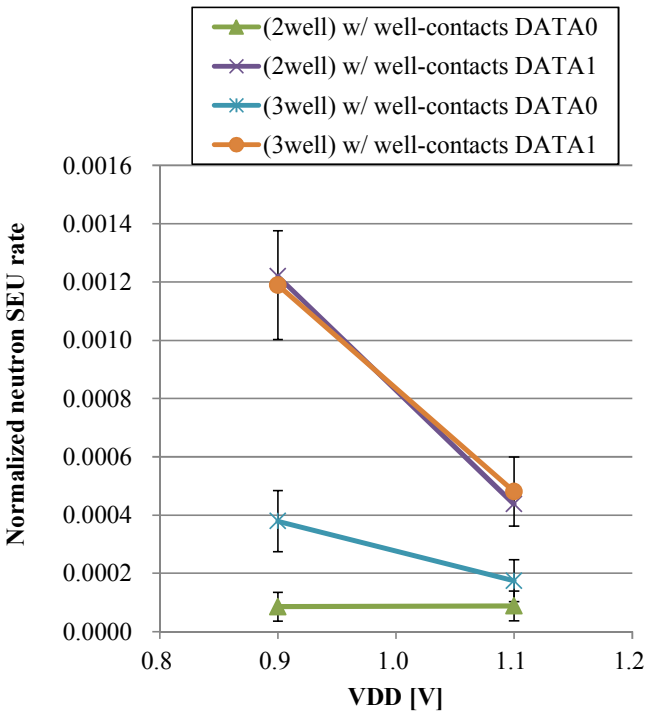

Figure 9. SEU rates in 20 nm THC-SEILA for DATA0 and DATA1 with well-contacts in the cell. Error bars represent 90% statistical confidence level.

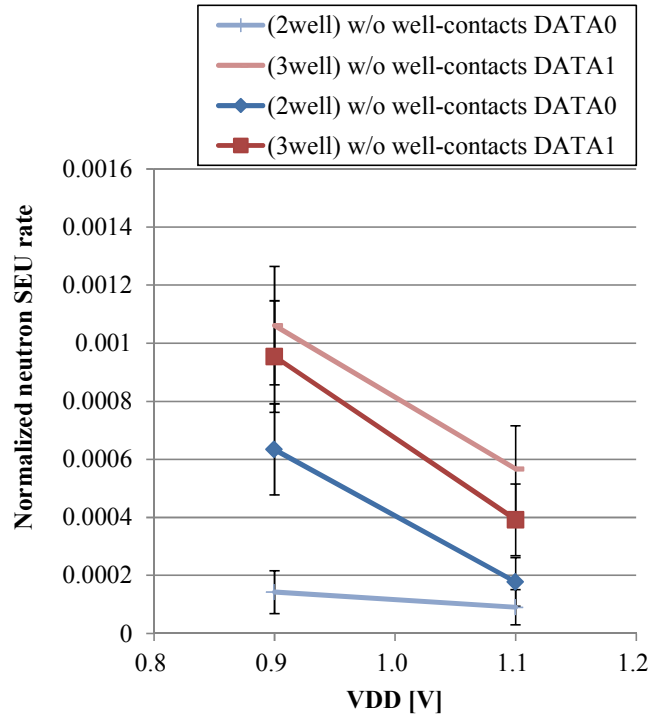

Figure 10. SEU rates in 20 nm THC-SEILA at DATA0 and DATA1 without well-contacts in the cell. Error bars represent 90% statistical confidence level.

Changing the well structure from double- to triple-well, the SEU rates increase only for DATA0, and no large different was observed for DATA1 in both the 20 nm THC-SEILAs with and without well-contacts. NMOS is sensitive to SEU in DATA0 [16], and adapting triple-well intensifies the charge collection due to parasitic bipolar action in NMOS [10]. The SEU increase due to the triple-well process is higher in the SEILA without well-contacts than in the SEILA with well-contacts in the cell. The well-contacts contribute to the decrease in the SEU rate in the triple-well.

Also alpha irradiation test was performed using an ^{241}Am alpha source in a vacuum chamber. In the alpha irradiation test at 0.9, 1.0 and 1.1V, no error was observed in the 20 nm THC-SEILA with and without well-contacts in double- and triple-well, respectively. The SEU rates of all the 20 nm TCH-SEILAs in all conditions are less than 1 FIT/Mbit with 90% statistically probability for 0.001 alpha/hour/cm^2.

V. Conclusions

This paper designed and evaluated SEILA which adopted MHC (DHC, THC) design technique in 28 nm and 20 nm. The MHC design mitigated the SEU occurrence originating from CCM. Table II summarizes the SEU rates of the SEILAs.

In 28 nm technology, SEILA was designed with DHC. The SEU rate in the 28 nm DHC-SEILA is comparable with that of the 65 nm DHC-SEILA. The SEU rate in the 28 nm DHC-SEILA is not low enough since more latches are used in the 28 nm microprocessor than the 65 nm one.

Motivated by this, SEILA was designed in 20 nm technology with THC for achieving higher SEU prevention, and its neutron and alpha SEU rates were evaluated. The neutron induced SEU rate is 14 times lower in the 20 nm THC-SEILA than in the 28 nm DHC-SEILA. In the alpha irradiation test, no error was observed and the SEU rate is less than 1 FIT/Mbit with 90% statistically probability for 0.001 alpha/hour/cm^2.

Beyond the 20 nm technology, bulk CMOS technology is predicted not to be used, and instead FinFET or SOI technologies will be used. Soft error tolerance in FinFET and SOI technology is higher than bulk CMOS technology [17]. As a result, 20 nm bulk CMOS technology can be the toughest technology for mitigating soft error in SEILA. The results in this paper suggest that SEILA can be used as a radiation-hard latch in all transistor technologies.

Table II. Summary of SEU rates in SEILAs at 1.0V. The SEU rates are normalized with the SEU rate in 65 nm SHC-normal latch. Note that the SEU rates in 20 nm THC-SEILAs have no experimental data and the showing SEU rate is the average of SEU rate at 0.9 V and 1.1 V.

Latch name	SEU rate (2well)	SEU rate (3well)
65 nm DHC-SEILA [10]	0.0087	0.0061
28 nm DHC-SEILA	0.0062	Not available
20 nm THC-SEILA w/ well-contacts	0.00046	0.00056
20 nm THC-SEILA w/o well-contacts	0.00039	0.00061

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