Exploring Well-Configurations for Minimizing Single Event Latchup

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***Abstract*—This work experimentally studies single event latchup (SEL) prevention by altering well configurations. The well structures under consideration in this paper are ordinary twin-well structure, triple-well structure with deep N-well (DNW) and triple-well structure with deep P-well (DPW). Doping profiles are also varied in our experiments. Neutron irradiation tests for test chips fabricated in 55-nm and 90-nm bulk Si CMOS processes show that SEL can be suppressed with a DPW or a DNW well configuration and a high-dose implantation in the well. Among these, DPW was the most effective to eliminate SEL, and no SEL was observed throughout our irradiation tests in the SRAM with DPW in both 55-nm and 90-nm processes. In addition, DPW brings a desirable side effect of single event upset (SEU) reduction. A disadvantage is a cost to develop a DPW process. DNW is a common process option and hence it is easily adopted for SEL prevention, but we need to pay attention to the fact that DNW increases SEU rate. Increasing well doping in twin-well structure reduced SEL by 60%.**

***Index Terms*—Alpha, neutron, parasitic bipolar action, single event latchup, soft-error, SRAM, terrestrial environment.**

I. Introduction

SINGLE EVENT LATCHUP (SEL) occurrence in SRAM is one of the most important reliability issues for SRAM based electron devices fabricated in bulk CMOS technology. SEL is an abnormal high-current state in a device triggered by the passage of an energetic particle [1], [2], and it results in the loss of device functionality. SEL can cause permanent damage to the device [3]. Even if the device is not permanently damaged, the device needs to be turned off to recover from SEL [4]. This means that popular countermeasures for concealing upsets, such as error correction code (ECC), are helpless to SEL since SEL cannot be terminated. SEL had been regarded as an issue only for the devices used in environment having a large flux of high energy particles, such space environment [5]. On the other hand, SEL is becoming a critical concern even at ground level because terrestrial neutrons can cause SEL in technology nodes below 160 nm [6]. Dodd *et al.* reported that non-negligible SEL rates were observed in commercial products at terrestrial environment [7].

An abnormal current flows when a parasitic p-n-p-n bipolar, i.e. thyristor, in bulk CMOS devices is activated and power and ground are shorted [8], [9]. Note that there is no p-n-p-n junction in SOI devices and hence SOI devices are immune to SEL [10]. The parasitic p-n-p-n bipolar consists of P-drain, N-well, P-well and N-drain as shown in Fig. 1. Key parameters which influence SEL occurrence are the resistors ($\mathrm{R_{NW}}$ and $rm R_{PW\&Psub}$ in Fig. 1) and the current gains of the parasitic bipolar transistors (NPN and PNP in Fig. 1). $\mathrm{R_{PW\&Psub}}$ is determined by the resistivity of the P-well and the P-substrate and the distance between the NMOS transistor and P-well contacts. Similarly, $\mathrm{R_{NW}}$ depends on the N-well resistivity and the distance between the PMOS transistor and the N-well contacts. The current gains are determined by doping concentrations in the well and source regions and the distance between the well-junction and source regions.

To prevent SEL, several design methods have been proposed. Enlarging the distance from well edge to MOS source regions can suppress SEL [11]. Nicolaidis proposed a SEL mitigation scheme with built-in current sensor [12]. Adding a current-limiting device (CLD) to power line can also mitigate SEL since the reduction of power supply current prevents the parasitic bipolar from being activated [13], [14]. Inserting well-taps, which consists of well-contacts, in SRAM cell area also mitigates SEL [15]. All these methods increase the circuit area and standard SRAM macro needs to be re-designed.

On the other hand, process modification instead of design modification is an alternative approach. Using epitaxial wafer or thick wafer helps to reduce SEL, but its efficiency is quite limited [16]. It is known that well configuration changes SEL sensitivity. Using a deep N-well (DNW) prevents SEL effectively [17], where DNW is a popular process option in CMOS manufacturing processes and it is easy to be applied. However, the DNW application accompanies an undesirable side effect that single event upset (SEU) increases, since parasitic bipolar action (PBA) becomes more likely to occur [18]. Consequently if the increase in SEU rate due to DNW is not acceptable in products, ECC, which requires SRAM re-design, must be adopted despite its overheads in speed and area. Meanwhile, our preliminary work pointed out that Deep P-well (DPW) could contribute to SEL prevention [19]. Desirably, DPW does not increase SEU rate, whereas DNW elevates SEU rate. However, this evaluation

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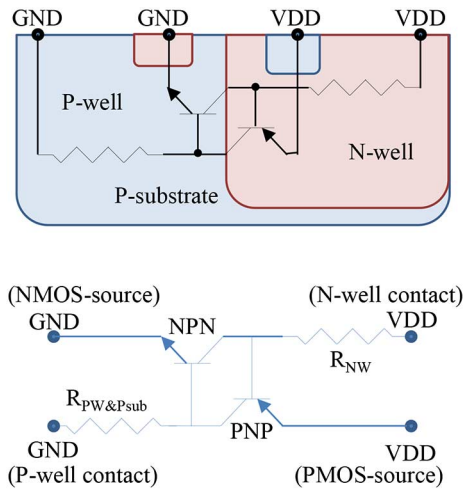

Fig. 1. Schematic of parasitic bipolar transistors contributing to SEL in a typical CMOS structure.

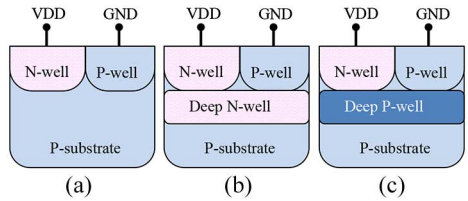

Fig. 2. Well configurations; (a) twin-well (2 W), (b) ordinary triple-well with deep N-well (DNW) and (c) with deep P-well (DPW). (a) w/o DW(twin-well) (b) w/ DNW(triple-well) (c) w/DPW.

was carried out only for a single design in 90 nm. In addition, dependence of SEL prevention on well doping profile was not studied.

In this work, we comprehensively study well configurations including ordinary twin-well without deep-well, triple-well with DNW and triple-well with DPW in terms of SEL tolerance, and give implications on the selection of well configuration taking into account both SEL and SEU. The dependences of SEL rate on well-tap interval in twin-well, well dose amount of twin-well, and dose amount of DPW are newly evaluated in this work. In addition, this paper includes a discussion on the mechanism of DPW for SEL prevention from two aspects; gain of parasitic bipolar transistors and stability of well potential. Well resistivity reduction thanks to DPW, which helps stabilize well potential, is experimentally confirmed. This work also shows that DPW is comparable or might be more effective for SEL prevention than CLD both in 55 nm and 90 nm.

The rest of this paper is organized as follows. Section II explains design of experiments to explore well configurations for minimizing SEL. Section III to V show measurement results of neutron irradiation tests. Based on these measurement results, we will discuss how well configuration should be selected in Section VI. Also, a comparison between CLD and DPW is presented there. Finally, concluding remarks are given in Section VII.

II. Experiment Design

This paper explores well configurations in terms of SEL and SEU rates based on experimental results of neutron irradiation tests. To achieve this, we need to prepare a comprehensive design of experiments consisting of test chip design and irradiation test setup. In this work, our target circuit is SRAM.

We first focus on test chip design. There are three well configurations under our consideration; twin-well without deep-well, triple-well with DNW and triple-well with DPW shown in Fig. 2, where these three well configurations are hereafter abbreviated to 2 W, DNW and DPW. To evaluate the impact of these well configurations on SEL and SEU, test chips should include these well configurations. SEL and SEU are thought to depend on well-tap interval and well dose amount, and then it is desirable to prepare test chips having different well-tap intervals and well dose amounts. In addition, to assess the dependence of SEL and SEU on technology nodes, test chips fabricated in different technology nodes need to be tested.

To cover these requirements, we prepared twelve test chip designs listed in Table I. Each test chip includes SRAM whose SRAM cell consists of conventional 6 T cells. Five designs were fabricated in 90 nm process and the other seven designs were fabricated in 55 nm process, where all the twelve designs were manufactured with P-substrate epitaxial wafers. DNW or DPW was formed across the whole chip except I/O area. DESIGN-A to -I have various well-tap intervals. DESIGN-J and -K are included to evaluate the effectiveness of SEL prevention with CLD. All the fabricated test chips were assembled on plastic packages with wire bonding.

We next examine irradiation test setup. When evaluating SEL, data pattern dependence could be observed. In addition, test types, i.e. static and dynamic tests, may show different tendencies.

We thus performed eight tests listed in Table II using the test chips in Table I. TEST-1 aimed to investigate the dependence of SEL and SEU on test type and data pattern using test chips of DESIGN-A(2 W). Fig. 3 illustrates static and dynamic tests we performed. In the static test, all SRAM bits were written, and were read after fifteen minutes passed. In the dynamic test, once the data were written, the data were repeatedly read until one hundred upsets were observed. This result will be presented in Section III-A. Based on this experimental result, we will choose test type and data pattern for the successive tests. Next, TEST-2 and -3 evaluate the impact of well-tap interval on SEL in 55 nm and 90 nm, respectively. DESIGN-E, -F, G and–I are used for TEST-2, and DESIGN-B, -C, and–D are used for TEST-3, where all the test chips used here were manufactured in twin-well process. These results will be presented in Section III-B.

TEST-4 evaluates the impact of 2 W, DNW and DPW on SEL and SEU using DESIGN-D in 90 nm. In this test, four 2 W test chips having different dose amounts, one DNW test chip and one DPW test chip were irradiated. Using the four 2 W test chips, the dependence of SEL on dose amount can be examined in TEST-4. This result will be discussed in Section IV.

SEL in DPW is studied further. TEST-5 studies the relation between DPW dose amount and SEL prevention efficiency. This result will be discussed in Section V.

TABLE I
SUMMARY OF TEST CHIP DESIGNS. WELL-TAP INTERVAL VALUES ARE NORMALIZED BY THAT OF DESIGN-B

Design	Tech-nology	Well-tap interval (normalized)	Well tap area / cell area	CLD	Well configuration*
DESIGN-A	90 nm	3.16	3.3%	No	2W (1), DPW (1)
DESIGN-B	90 nm	1.00	10.4%	No	2W (1)
DESIGN-C	90 nm	2.76	3.8%	No	2W (1)
DESIGN-D	90 nm	3.33	3.1%	No	2W (4), DNW (1), DPW (1)
DESIGN-E	55 nm	0.50	13.6%	No	2W (1)
DESIGN-F	55 nm	1.00	6.8%	No	2W (1)
DESIGN-G	55 nm	1.04	6.7%	No	2W (1), DPW (2)
DESIGN-H	55 nm	1.57	4.4%	No	2W (1),
DESIGN-I	55 nm	2.00	3.4%	No	2W (1)
DESIGN-J	55 nm	1.04	6.7%	Yes (added to DESIGN-G)	2W (1), DPW (1)
DESIGN-K	90 nm	3.16	3.3%	Yes (added to DESIGN-A)	2W (1), DPW (1)

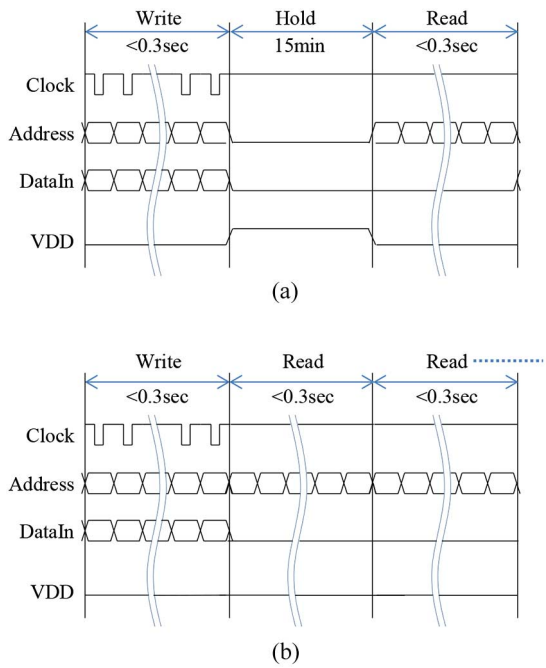

Fig. 3. Two types of test; (a) static and (b) dynamic tests.

Finally, Section VI summarizes the results of TEST-1 to -5 and gives a recommendation for selecting the best well configuration for SEL and SEU. In addition, SEL prevention efficiency of DPW will be compared with CLD, where CLD efficiency is evaluated in TEST-6 and -7.

The tests of TEST-1 to TEST-7 were performed with the spallation (board energy) neutron beams of Research Center for Nuclear Physics (RCNP) at Osaka University, the Weapons Neutron Research Center at Los Alamos Neutron Science Center (LANSCE), and Atmospheric-like Neutrons from thIck TArget (ANITA) of the Svedberg Laboratory at Uppsala University [20], [21]. These neutron beam energy spectra are similar to the sea level spectrum as shown in Fig. 4 and suitable for evaluating single event effects against terrestrial neutrons. On the other hand, to exclude any possible differences between beams, we only compare SEL rates measured at a single beam.

The occurrence of SEL was counted when unusual current was observed in power supply line, where the unusual current was assumed to be higher than the usual current by ten percent or more. For counting SEL, the current was monitored at five-second interval. The read operation was performed according to the timing chart shown in Fig. 3, regardless of SEL occurrence. In case that the current in power supply line exceeded a threshold value, on the other hand, the running test was immediately stopped to prevent the test chip from being permanently damaged.

III. DEPENDENCE ON TEST TYPE, DATA PATTERN AND WELL-TAP INTERVAL

First, we investigate the dependence of SEL sensitivity on test conditions; data pattern stored in SRAM and test types of dynamic and static tests (TEST-1). We also present the dependence on well-tap interval (TEST-2 and -3).

A. Dependences on Test Type and Data Pattern (TEST-1)

We performed TEST-1 to clarify a test condition in which SEL is more likely to occur. In this test, checker board (CHB) and all same data (ALL0/1) patterns were used. Fig. 5 shows the test result. Under static test, the dependence on written data pattern was hardly observed. On the other hand, the test type could affect SEL rate. However, the observed difference was within the error bars of 99% confidential level. This result of TEST-1 turns out that the test type and written data pattern are not critical factors for evaluating SEL in irradiation test. We evaluate SEL via static test with CHB pattern in TEST-2 to -5. Besides, SRAM operation could be affected by CLD, and hence dynamic test is selected for TEST-6 and -7.

B. Dependences on Well-Tap Interval (TEST-2 and -3)

We next carried out TEST-2 and TEST-3 to investigate the dependence on well-tap interval. As explained in the introduction section, resistors of R_{NW} and $R_{PW\&Psub}$ in Fig. 1 are key parameters for SEL sensitivity, and these depend on well-tap interval.

Fig. 6 shows the measured SEL rates in 55 nm (TEST-2). The well-tap interval values in Table I, Fig. 6 and Fig. 7 are normalized by the value of DESIGN-B. The result suggests that there is a threshold value of well-tap interval that drastically changes SEL sensitivity. SEL rates were keeping low for 0.5 and 1.6 well-tap intervals while SEL rate increased by two orders of

TABLE II
LIST OF IRRADIATION TESTS

TEST	Purpose	Test Chip	Facility	VDD	Temp.	Section
TEST-1	Evaluate dependence on test type and data pattern	DESIGN-A (2W)	ANITA	1.2V	RT*	IIIA
TEST-2	Evaluate dependence on well-tap interval in 55 nm	DESIGN-E (2W), DESIGN-F (2W), DESIGN-G (2W), DESIGN-H (2W), DESIGN-I (2W)	RCNP	1.2V	RT*	IIIB
TEST-3	Evaluate dependence on well-tap interval in 90 nm	DESIGN-B (2W), DESIGN-C (2W), DESIGN-D (2W)	RCNP	1.2V	RT*	IIIB
TEST-4	Evaluate dependence on well configuration (dose amount & 2W/DNW/DPW)	DESIGN-D (2W with four different dose amounts, DNW, DPW)	RCNP	1.2V	RT*	IV
TEST-5	Evaluate dependence on dose amount in DPW	DESIGN-G (2W, DPW with two different dose amounts)	RCNP	1.2V 1.4V	RT*	V
TEST-6	Compare SEL prevention efficiency between CLD and DPW in 55 nm	DESIGN-J (2W, DPW)	ANITA	1.1V 1.2V 1.3V	85C	VI
TEST-7	Compare SEL prevention efficiency between CLD and DPW in 90 nm	DESIGN-A (DPW) DESIGN-K (2W, DPW)	LANSCE	1.2V 1.3V	RT* 85C	VI

* Room temperature

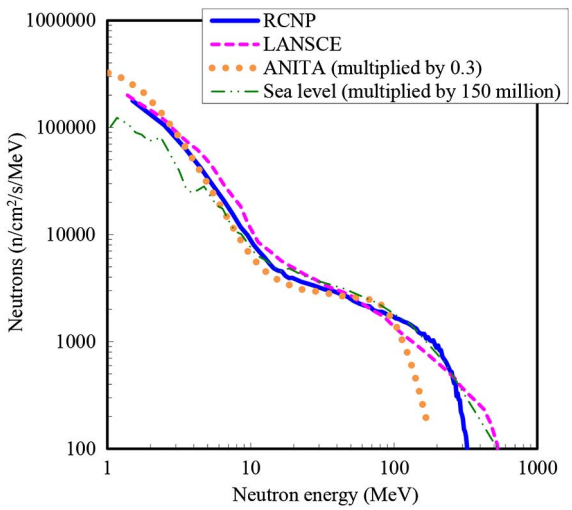

Fig. 4. Spectra of RCNP, LANSCE, ANITA, and Sea level from JEDEC [4], [20], [21]. Spectra of ANITA and Sea level are multiplierd by 0.3 and 150 milion, respectively.

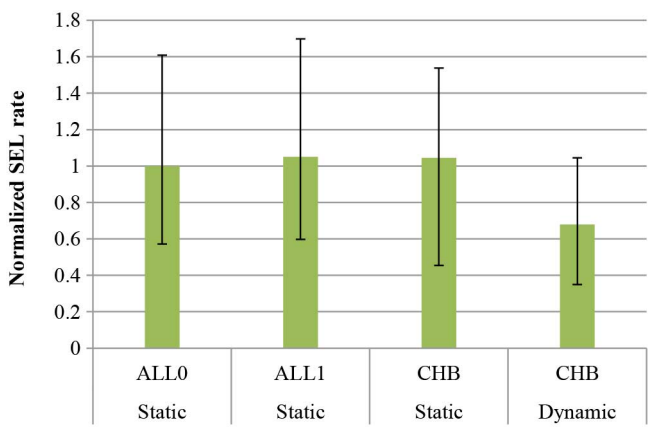

Fig. 5. TEST-1 result. SEL rates at 1.2 V on CHIP-A (2 W) with error bars at 99% cofidential level. SEL rates are normilized by the SEL rate for static test with ALL0 pattern.

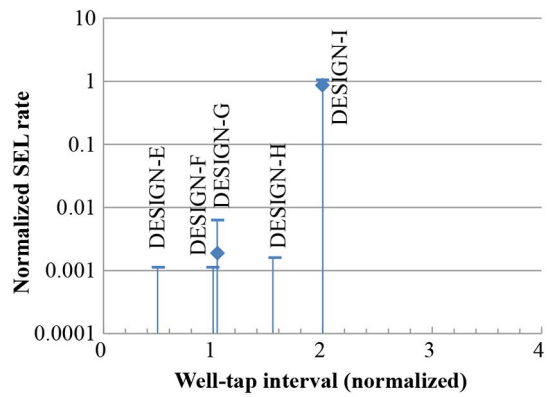

Fig. 6. TEST-2 result. SEL rates in 55 nm SRAM at 1.2 V on DESIGN-E (2 W), DESIGN-F (2 W), DESIGN-G (2 W), DESIGN-H (2 W) and DESIGN-I (2 W) with error bars at 99% cofidential level as a fucction of well-tap interval. SEL rates are normilized by the SEL rate of DESIGN-D(2 W) shown in Fig. 7. Note that no SELs were observed in DESIGN-E, -F and–H.

magnitude in case of 2.0 well-tap interval. A similar tendency was observed in 90 nm SRAM and this is shown in Fig. 7. The threshold value was different, but the SEL rate for 3.3 well-tap interval of DESIGN-D was higher than that for 2.8 well-tap interval of DESIGN-C by two orders of magnitude.

These results also indicate that even at room temperature and normal voltage, SEL can be observed especially in SRAM with large well-taps interval. In SRAM design, the well-tap interval should be smaller than such a threshold value. Adding more well-taps leads to shorter well-tap interval and higher SEL tolerance, but the area overhead of the well-tap is not negligible as shown in Table I. Here, the cell area does not include the well-tap area. To minimize the area overhead of the well-tap, we need to carefully evaluate the threshold value. On the other hand, when evaluating the SEL prevention efficiency with a limited irradiation beam time, SRAM with large well-tap interval can be a good DUT, since the number of SEL occurrence could be large.

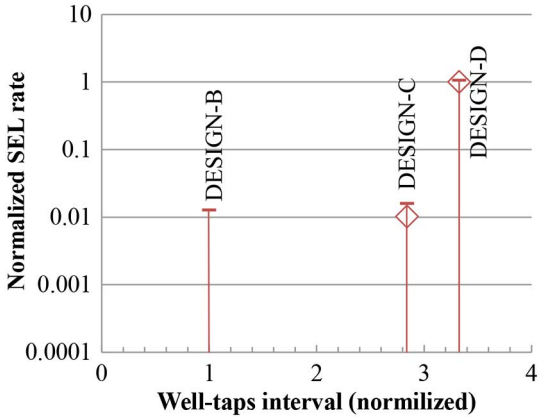

Fig. 7. TEST-3 result. SEL rates in 90 nm SRAM at 1.2 V on DESIGN-B (2 W), DESIGN-C (2 W) and DESIGN-D (2 W) with error bars at 99% cofidential level as a fucction of well-tap interval. SEL rates are normilized by the SEL rate of DESIGN-D (2 W). Note that no SELs were observed in DESIGN-B.

IV. Dependence of SEL on Well Configurations (TEST-4)

This section evaluates SEL and SEU dependence on well configurations using DESIGN-D, which was the most SEL sensitive design in TEST-3. We fabricated test chips of DESIGN-D with six different conditions of well process listed in TABLE III. Note that all the DESIGN-D test chips were manufactured with the same masks and processes except the well process. The measured neutron-induced SEL rates are shown in Fig. 8.

First, dose amount difference in 2 W is discussed. The SEL rate dropped to 70% due to the 20% increase in impurity (Phosphorus) dose amount of P-well (W0 vs. W4). When both the N- and P-well dose amounts increased by 50%, the SEL rate decreased to 40% (W0 vs. W2). The increase in the well dose amount lowers the gain of parasitic bipolar transistors, which contributed to SEL reduction. In addition, the gain decrease reduces the SEU rate. On the other hand, the 4X increase in the dose amounts did not bring further SEL reduction (W2 vs. W6). The SEL rate reduction by increasing well doping was at most 60%.

We also evaluated SEL of DNW and DPW SRAM. Fig. 8 shows that using DNW is more helpful for SEL prevention than the increase in well dose amount (W3 vs. W2). We observed two SELs in the DNW SRAM (W3) while no SELs occurred in the DPW SRAM (W1) during the same irradiation time. DPW could have higher SEL prevention capability than DNW (W3 vs. W1) with 68% likelihood.

DNW decreased SEL rate, but it increased SEU rate. SEU rate of DNW SRAM (W1) increased by about 20% compared to twin-well SRAM (W0). Generally, a 20% increase in SEU is not large enough to change the decision on whether ECC is required, but still an increase in SEU is an undesirable side effect for chip reliability. Reference [22] reported that DNW doubled SEU rate, and we need to pay a certain amount of attention to this side effect. On the other hand, DPW contributed to not only SEL prevention but also SEU reduction. Fig. 8 shows that DPW reduced SEU rate by more than 20%. Among six well configurations in Table III, DPW configuration (W1) was the best in terms of both SEL and SEU. DNW configuration (W3) attained the second lowest SEL while SEU rate increased by 20%. In the following sections, we further discuss DPW which attained the highest SEL prevention.

TABLE III
Well Process Conditions for Design-D

Wafer	*Symbol*	*N-well dose amount*	*P-well dose amount*	*DNW*	*DPW*
W0	Ref.	1.0 (normalized)	1.0 (normalized)	No	No
W4	NW+	1.0	1.2	No	No
W2	PNW+	1.5	1.5	No	No
W6	PNW++	4.0	4.0	No	No
W3	DNW	1.0	1.0	Yes	No
W1	DPW	1.0	1.0	No	Yes

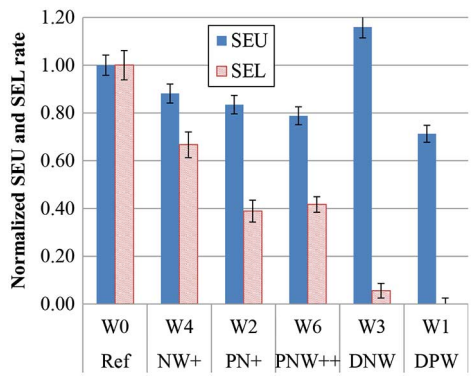

Fig. 8. TEST-4 result. SEU and SEL rates in six well process coditions listed in TABLE III. SEU and SEL rates are normilized by SEU and SEL rates of W0 (reference), respectively.

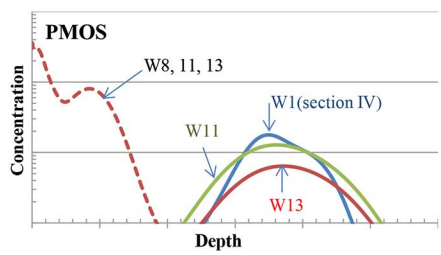

Fig. 9. N-well and DPW profiles of wafer of W1, W8, W11, W13. Right mountain-like curves correspond to DPW.

V. Prevention Efficiency on Deep P-Well (TEST-5)

This section investigates dependence of SEL mitigation efficiency on DPW doping profile. We performed neutron irradiation test on CHIP-G, where test chips were manufactured with three well configurations; 2 W and two DPW processes having different DPW dose profiles (W 11 and W 13 in Fig. 9). The dose amount of W 11 in DPW region is twice higher than that of W13. W1, which is included in Table III, is also plotted for reference.

Fig. 10 shows that both the DPW test chips (W11 and W13) achieved high SEL prevention and no SELs were observed in W11 and W13, where only 1.4 V test was performed for W11

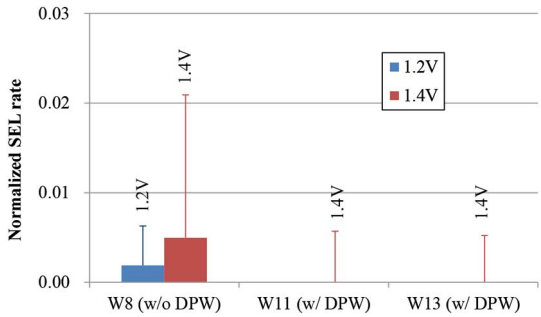

Fig. 10. TEST-5 result. SEL rate in W8, W11, W13 of DESIGN-G. SEL rates are normilized by SEL rate of DESIGN-C (2 W) with ALL0, static test condition shown in Fig. 7. Note that no SELs were observed in W11 and W13.

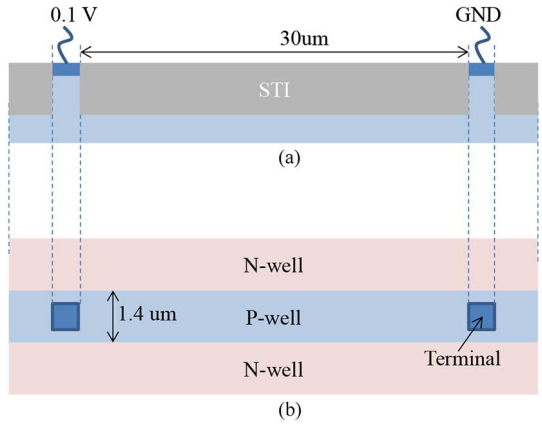

Fig. 11. (a) cross section and (b) top view of P-well resistor monitor.

and W13. Note that SEL is likely to occur at higher supply voltage, and hence the voltage of 1.4 V, which is higher than nominal supply voltage, was selected for the irradiation test. The achievable SEL prevention effects of W11 and W13 were not distinguishable in this test. On the other hand, the SEL rates of W11 and W13 were less than 1 FIT/Mbit for a flux of 13 neutron/hour/cm^2 (the flux at New York) [4] at a 90% confidence level. For achieving 1 FIT/Mbit SEL rate, the DPW doping profile did not play an important role. This observation is desirable since it makes accurate process control unnecessary in DPW process and makes it easier to apply DPW to SRAM for SEL prevention. It also should be noted that no SELs occurred in all the tests with DPW test chips (W1, W11 and W13), not only in TEST-5 but also TEST-4, -6 and -7 in our irradiation tests, where TEST-6 and -7 will be presented in Section VI.

We next discuss how DPW contributes to SEL prevention from two aspects. The first aspect is the gain of parasitic n-p-n bipolar transistor, which consists of N-drain, P-well and N-well, and the gain decreases due to an increase in effective accepter concentration in P-well. This is consistent with a fact that higher doping in twin-well also reduced SEL rate in TEST-4 (W0, W2, W4 and W6). The second aspect is the stability of well potential. DPW makes the P-well resistivity lower, which helps suppress well potential variation. To confirm this, we measured well resistance with and without DPW using a test structure to monitor the well resistor shown in Fig. 11. The resistance between two terminals, which included the resistance of two well contacts, was measured via wafer probing. P-well resistance with DPW was about 60% lower than that without DPW as shown in Table IV. On the other hand, N-well resistances with and without DPW were the same, since the volume of N-well was not changed. The reduction of P-well resistance stabilizes well potential and makes parasitic bipolar transistors less likely to be activated [9].

TABLE IV
NORMALIZED RESISTORS OF WELL WITH AND WITHOUT DPW

	w/o DPW	w/ DPW
N-well	1.0 (normalized)	1.0
P-well	1.0 (normalized)	0.4

VI. DISCUSSION

We presented the impact of well configurations on SEL in the previous sections, and showed that the following three well configurations were helpful to suppress SEL; (1) highly doped twin-well structure, (2) triple-well structure with DNW and (3) triple-well structure with DPW. On the other hand, these configurations have different SEL mitigation efficiencies and different costs for adoption. These differences are discussed in this section.

Increasing well dose amount in ordinary twin-well process reduced SEL occurrence. Although the reduction ratio was moderate (at most 60% in our experiment), this is not accompanied with SEU increase. More importantly, this can be done via process tuning, and no new manufacturing processes need to be developed or added. If the SEL reduction of up to 60% is sufficient for the products, this approach is the most suitable.

DNW attained high prevention efficiency for SEL. DNW is a popular option provided in general CMOS manufacturing processes and it is easy to be applied at a cost of additional masks. However, DNW increased SEU rate. If the SEU rate increase due to DNW is acceptable or ECC is already adapted in the products, DNW is a good candidate for preventing SEL with a reasonable cost. Especially, this is attractive for fabless design companies since no special requests need to be given to a foundry.

DPW is the most effective for SEL reduction. In addition, SEU is also reduced. For the products in which the device reliability is the primary metric, DPW can be the best option. However, DPW is not a common process option provided by foundries, and hence there is a cost impact to develop a new DPW process. If this cost is cheaper than other solutions, such as circuit-level solutions, one of which will be explained in the next paragraph, DPW can be highly recommended. Here, it should be noted that the development of DPW is not technically difficult since DPW can be constructed by deep Boron ion implantation and this is often available in foundries for power MOS devices and sensor devices [23].

To clarify the advantage of DPW, we evaluated the SEL prevention efficiency of CLD [13], [14] (TEST-6 and -7). TEST-6 was performed on DESIGN-J (2 W) and DESIGN-J (DPW). As a CLD, a 5 um wide PMOS was inserted in series to each line which powered the SRAM cells in a column. The gate of the PMOS was connected to ground (GND). Fig. 12 shows the test

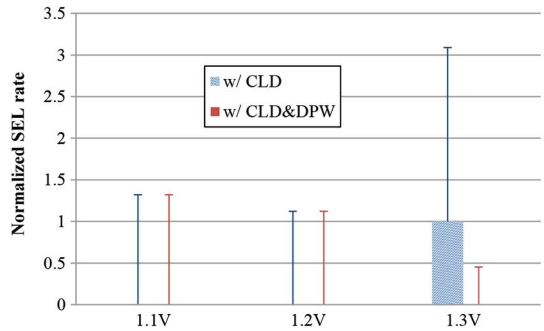

Fig. 12. TEST-6 result. SEL rates of DESIGN-J at 85 degree celcius. SEL rates are normilized by SEL rates at 1.3 V. Note that no SELs were observed with CLD and DPW, and at 1.1 V and 1.2 V with CLD.

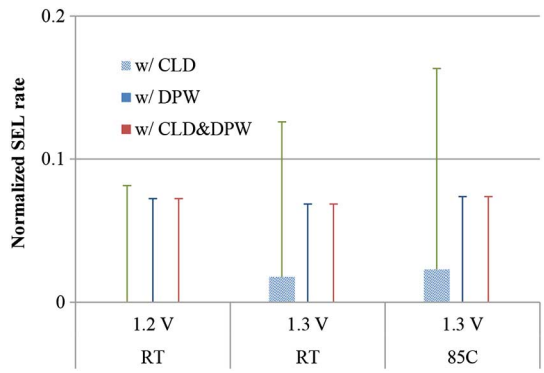

Fig. 13. TEST-7 results. SEL rates of DESIGN-A and DESIGN-K at room temperature (RT) and 85 degree celcius. SEL rates are normilized by SEL rate of DESIGN-A (2 W) with ALL0, static test condition shown in Fig. 5. Note that no SELs were observed with CLD at 1.2 V and with DPW and with CLD and DPW.

result that SEL was observed even with CLD in the 2 W test chip while no SEL was observed in the both DPW test chips with and without CLD.

TEST-7 was performed on DESIGN-A (DPW) and DESIGN-K (2 W and DPW). DESIGN-A and DESIGN-K had the same SRAM macros, and only the difference is that CLD was inserted in DESIGN-K. In the test chip without DPW, SEL was observed even with CLD as shown in Fig. 13, whereas no SELs were observed in the DPW test chips. Note that the SEL rates of the vertical axis in Fig. 13 are normalized by that of DESIGN-A (2 W), which is the SRAM without CLD in ordinary twin-well shown in Fig. 5. This means that the CLD was also helpful for SEL prevention and suppressed SEL by more than 99%. On the other hand, the SEL prevention by DPW can be expected to be similar or might be better than that of CLD while the number of observed SELs in this experiment was limited and a significant difference was not observed.

We finally discuss the performance penalty due to DPW. One might think that DPW could change the SRAM performance or could increase manufacturing variation by an increase in the number of dopants in the p-substrate since random dopant fluctuation is one of the major sources of manufacturing variation. However, it should be noted that DPW changed the doping profile at a deep region and the doping profile near MOS devices was unchanged as shown in Fig. 9. The number of dopants in

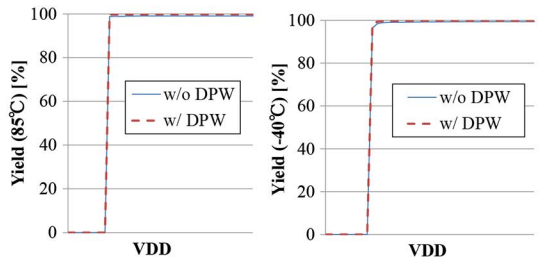

Fig. 14. Chip level yields measured by wafer level test in 85 and -40 degree Celsius.

the channel region is the source of manufacturing variation, and variation in such a deep well does not influence transistor performance. Consequently, the DPW profile (Fig. 9) should keep MOS performance and variation unchanged. To clarify this, we compared chip level yields of the chips with and without DPW.

Fig. 14 shows chip level yields evaluated by wafer level tests at 85 and -40 degree Celsius. In the tests, arbitrary data was written into SRAM, and 20 ms later all the data were read and checked. This test procedure was repeated for various supply voltages. To evaluate the SRAM yield, we tested 64 dies on a wafer. If there were some performance differences between SRAMs with and without DPW, such as in read and write access time and drive current balance between PMOS and NMOS, the yield would change. On the other hand, no difference was found in the yield evaluation results shown in Fig. 14. This result indicates that DPW neither change the performance nor increase manufacturing variation.

VII. Conclusion

This work experimentally demonstrated through neutron irradiation tests that altering well configuration could improve SEL immunity, and revealed that DPW, DNW and highly doped well reduced SEL rate. These three configurations for SEL prevention have different features. Increasing dose amount in twin-well can mitigate SEL without SEU increase, and at most 60% SEL reduction could be obtained via process tuning. DPW is the most effective solution to eliminate SEL occurrence, and no SELs were observed in our irradiation tests. Furthermore DPW is helpful to reduce SEU as well. While adoption of DPW adds extra cost to develop a new DPW process, the DPW process development itself is not technically difficult. The SEL prevention by DPW can be expected to be similar to or might be better than that of CLD. An advantage to select DNW for SEL prevention is that DNW is a common process option and can be easily adopted at a cost of additional masks. However, we need to pay attention to a fact that DNW increases SEU rate.

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