Reliability-Configurable Mixed-Grained Reconfigurable Array Compatible with High-Level Synthesis

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***Abstract*—This paper presents a mixed-grained reconfigurable VLSI array architecture that can cover mission-critical applications to consumer products through C-to-array application mapping. A proof-of-concept VLSI chip was fabricated in a 65nm process. Measurement results show that applications on the chip can be working in a harsh radiation environment.**

I. Introduction

With the exponential rate of enhancement both in transistor performance and integration scale, VLSI systems have been driving advancement of information systems. People and society, in the meantime, have been more and more dependent on the services provided by the systems, and now it becomes a social requirement to guarantee the reliability of the information systems and that of the VLSI systems accordingly.

On the other hand, as VLSI technology advances, non-recurring engineering (NRE) costs are significantly elevating, and nowadays only the highest-volume applications can accommodate the high NRE cost of custom SoC design. Therefore, reconfigurable VLSIs are drawing much attention as an alternative of SoCs development not only for small-volume consumer products but also mission-critical, such as space and medical, applications.

Coarse-grained reconfigurable architecture (CGRA) is inherently superior in soft error immunity to FPGA, since the amount of configuration bits is by orders of magnitude smaller than that of FPGA. Although there are several CGRA proposals for reliability (e.g. [1], [2]), none of them have been validated on silicon except [3]. Reference [3] successfully demonstrated a trade-off between soft error immunity and area; however, its compatibility with design tools is not well established since a state machine cannot be implemented.

We have developed a reliability-configurable array in which the reliability level for each processing element can be chosen flexibly depending on applications and environments [4]. This enables system designers to systematically trade off area for improving the soft error immunity without having a deep knowledge of reliability enhancement techniques. In addition, high-level design automation tools can be utilized to map an application from standard C programs taking into account a given reliability requirement. To support such a design tool [5], [6], the proposed architecture introduces 1-bit processing elements into CGRA of [3] for implementing state machines.

II. Proposed Architecture and Its Implementation

The proposed architecture consists of coarse-grained ALU clusters, fine-grained LUT clusters and memory clusters,

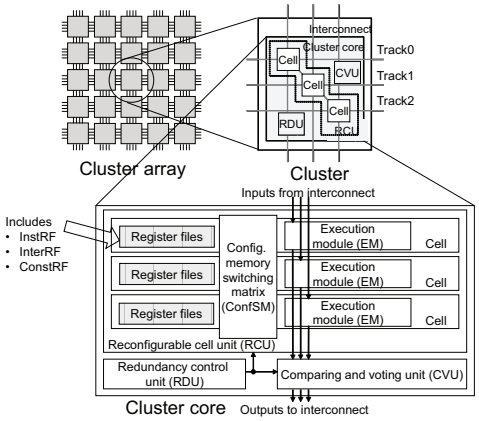

Fig. 1. Cluster and cluster interconnection.

where the basic element is noted as a cluster. The reliability level of each cluster can be configured individually for improving reliability-area trade-off with selective redundancy [7]. The basic architecture for ALU and LUT clusters is shown in Fig. 1. 20 LUT clusters are organized in a two dimensional array forming a LUT block. LUT blocks, ALU clusters and memory clusters are placed in a two-dimensional array (Fig. 2). As for dynamic reconfiguration, two classifications exist; state is for cycle-wise instruction selection of ALU with the interconnections unchanged, and context is for modifying interconnections. Designated LUT clusters are responsible for generating the state and context signals and these signals are distributed throughout the array.

ALU cluster includes three instruction register files (InstRF) for state-wise EM configuration, three interconnect registers (InterRF) for context-wise interconnection, and a context-wise constant register (ConstRF). The execution module (EM) performs logic operations, shifting and clamp functions in addition to arithmetic operations such as 16-bit multiplication, 16/17-bit signed and unsigned addition and subtraction. The reliability levels, which are enabled by RDU and CVU, are summarized in Table I. TMR, SMS and SMM offer different immunities to soft errors (SEU/SET: single event upset/transient) and capabilities of dynamic reconfigurability (#contexts). InterRF and ConstRF are protected by ECC (error correction code). All the register files are overwritten through ECC decoders or voters with refreshing clock for preventing error accumulation. The refreshing clock frequency trades reliability for power consumption. The EM in the LUT cluster is a 4-input LUT suitable for 1-bit processing, such as flag operations. LUT clusters can be cascaded to form a larger LUT, and provides TMR and SMM.

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TABLE I
REDUNDANCY AND RELIABILITY TO SOFT ERRORS IN THREE OPERATION MODES IN ALU CLUSTER. INTERRF AND CONSTRF ARE PROTECTED WITH ECC IN ALL THE THREE MODES.

Level	Redundancy		SEU in	SEU	SET	Utilization	
	InstRF	EM	InstRF	in EM	in EM	#contexts	#cells
TMR	3	3	D & R	D & R	D & R	3	3
SMS	3	1	D & R	D	ND	1	1
SMM	1	1	ND	D	ND	3	1

D & R : Detection and recovery, D : Detection, ND : Does not detect

As for memory cluster, while it contains only a dual-port SRAM macro protected by ECC, it is designed to be compatible with interconnect structure. There are two reliability levels; one provides dual-port access while the other gives single-port access. In the latter case, the other port is used for periodical refreshing to avoid error accumulation.

Figure 2 illustrates the mixed-grained array consisting 26 ALU and 6 memory clusters and 4 LUT blocks with the chip layout. Cyber Workbench [5], [6] customized for the proposed array constructs CDFG (control data flow graph) and synthesizes an RTL implementation taking into account given reliability specification [7]. Finally, the RTL implementation is mapped on the array through technology mapping and P&R.

The array was fabricated in a 65nm 12ML CMOS process. The die size is $4.2\times4.2\text{mm}^2$. The number of states and contexts are set to 16 and 3, respectively. Configuration is performed through a scan-chain consisting of 165,312 FFs. ALU, LUT and memory clusters include 120k, 4k and 99k gates, respectively. Thanks to dynamic configuration using states in FSM, area-efficient mapping becomes possible. For example, an edge detection filter can be implemented with 25 ALU clusters while 62 ALU clusters are needed without dynamic reconfiguration (i.e. in a single state). The reduction ratio of used clusters is 60%. The proposed architecture can exploit such latency-area exploration in high-level synthesis.

III. MEASUREMENT RESULTS

The maximum frequency can be limited by the distribution of state and context signals, and was measured using a PLL on the chip. Results show that the maximum frequency possible to propagate state signals is 240MHz, while it is 165MHz for context signal.

To validate the functionality and reliability of the architecture, a demonstration using two mappings of SMM and SMS was performed (Fig. 3). The chip receives a live data stream from a video camera, processes it and sends it to a monitor demonstrating the processed stream. The mapping of negative filter was generated from a C source code.

A snapshot of the results is shown in Fig. 4. After positioning Am-241 foil whose flux is $9\times10^9\text{cm}^{-2}\text{h}^{-1}$ over the chip, it was observed that SMS mapping continued to output the processed video as expected in 200s. On the other hand, SMM mapping got destroyed in 2 s due to SEUs in the configuration registers and the video processing stopped within 10 s in all four trials. Thus, the proposed architecture enables reliable operation under radiation through application mapping.

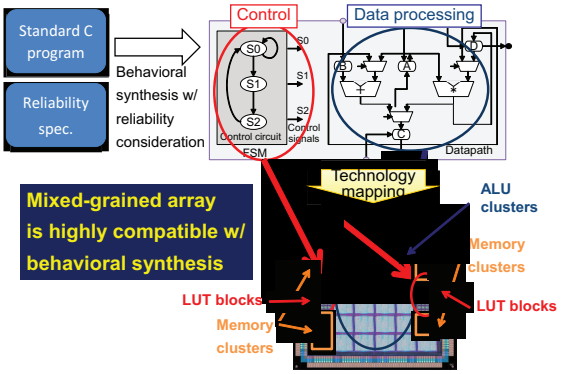

Fig. 2. Designed reconfigurable array and design flow.

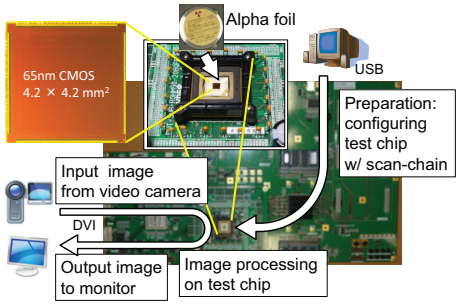

Fig. 3. Demonstration setup.

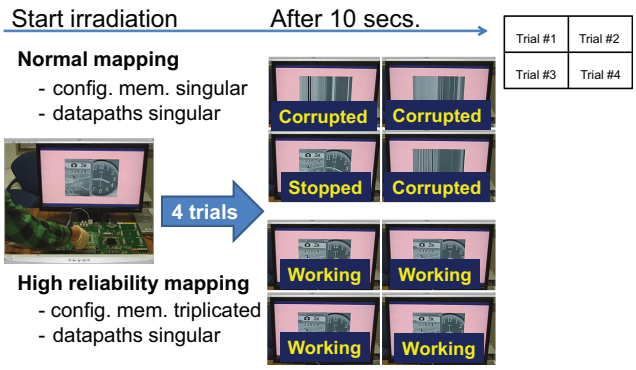

Fig. 4. Results of image processing under irradiation

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