Toward Robust Subthreshold Circuit Design – Variability and Soft Error Perspective –

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***Abstract*—Subthreshold circuits are drawing attention for ultra-low power application. However, subthreshold circuits have inherent problems that their performance is extremely sensitive to manufacturing and environmental variability and they are susceptible to soft errors. This paper discusses robust subthreshold circuit design from variability and soft error perspective.**

I. Introduction

Subthreshold circuits are promising to severely energy-constrained devices with low demands for their operation speeds, such as devices for habitat monitoring, health monitoring, structural health monitoring, and biomedical equipment. Recently not only such severe low energy devices but also middle performance chips are developed [1], [2]. In addition as a new application, a cubic-millimeter wireless intraocular pressure sensor is proposed [3]. In this paper, near-threshold circuits are included in subthreshold circuits.

Subthreshold circuits have a problem that their performances are extremely sensitive to manufacturing variability and environmental variability such as temperature and supply voltage fluctuations. In addition, subthreshold circuits have been thought to be vulnerable to soft errors.

We have worked for putting subthreshold circuits robust to practical use at device, circuit and CAD levels. At device level, we constructed a transistor variability model that reproduces subthreshold circuit performance [4], and evaluated soft error immunity of subthreshold SRAM [5]–[9]. At circuit level, adaptive performance control is studied parting from conventional worst-case design [10]. For implementing and verifying adaptive control, stochastic evaluation frameworks of timing error and power consumption are developed [10], [11]. Furthermore, we propose a self-timed processor to cope with large variation in memory access time [12].

In this paper, adaptive speed control for overcoming variability is first introduced, and the soft error susceptibility of subthreshold SRAM is presented.

II. Run-time Performance Adaptation

Vth variation due to manufacturing variability and temperature fluctuation significantly varies speed and power consumption of subthreshold circuits. If adding up worst-cases for each variation factor, power dissipation may increase more than 10x. We therefore devised an adaptive speed control scheme [10] (Fig. 1). The timing error predictive flip-flop (TEP-FF) causes a setup violation earlier than the main flip-flop due to the inserted delay element. This error signal is used as a warning signal indicating a shortage of timing slack, and the circuit is speeded up or down according to this signal.

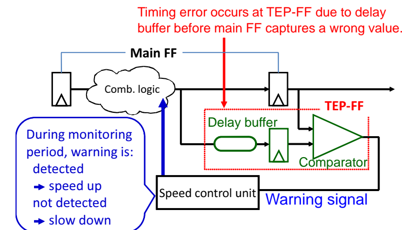

Fig. 1. Run-time adaptive speed control with TEP-FF [11].

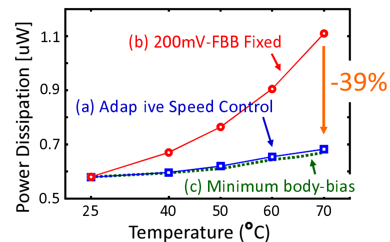

Fig. 2. Measurement result of speed adaptation (3MHz, 0.35V) [10].

This adaptive speed control was applied to a 32-bit Kogge-Stone adder. A test chip was fabricated in 65nm process. Figure 2 shows a measurement results under temperature variation. In this test chip, the circuit speed is adjusted by body-biasing. (a) corresponds to the proposed speed control, (b) is the power dissipation when 200 mV forward body-bias is given to satisfy the speed requirement at 25°C, and (c) is the power dissipation when the minimum body-bias is given at each temperature. This result shows that the power dissipation of the proposed speed control is close to (c) and the speed control is well working. Compared to conventional adaption of (b), the power dissipation is reduced by 40%. We also confirmed that 46% power reduction was possible compared to worst-case design for process and temperature.

This adaptive speed control involves a fundamental problem that timing errors cannot be completely eliminated. This is because the circuit could be slowed down excessively, if critical paths are not activated for a long time, the circuit could be slowed down excessively. However, this timing error is very difficult to evaluate in design time, since simulation is too slow for rare errors, such as an error per month. To enable design-time verification, we developed a stochastic error rate estimation method [11]. The necessary evaluation time was reduced by twelve orders of magnitude, which can guide design optimization of run-time adaptive system.

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III. Neutron-induced soft error

In terrestrial environment, alpha particle and neutron are major sources for soft error, especially neutron could be dominant. This section presents measurement results of neutron-induced soft errors in 10T SRAM over a wide range of supply voltages between 1.0 and 0.3 V reported in [6], [7]. This section also mentions future trends on neutron-induced soft error.

A test chip including a 256 kb 10T SRAM was fabricated in a 65-nm bulk CMOS process with triple well structure and irradiated with accelerated spallation neutron beam. This SRAM can operate even at 0.3 V, because the cross-coupled inverters are large enough to mitigate threshold voltage variability. The size of a memory unit is 4.4 μm $\times$ 0.8 μm.

Figure 3 illustrates the dependence of the SBU and MCU rates on the supply voltage. The MCU rate was derived by dividing the number of failing bits (for example, a "2b MCU" was considered to be two errors) by the measurement period. The SBU rate dramatically increases as the supply voltage is reduced. On the other hand, the dependence of the MCU rate on the supply voltage is smaller than that of the SBU rate. Previous work [13] has shown that the MCU rate is less sensitive to the supply voltage between 1.2 and 0.7 V and concluded that this is because most neutron-induced MCUs are caused by the parasitic bipolar action. Interestingly, however, the MCU rate shown in Fig. 3 slightly increases when the supply voltage is below 0.5 V. Remind that charge sharing and parasitic bipolar action have opposite directions in terms of supply voltage. While the parasitic bipolar action is the dominant mechanism of MCUs in the super-threshold region in our design, the effect of charge-sharing becomes larger in the subthreshold region, which results in the increase in the MCU rate between 0.3 and 0.5 V, as depicted in Fig. 3.

Next, the MCU distributions in the memory cells are shown in Fig. 4. A decrease in the supply voltage also increases the probability of large-bit MCUs due to the decrease in the critical charge. 6-bit MCU was observed at 0.3V.

Figure 5 shows the simulated SEU probability including both SBU and MCU per neutron flux as a function of critical charge at the incident angles of 60° and 0°. Individual contributions from secondary H (proton), He (alpha), and heavier ions to the SEU are separated for the result of 0° in Figure 5. There is little difference between the SEU probabilities at the angles of 60° and 0°. On the other hand, the critical charge of our 10T SRAM in 0.4-V operation is estimated by circuit simulation to be 1.4 fC. Therefore, He and heavier ions are the dominant secondary ions causing SEUs in 0.4-V operation because these ions occupy 89 % of the SEU probability at 1.4 fC of critical charge.

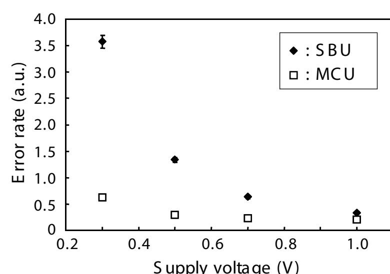

Fig. 3. SBU and MCU rates as a function of supply voltage of memory cell array [6]. SBU and MCU rates are plotted with error bars, where each error bar indicates $\pm 3\sigma$.

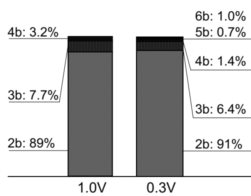

Fig. 4. Comparison of MCU distributions.

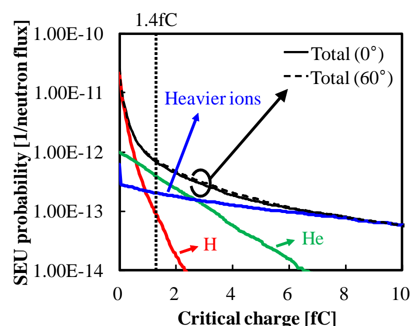

Fig. 5. Simulated SEU probability of each ion as a function of critical charge [7].

At 0.4V operation, protons are not dominant, but another newer result with other 90nm bulk SRAM at 0.19V presented a dramatic SEU increase, which is explained by proton contribution [8]. Another technology direction is SOI device, and [9] reports that ultra-thin-BOX SOI is helpful to mitigate SEU, especially MCU. Thanks to this, by introducing ECC for SBU, highly reliable SRAM can be obtained.

Acknowledgements

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