Preventing Single Event Latchup with Deep P-well on P-substrate

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***Abstract*—We propose a method that prevents single event latchup (SEL) using deep P-well on P-substrate. To confirm the effectiveness of the proposed method, SEL and single event upset (SEU) are evaluated for three well configurations; double-well, ordinary triple-well and the proposed deep P-well on P-substrate. Neutron irradiation test shows that the proposed method achieves SEL prevention without SEU increase.**

Keywords-component; Single Event Latchup (SEL); Double-well, Triple-well, Neutorn, Single Event, Soft-error, Latchup, Deep-well; SRAM, Terrestial environment.

I. INTRODUCTION

Single Event Latchup (SEL) is one of the most important reliability issues on SRAM based electron devices in terrestrial environment. SEL is an abnormal high-current state in a device caused by the passage of an energetic particle through sensitive regions in the device structure, and it results in the loss of device functionality. SEL can cause permanent damage to the device. Even if the device is not permanently damaged, the device needs to be turned off to recover from SEL [1]. This means popular error detection and corrections (EDACs) such as error correction code (ECC) are helpless to SEL.

SEL in a CMOS device occurs when the passage of a particle activates a parasitic p-n-p-n bipolar and the bipolar shorts power and ground [1]-[4]. The parasitic p-n-p-n bipolar consists of PMOS-source, N-well, P-well and NMOS-source as shown in Figure 1. Key parameters which influence SEL occurrence are resistors (R_{NW} and $R_{PW\&Psub}$ in Figure 1) and the current gains of the parasitic bipolar transistors (NPN and PNP in Figure 1). $R_{PW\&Psub}$ is determined from resistivity of the P-well and the P-substrate and the distance between the NMOS transistor and P-well contacts. Similarly, R_{NW} depends on the N-well resistivity and the distance between the PMOS transistor and the N-well contacts. The current gains are determined by doping concentrations in the well and the source region and the distance between well-junction and source regions.

To prevent SEL, several methods have been proposed. Adding a current-limiting device to power line can mitigate SEL by reducing the power supply current in the case of a latchup event [2][3]. This method involves additional area for the current limiting device, and an SRAM macro must be re-designed. Another approach to mitigate SEL is to use deep-N-well (DNW) on P-substrate, i.e. triple-well, and it can be readily applied to SRAM macro that has been already designed without area overhead [4]. However, triple-well increases single event upset (SEU) on SRAM especially multi cell upset (MCU) [5][6]. The DNW makes parasitic bipolar action (PBA) more likely to happen to NMOS since the DNW splits P-well and P-substrate and P-well potential becomes more sensitive to a particle strike.

In this work, we propose an SEL prevention method that uses deep P-well (DPW) on P-substrate. The DPW does not split any well areas, and consequently SEU rate does not increase. The SEL prevention efficiency and SEU rate are evaluated through a neutron irradiation test on three types of SRAMs; with DNW, DPW and without deep-well (DW), and the superiority of the proposed method is clarified.

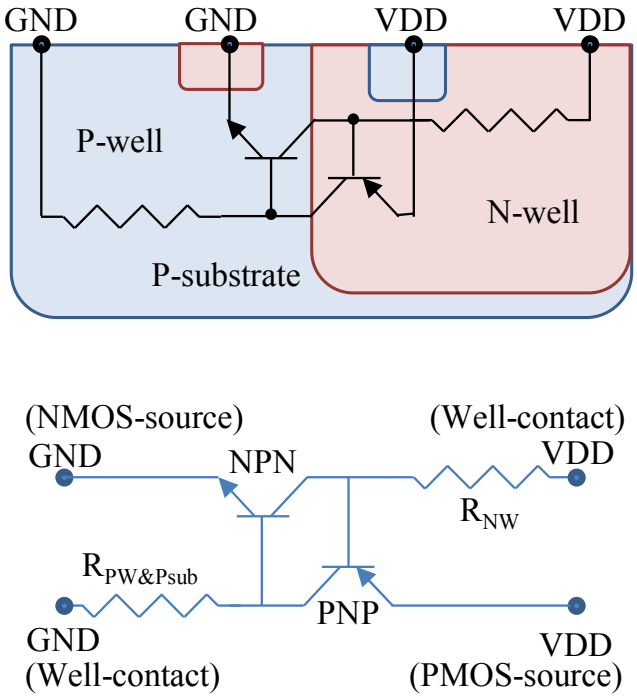

Figure 1. Schematic of parasitic bipolar transistors contributing to SEL in a typical CMOS structure.

II. PROPSOED PREVENTION METHOD

The proposed SEL prevention method put DPW under N- and P-wells on P-substrate as shown in Figure 2 and 3. The DPW can be expected to be easily adopted without changing design rule because DPW does not split any well area, which is different from DNW.

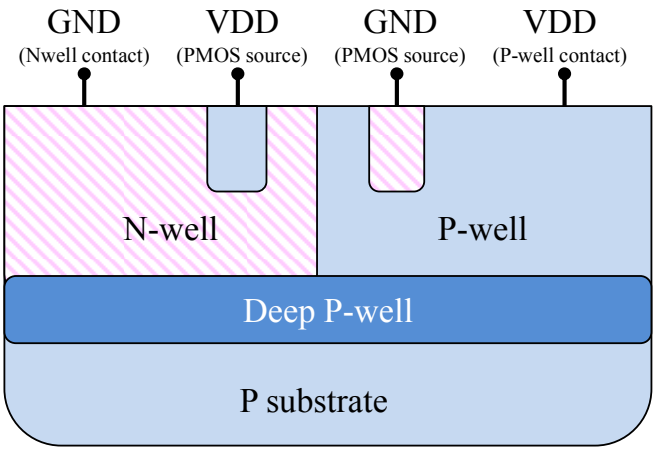

Figure 2. Deep P-well structure.

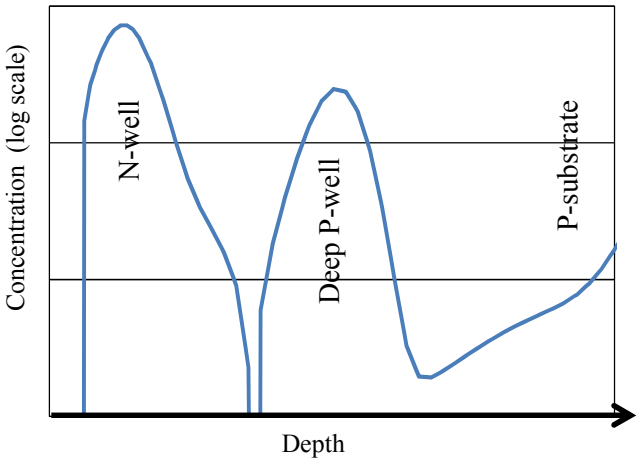

Figure 3. N-well and deep P-well profile.

The DPW is expected to have three effects contributing to SEL prevention. First, DPW decreases the resistance between SRAM cell and well-contacts ($R_{PW\&Psub}$ in Figure 1) and suppresses well potential variation. Second, the gain of parasitic n-p-n bipolar transistor, which consists of NMOS-source, P-well and N-well as shown in Figure 1, decreases due to an increase in effective accepter concentration in the base (p). Third, DPW could prevent the electrons which are generated below DPW from being collected to N-well although DPW does not isolate P-substrate and P-well like DNW.

III. EXPERIMENTAL PROCEDURE

We performed a neutron irradiation test for evaluating the efficiency of the proposed SEL prevention method at 25 degree Celsius. Figure 4 shows the setup of neutron irradiation test. This irradiation test was done with the spallation (board energy) neutron beam of Research Center for Nuclear Physics (RCNP) at Osaka University, where its energy spectrum is shown in Figure 5. We carried out static SRAM test.

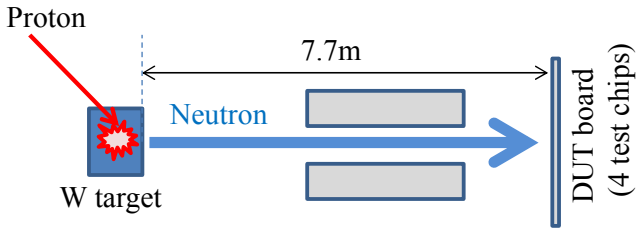

Figure 4. Setup of neutron irradiation test.

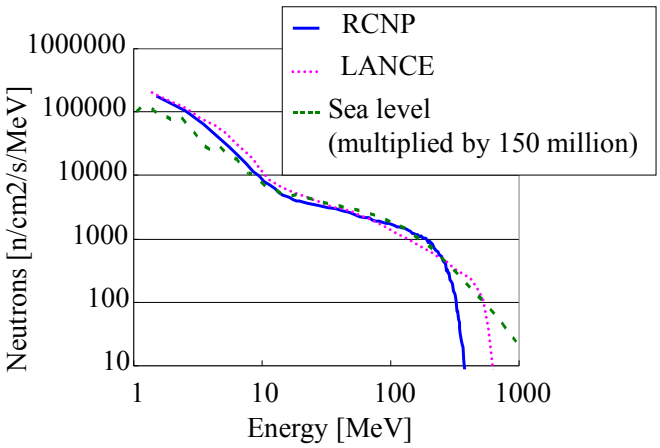

Figure 5. Neutron energy spectrum of RCNP neutron beam compared with those of LANSCE neutron beam and of atmospheric neutrons.

The test board has four SRAM test chips as shown in Figure 6. Power (VDD, VDE) and ground (GND) are shared by four chips on the test board. VDD and VDE are supply voltages given to memory and I/O, respectively. Ground is shared by memory and I/O in the test chip. The occurrence of SEL was counted when unusual current was observed on VDD, where the unusual current was assumed to be higher than the usual current by ten percent or more.

Each test chip includes about 2 Mbit conventional 6T-SRAM cells manufactured in 90 nm process technology. This means that the test board has about 8 Mbit. The test chips were manufactured with epitaxial wafers. The chip is assembled with a plastic package with wire bonding. To clearly observe the contribution of deep P-well to SEL prevention, we intentionally designed the SRAM macro having a larger well-tap interval. Note that in actual products, the well-taps are densely placed to suppress well potential variation.

We fabricated the test chips with three well configurations shown in Figure 7; double-well (i.e. without DW), triple-well with DNW and the proposed structure with DPW. The deep-well (DNW/DPW) was formed across the whole chip excepting I/O area. The concentration profiles on cross-section of N-well, DPW and P-substrate are shown in Figure 3. All the test chips were manufactured with the same mask and process except on the well configuration.

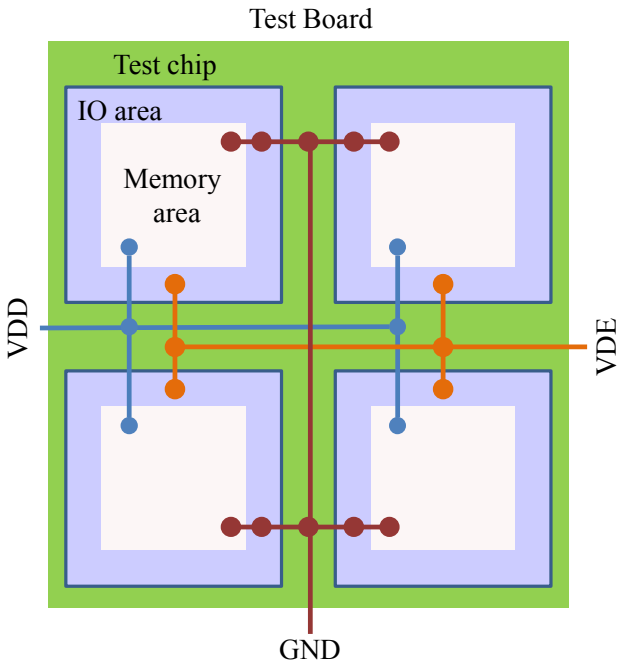

Figure 6. Configuration of test chip and board in neutron irradiation test.

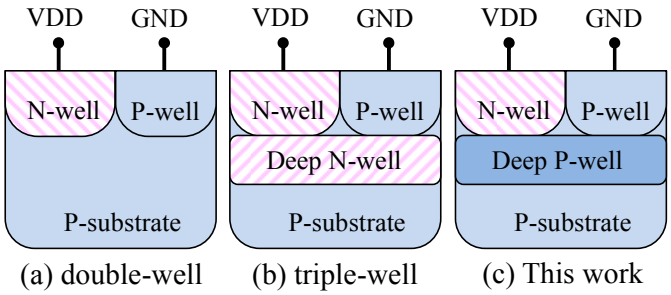

Figure 7. Well structures. (a) double-well, (b) ordinary triple-well with deep N-well, and (c) proposed structure with deep P-well.

IV. Results and Discussion

Table 1 shows the number of SELs observed in the neutron irradiation test. We observed no SELs in the proposed SRAM with deep P-well while nine SELs occurred in double-well (without DWs) SRAM. No SELs were observed in triple-well (with DNW) SRAM. The results indicate that the proposed method is helpful for SEL prevention. In this experiment, on the other hand, the difference between DPW and DNW in SEL prevention efficiency was not distinguishable.

Table 1. SEL counts in sixty minutes irradiation.

	1.0V	1.2V	1.3V	1.4V
Double-well (w/o deep well)	0	0	2	7
Triple-well (w/ deep N-well)	0	0	0	0
This work (w/ deep P-well)	0	0	0	0

Figures 8 and 9 show SEU and MCU rates, respectively. SEU and MCU rates of the proposed SRAM (with DPW) are the almost same as the rates of double-well SRAM (without DW) at 1.2V, although SEU and MCU rates of triple-well (with DNW) SRAM increase by 22% and 386%, respectively, compared to double-well SRAM (without DW).

The proposed SEL prevention method with DPW achieves high mitigation efficiency without increasing SEU rate. The mitigation efficiency of the proposed method is comparable with triple-well (with DNW). In addition, SEU rate of the proposed structure is comparable with that of double-well (without DW). The proposed method can have both the advantages; SEL prevention of deep N-well and SEU immunity of double-well.

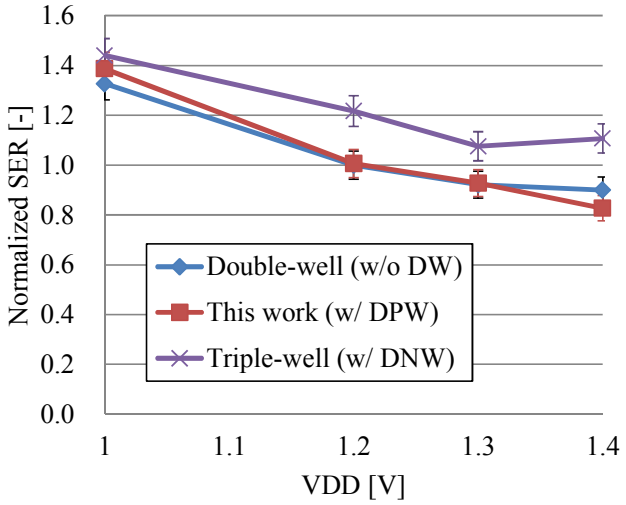

Figure 8. Neutron induced SEU (SBU+MCU) rates normalized by SEU rate of double-well (w/o DW) SRAM at 1.2 V.

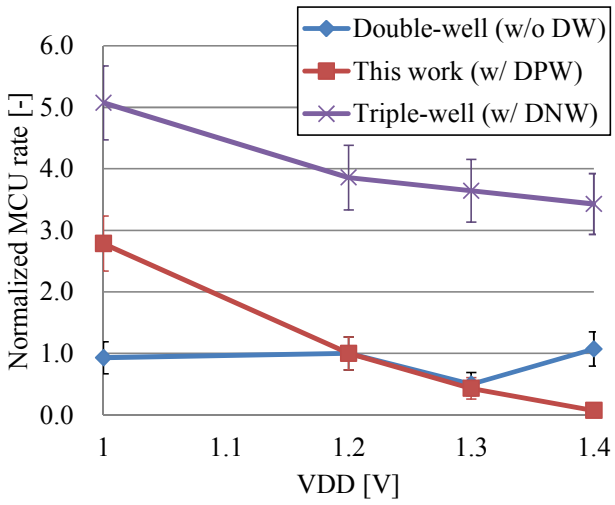

Figure 9. Neutron induced MCU rates normalized by MCU rate of double-well (w/o DW) SRAM at 1.2 V.

V. CONCLUSIONS

We proposed a method for preventing single event latchup (SEL) with deep P-well on P-substrate. To confirm the effectiveness of the proposed method, SEL and single event upset (SEU) were evaluated for three well configurations; double-well, ordinary triple-well and the proposed deep P-well on P-substrate. In neutron irradiation test, we observed no SELs in the proposed SRAM with deep P-well while nine SELs occurred in double-well (without DWs) SRAM. No SELs were observed in triple-well (with DNW) SRAM. This result confirms that the proposed method can prevent SEL without SEU increase.

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