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Proposal of Metrics for SSTA Accuracy Evaluation*

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SUMMARY With the recent advance of process technology shrinking, process parameter variation has become one of the major issues in SoC designs, especially for timing convergence. Recently, Statistical Static Timing Analysis (SSTA) has been proposed as a promising solution to consider the process parameter variation but it has not been widely used yet. For estimating the delay yield, designers have to know and understand the accuracy of SSTA. However, the accuracy has not been thoroughly studied from a practical point of view. This paper proposes two metrics to measure the pessimism/optimism of SSTA; the first corresponds to yield estimation error, and the second examines delay estimation error. We apply the metrics for a problem which has been widely discussed in SSTA community, that is, normal-distribution approximation of max operation. We also apply the proposed metrics for benchmark circuits and discuss about a potential problem originating from normal-distribution approximation. Our metrics indicate that the appropriateness of the approximation depends on not only given input distributions but also the target yield of the product, which is an important message for SSTA users.

key words: *statistical static timing analysis, statistical max operation, DFM, SoC*

1. Background

With the recent advance of process technology scaling, the manufacturing variation of gates and wires in SoC has been increasing continuously. Traditional corner based timing analysis usually assumes overly pessimistic situations, which causes a timing convergence problem and/or a design with excessive margin.

To overcome these problems, Statistical Static Timing Analysis (SSTA) is proposed which takes the variations into account in a statistical manner [1]–[5].

SSTA, which is different from traditional deterministic methods in STA, propagates the probabilistic distribution of signal arrival time along the gates and wires. But it has not been widely used in practical designs, since variation modeling, accuracy, yield prediction error, and so on, have not been well studied. When SSTA is used for estimating the delay yield, designers have to be aware of the estimation error involved in the SSTA implementation and algorithm. Generic metrics to measure the prediction error are eagerly awaited in order to discuss the performance among several SSTA methods.

This paper proposes two general metrics that can evaluate the accuracy of SSTA. When discussing SSTA accuracy, there are two situations. In the first situation, we want to know the yield estimation error for the given speed specification. In the second, given a target yield, the error of the required delay is also important. We therefore devise two metrics; one is for delay yield estimation and the other is for delay time estimation. As an application example, we then use these metrics to discuss a well-known problem in SSTA implementation, i.e., how much error the normal-distribution approximation of max operation may involves.

2. Definition of Metrics for SSTA Accuracy Evaluation

In this section, we propose the error evaluation metrics to measure the accuracy of the delay distribution computed by SSTA.

We perform timing verification with SSTA in order to learn whether the current design satisfies the expected yield under the given timing specification. When setting target delay yield p under the given operating frequency, the probability that the maximum path delay in the circuit is smaller than the delay specification must be no less than p.

To discuss the accuracy of SSTA, we propose two metrics: metric F is the delay estimation error at the target yield point, and metric Y is the yield estimation error due to SSTA algorithm and implementation. Figure 1(a) shows the actual delay distribution and Fig. 1(b) shows the distribution estimated by SSTA. Here we define the target yield $p(\%)$ and the corresponding delay time in the estimated distribution as x_1. In the actual distribution, delay time x_2 which corresponds to yield $p(\%)$ is different from x_1. At this time, the approximation error in a delay probabilistic distribution F

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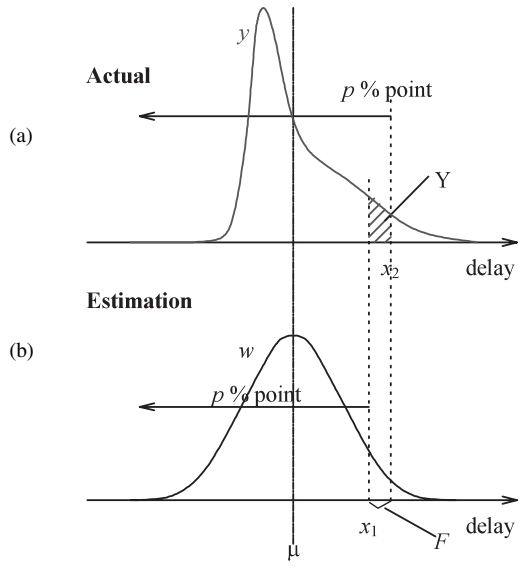

Fig. 1 Definition of F and Y (PDF).

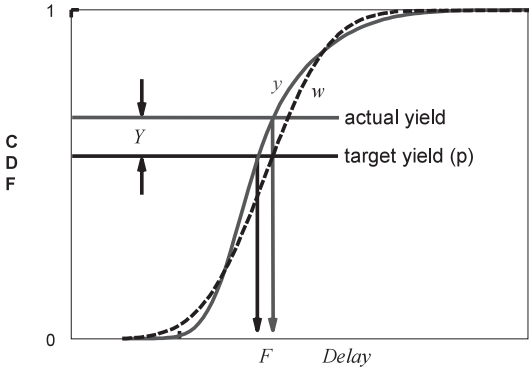

Fig. 2 Definition of F and Y (CDF).

can be calculated as follows.

$$F = (x_2 - x_1) / x_2 \tag{1}$$

Yield estimation error Y corresponds to cumulative probability in a range $[x_1, x_2]$ of the actual distributions which can be calculated as follow.

$$Y = \phi(x_2) - \phi(x_1) \tag{2}$$

In Eq. (2), $\phi(x)$ is a cumulative density function, and is defined as follows:

$$\phi(x) = \int_{-\infty}^{z} g(z)dz \tag{3}$$

Figure 2 is an expression of the same index with CDF.

3. Experimental Discussion on the Appropriateness of Normal-Distribution Approximation of Statistical Max Operation

In this section, we study a well-know error source involved in many SSTA implementations, normal-distribution approximation of statistical max operation as an example, and its appropriateness is discussed with the proposed metrics. The reasons why normal-distribution approximation is widely used are summarized as follows:

1. Easier handling of the correlation between the distributions by using a correlation coefficient.
2. Lower computational cost and memory requirement compared to piece wise linear approximation of the Probabilistic Density Function.
3. Lower computational cost of handling re-convergence path with combining the variation factor orthogonalization by principal component analysis and a canonical gate delay modeling from Taylor expansion.

We show experimental results for F and Y metrics for basic 2 input gate, 3 input gate, and example circuits in order to understand what condition causes the serious yield estimation error by the Gaussian distributed approximation.

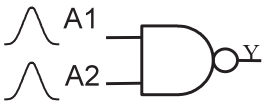

Fig. 3 Two input gate model.

Table 1 Experiment condition for 2 input gate model.

	Mean (μ)	Standard deviation (σ)
A1	-3, -1, 0, 1, 3	0.5, 1, 2, 4
A2	0	1

3.1 Case Study for 2 Input Gate Model

As shown in Fig. 3, the 2 input gate model was evaluated in order to understand the basic principles. We applied different Gaussian distributions to the input pins A1, A2 with setting the correlation coefficient to 0.0, 0.5 and 0.9, and computed F, Y metrics from the comparison between the Monte Carlo simulation results of output pin Y and approximated Gaussian distribution having the same mean and standard deviation values with the simulation.

All the combinations of mean and standard deviation values in Table 1 are applied for input pins A1, A2. Input pins A1, A2 are equivalent in this evaluation, so we fixed the parameters of input pin A2.

Figure 4 is the evaluation result of the metric Y in μ_1=0 and σ_1=1 case. The metric F and Y are calculated as follows. First, the delay value x_1 at the normal distribution is obtained for the target yield p. Next, the delay value x_2 is obtained for the actual yield p from the real distribution by Monte Carlo simulation. Once x_1 and x_2 are obtained, F and Y are calculated by the Eqs. (1) and (2). This result shows a good agreement between the true distribution and approximated Gaussian distribution.

Figure 5 is the evaluation result of the metric Y when

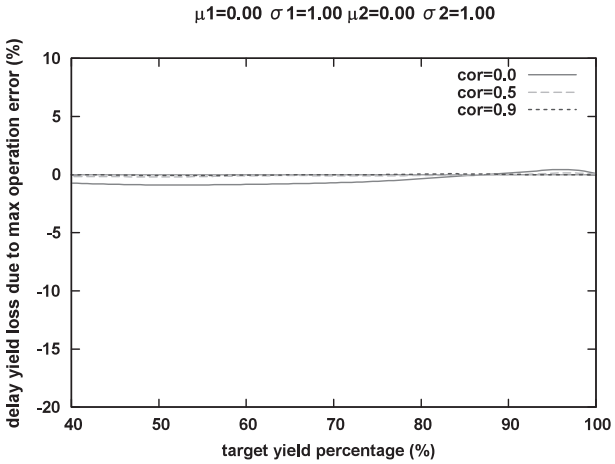

Fig. 4 The result of metric Y for 2 input gate model. ($\mu_1 = 0$, $\sigma_1 = 1$)

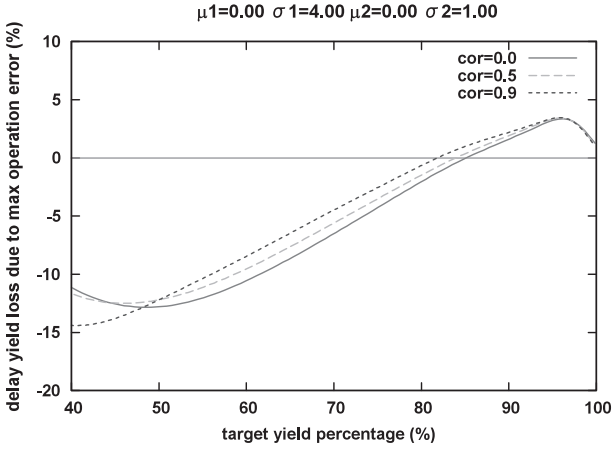

Fig. 5 The result of metric Y for 2 input gate model. ($\mu_1 = 0$, $\sigma_1 = 4$)

the standard deviations of input pins A1, A2 differ by a factor of 4. This result shows that the approximated Gaussian distribution has an error of more than 10% in the target yield range (40–100%).

When the metric Y has a positive value, it means that the true yield is less than the approximated target yield. On the other hand, when the metric Y has a negative value, it means that there is an overestimation of the target yield which may lead to increased design time for convergence. So, careful attention must be paid to the computation accuracy in using the proposed metrics.

Figure 6 shows the contour lines of the distribution of the Y metric in a negative value case (in other words, Gaussian approximation overestimates the delay) under the various combinations of μ and σ. This contour plot shows that there is a region where the metric Y becomes significantly worse.

3.2 Case Study for 3 Input Gate Model

In this section, the 3 input gate model depicted in Fig. 7 is evaluated as a representative of multiple input gates. As in

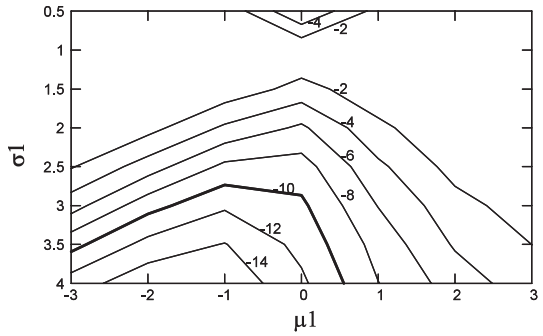

Fig. 6 The contour plot of metric Y for 2 input gate model. (cor=0.0) (Measured by maximum error with target yield range 50–100%)

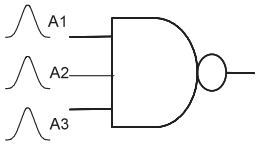

Fig. 7 Three input gate model.

Table 2 Experiment condition for 3 input gate model. (Small Y metric case for A2, A3 pins from Fig. 6)

	Mean (μ)	Standard deviation (σ)
A1	-3, -1, 0, 1, 3	0.5, 1, 2, 4
A2	0	1
A3	0	2

Table 3 Experiment condition for 3 input gate model. (Large Y metric case for A2, A3 pins from Fig. 6)

	Mean (μ)	Standard deviation (σ)
A1	-3, -1, 0, 1, 3	0.5,1,2,4
A2	0	1
A3	-2	4

the 2 input gate model case, we fixed the delay distribution for input pin A2 and chose 2 cases for that of input pin A3 as shown in Table 2 and Table 3. These 2 conditions correspond to the small Y metric case (less than 5%) and the large Y metric case (more than 10%) in Fig. 6. We selected these 2 cases to see the difference of the presence of additional input pin A1. Note that correlation coefficient between the input pins are set to 0.

Figures 8 and 9 show the results of the simulations using the combination in Table 2 corresponding to small Y metric cases of A2, A3 input pins. The Ref (dotted) line in figures shows the case when the mean value of input pin A1 was chosen to be small enough to avoid the effect in the MAX operation. Thus the difference of dotted lines and

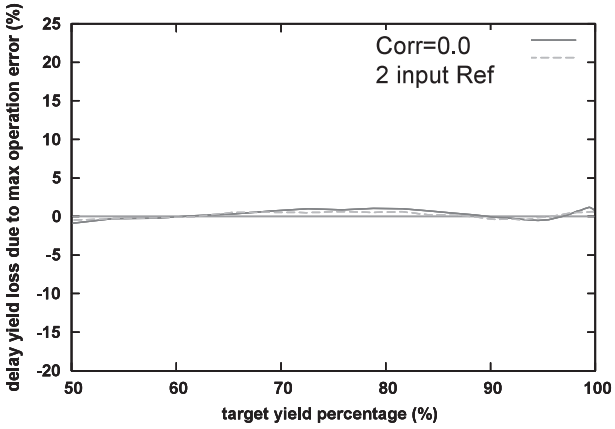

Fig. 8 The result of metric Y for 3 input gate model. ($\mu_1 = 0, \sigma_1 = 1, \mu_2 = 0, \sigma_2 = 1, \mu_3 = 0, \sigma_3 = 1$)

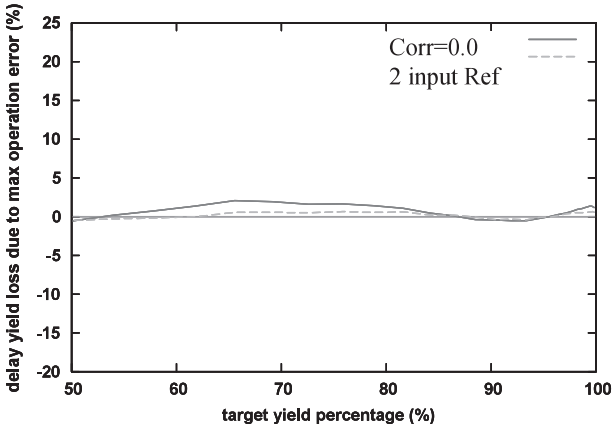

Fig. 9 The result of metric Y for 3 input gate model. ($\mu_1 = 0, \sigma_1 = 4, \mu_2 = 0, \sigma_2 = 1, \mu_3 = 0, \sigma_3 = 1$)

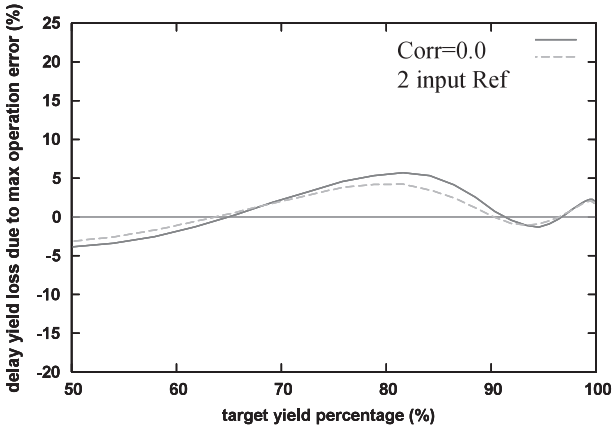

Fig. 10 The result of metric Y for 3 input gate model. ($\mu_1 = 0, \sigma_1 = 1, \mu_2 = 0, \sigma_2 = 1, \mu_3 = -2, \sigma_3 = 4$)

solid lines shows the difference due to the presence of the A1 pin.

From Figs. 8 and 9, the value of Y metric increases compared with the 2 input gate case, but the difference is 3% at maximum which is small enough and acceptable.

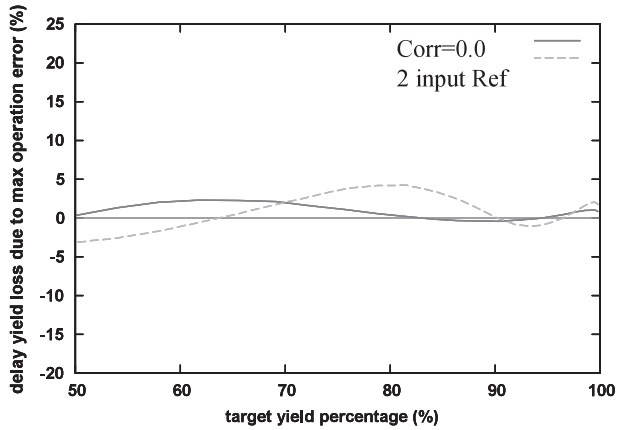

Fig. 11 The result of metric Y for 3 input gate model. ($\mu_1 = 0, \sigma_1 = 4, \mu_2 = 0, \sigma_2 = 1, \mu_3 = -2, \sigma_3 = 4$)

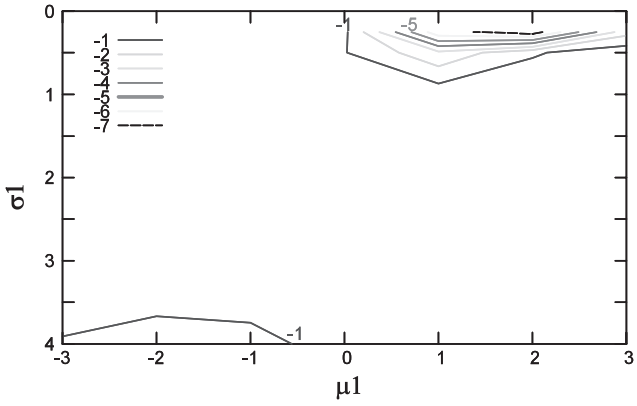

Fig. 12 The contour plot of metric Y for 3 input gate model. ($\mu_2 = 0, \sigma_2 = 1, \mu_3 = 0, \sigma_3 = 1$)

Figures 10 and 11 show the results of the combination in Table 3 corresponding to large Y metric cases of the A2, A3 input pins. The difference of dotted lines and solid lines shows the difference due to the presence of A1 pin as in Figs. 8 and 9. In these two cases, the standard deviation of input pin A1 is in the range of the maximum standard deviation of A2 and A3 input pins.

From these results, which are the as same as in the 2 input gate model case, the difference of the Y metrics are within a range of a few percent when the standard deviation of input pin A1 is same or less than that of other 2 input pins.

We found that if the mean value of A1 pin is much larger than that of A2 and A3 pins, the output distribution is determined by A1 pin only. Also, if the mean value of A1 pin is much smaller than that of A2 and A3 pins, the presence of the A1 pin is negligible in max operation and does not contribute to the Y metric value. In other words, close mean values and sufficient different standard deviation of input pins lead to large Y metric difference in the 3 input gate model case compared with 2 input gate model case.

To confirm the above observation, we tried to figure out the overall tendency of metric Y by applying finer step of A1

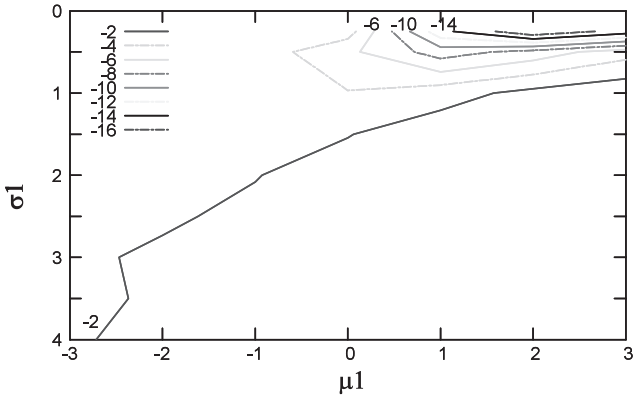

Fig. 13 The contour plot of metric Y for 3 input gate model. ($\mu_2 = 0$, $\sigma_2 = 1$, $\mu_3 = -2$, $\sigma_3 = 4$)

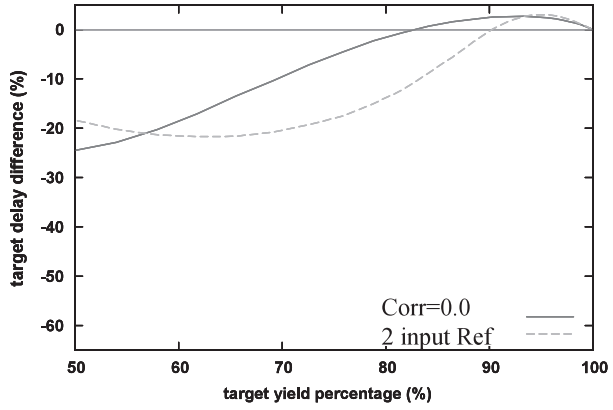

Fig. 14 The result of metric F for 3 input gate model. ($\mu_1 = 0$, $\sigma_1 = 4$, $\mu_2 = 0$, $\sigma_2 = 1$, $\mu_3 = -2$, $\sigma_3 = 4$)

pin parameters. Figure 12 shows the case in which the delay distribution of A2 pin is fixed to μ_2=0 and σ_2=1 and that of A3 pin is fixed to μ_3=0 and σ_3=2. Figure 13 shows the case in which the delay distribution of the A2 pin is fixed at μ_2=0 and σ_2=1 and that of A3 pin is fixed to $\mu_3 = -2$ and σ_3=4. Both cases are measuring by max error with target yield range 50–100% same as Fig. 6.

In these two cases, adding an input with extremely narrow standard deviation deteriorates the metric Y value due to the increase of the difference in the standard deviation between the input pins. However, introducing an extra input pin tends to relax the Y metric value in many cases.

Metric Y does not become large when in targeting high yield such as 3σ, because it is an integrated value. But, it is worth mentioning that these experiments assumed that the mean value of the approximated Gaussian distribution and the real distribution are exactly the same. If it is not possible to derive the correct mean value, the value of metric Y will increases significantly over entire range of target yield.

On the other hand, metric F shows a different tendency because metric F is not an integrated value. Figure 14 shows metric F under the same conditions as in Fig. 11. Thus we can use F and Y metrics for the different aspects of error.

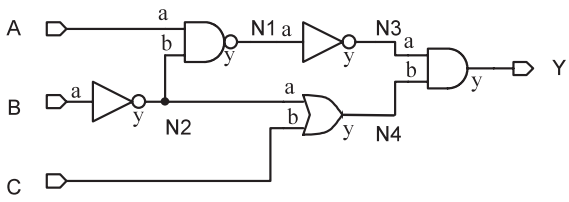

Fig. 15 Experiment circuit ex4 schematic.

3.3 Case Study for an Example Circuit

In this section, we evaluate the Y metrics for the multiple stage paths of cells according to the result of Sects. 3.1 and 3.2. Previous sections have shown that F and Y tend to increase if two distributions' means are close but have different standard deviations.

We make the test data such that the difference between the real distribution and its approximated Gaussian distribution is significant at multiple stages of logic cells and evaluate the effect of error on the approximated Gaussian distribution.

The following case will cause above situations.

1) The σ of multiple arcs on a cell is different from each other.

The library includes logic cells which have significantly different delay variation at each pin. Figure 3 A1→Y: N (10, 2), A2→Y: N (10, 0.5) are the examples, but the arrival time needs to be close, otherwise one of the input pins dominates the output distribution and does not incur the error on the approximation of that.

2) The library has two types of cells each having either a large or small standard deviation such as CELL1 N (10, 2), CELL2: N (10, 0.5).

When cells having a very different standard deviation connect to 2 input cells at each input pin, and the have a nearly equal arrival time, the F, Y could be considerably larger.

3) More than 2 paths become critical path.

This case means 2 paths are both critical but the deviations of those are significantly different. For example, one critical path delay is dominated by the interconnect delay whose deviation is small and the other critical path is dominated by the gates whose deviation is large.

Figure 15 shows the experimental circuit ex4 which meets the above conditions.

Table 4 shows the library example. The average of cell delay has been determined to generate multiple critical paths.

The conditions of the experiment are as follows,

a) Typical value: Ordinary STA (use only mean of Table 4)
b) Gaussian distribution: σ/μ=0.1 (As the Table 4)

Table 4 Experiment condition for the circuit ex4.

CELL	in out	Delay type (μ, σ)
inv	a→y	gauss (10.2, 1.02)
nand	a→y	gauss (25.0, 2.5)
	b→y	gauss (15.0, 1.5)
and	a→y	gauss (20.0, 2.0)
	b→y	gauss (20.0, 2.0)
or	a→y	gauss (25.0, 2.5)
	b→y	gauss (35.0, 3.5)

Table 5 Experiment result for the circuit ex4.

Condition	Mean	Standard deviation	Skewness	Kurtosis
a	55.400	N/A	N/A	N/A
b	58.407	2.700	0.192	0.169
c	59.506	3.939	1.000	1.901
d	60.773	5.681	1.459	2.795
e	57.976	2.473	0.244	0.130
f	60.862	4.421	-0.238	-0.268

c) Gaussian distribution: the σ of OR gate at Table 4 is 2 times bigger.
d) Gaussian distribution: the σ of OR at Table 4 is 3 times bigger.
e) Gaussian distribution: the σ of OR at Table 4 is half.
f) Uniform distribution: all cells delays are uniform between in the $\mu \pm 3\sigma$.

Table 5 shows the statistical results at the end node Y. We also evaluate the skewness and the kurtosis which are ordinarily used in statistical analysis. The skewness is the degree of asymmetry of a distribution and the kurtosis is the degree of peakedness of that. Both values are 0 in Gaussian but deviates from zero as the distribution differs from Gaussian. In Table 5, those values are b < c < d which means d, c, and b become increasingly different from the Gaussian distribution in this order. As Fig. 16 shows, Y especially becomes bigger in b and c, but d does not show the significant error even the skewness and kurtosis have worst values. This shows that even the skewness and kurtosis would show some tendency but not necessarily exhibit the estimation error itself.

When there is significantly difference in the standard deviation of the delays in the library or circuit structure, the error of max operation might not be negligible.

3.4 Case Studies Summary

Previous case studies can be summarized as the following rule of thumb for a Gaussian approximation error.

The 2 input case study shows:

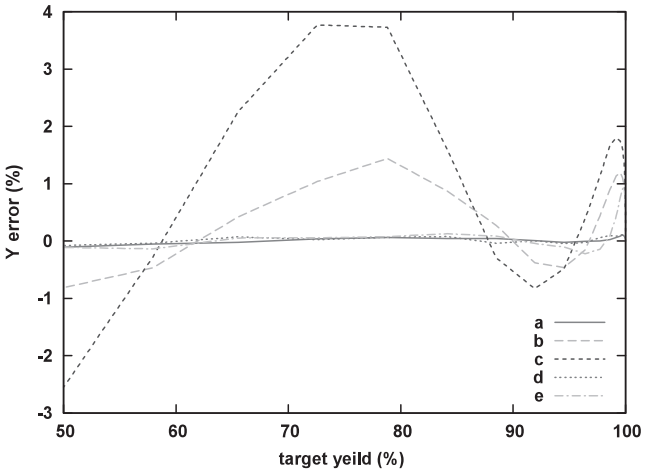

Fig. 16 The result of metric Y for ex4 circuit.

1) The metrics F indicates delay error and the metrics Y indicates the yield error. Each shows a different aspect of approximation error.
2) The metrics F and Y become both optimistic and pessimistic depending on the target yield.
3) The error ratio becomes larger at the lower target yield, thus special attention must be paid when using SSTA at the lower target yield such as in early process development phase.
4) The metrics F and Y do not strongly depend on the correlation of the input signals.
5) The contour plot of Y indicates that Y is more sensitive to the difference of standard deviations than that of means..

The 3 input case study shows:

6) The F and Y metrics are relaxed by adding an input pin in many cases.
7) If the variation of the additional input is much smaller than the existing inputs, the metrics F and Y become considerably worse.
8) If the variation of the additional input is comparable to the existing inputs, the metrics F and Y do not change significantly.
9) Figure 13 suggests that exceptional cases exist that even through the μ, σ of an additional input pin is within the range of the existing pins ($\mu_1 < \mu < \mu_2$, $\sigma_1 < \sigma < \sigma_2$), the metric could be slightly worse.

4. Conclusion

We proposed the quantitative metrics F and Y to evaluate the error of SSTA due to the internal modeling and algorithms. From the experimental result of the 2 input gate model, we showed that Gaussian approximation of max operation includes more than 10% error in the target yield range (40–100%) when the standard deviation values are the different by a factor of 4. From the experimental result of the 3 input gate model, we showed that the error from Gaussian distributed approximation are dominated by the 2 in-

put pins which have close mean values and the largest difference standard deviation values. These metrics can be used as evaluation metrics for EDA tool accuracy or Non-Gaussian distribution model which has been recently proposed. This study shows that when applying the SSTA tools for real designs, simple Gaussian approximation is not accurate enough for some design situation. But the EDA tools do not necessarily reveal the detail internal algorithms, or even it may support non-Gaussian method, it is not easy to confirm the accuracy for statistical result at the real complicated data. In this point of view, the proposed F and Y metrics and the simple test data can easily confirm the figure of merit.

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