Soft-Error in SRAM at Ultra-Low Voltage and Impact of Secondary Proton in Terrestrial Environment

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***Abstract*—This paper presents soft-error measurement results through neutron and alpha irradiation tests and simulation in SRAM at ultra-low voltages, down to 0.19 V. Soft-error-rate at 0.19 V is higher than at 1.0 V by two orders of magnitude. This measurement result supported by simulation clarifies that direct ionization from secondary protons generated by nuclear reaction with neutron collision contribute to a dramatic increase in SRAM soft-error-rate at ultra-low voltages in terrestrial environment.**

***Index Terms*—Alpha, low voltage, multiple-bit-upset, neutron, single event, soft-error, SRAM.**

I. Introduction

LOW power operation is strongly demanded in recent and future highly-integrated electronic devices. An aggressive voltage scaling down to the threshold voltage of MOSFETs can dramatically reduce power consumption of electronic devices [1]. Recently, memory operation at ultra-low voltage down to 0.2 V has been achieved with 9 T-SRAM [2]. SRAM operation at such an ultra-low voltage attains low power consumption at the sacrifice of speed performance. Another approach called sleep technology, which scales down supply voltage during data holding as much as memory retention is possible [3], has already been used in SRAM for reducing power consumption. The sleep technology saves power consumption during non-active operations without involving performance penalty for active operations.

Neutrons indirectly induce soft-error through reaction with atomic nucleus of transistor materials as shown in Fig. 1. The nuclear reaction generates charged secondary particles like protons, alpha particles and heavy ions. The charged particle generates electron-hole pairs by direct ionization on the particle track and deposits charge. The generated charge is collected to drain by drift and diffusion, and causes a soft-error.

In recent 65 nm to 25 nm technologies, it is reported that direct ionization due to secondary alpha particles is a major contributor to neutron soft-error-rate (SER) in terrestrial environment [4]. On the other hand, in low voltage SRAM, direct ionization from secondary protons can be a major contributor [4]–[6], because the low voltage operation reduces critical-charge (Qc), where Qc means minimum requisite charge for causing a soft-error. Ref. [6] demonstrated that low energy protons contribute to SER by direct ionization and the cross-section of low energy protons ($<$ 2 MeV) is three orders of magnitude larger than that of high energy protons ($>$ 10 MeV). The proton impact on SER is also investigated in [7]–[9]. In space environment, [7] reported that direct ionization from protons is a major contributor to the total SER in the ISS orbit and geosynchronous (worst day) orbit. Returning to terrestrial environment, [5] demonstrated that the number of generated secondary protons is one or two orders of magnitude larger than the number of alpha particles. The direct ionization from proton could dramatically increase neutron SER of ultra-low voltage SRAM.

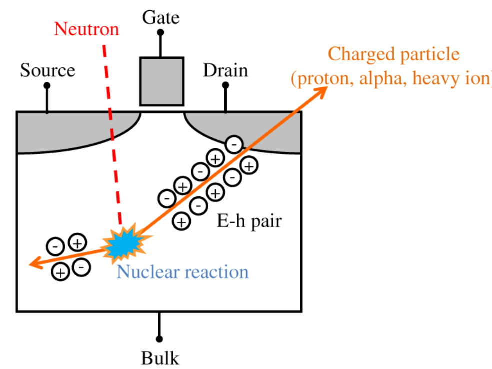

Fig. 1. Soft error mechanism by neutron.

SER in 65 nm 10-T sub-threshold SRAM was experimentally studied through neutron irradiation test [10] and alpha irradiation test [11]. The neutron SER at 0.3 V was 7.8 times higher than that at 1.0 V. The alpha SER at 0.3 V was eight times higher than that at 1.0 V, and the increase ratios of neutron and alpha SERs were almost the same. On the other hand, the SRAM cell in these works is composed of larger transistors for mitigating Vth variation and achieving ultra-low voltage operation, and the NMOS and PMOS gate areas of cross-coupled inverter are 7.8 and 6.9 times larger than the area of a minimum-sized transistor. Due to this, the critical charge was not small enough that the secondary proton direct ionization caused upsets [12]. Thus, a drastic increase in neutron SER due to secondary proton direct ionization was not clearly observed [10]. If proton direct ionization starts to contribute to soft-error, the increase in neutron SER should be much larger than that in alpha SER [5].

In this work, we evaluate SER on SRAM at ultra-low voltage down to 0.19 V through neutron and alpha irradiation tests

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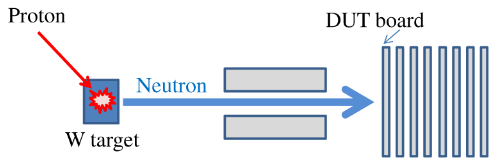

Fig. 2. Neutron test configuration at RCNP.

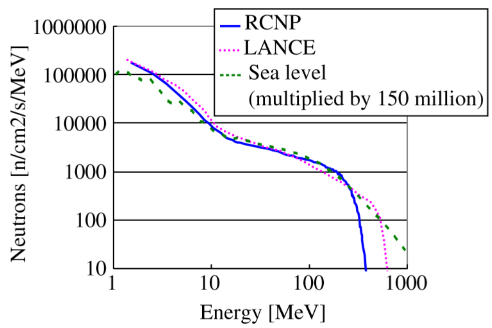

Fig. 3. Neutron energy spectrum at sea level (multiplied by 150 million) and those of spallation neutron beams at RCNP and LANCE [14].

on SRAM manufactured with 90 nm technology. We evaluate the impact of direct ionization from the secondary protons in terrestrial environment based on radiation experiments and Monte-Carlo simulations using Particle-and-Heavy-Ion- Transport-code-System (PHITS) [13].

The rest of this paper is organized as follows. Accelerated test procedure at ultra-low voltage is explained in Section II, and Section III shows test results. Section IV presents SER calculation by simulation. Section V concludes this paper with a brief summary.

II. Irradiation Test Procedure

We have performed alpha and neutron irradiation test on SRAM devices. This section explains the experimental setups.

Alpha irradiation test was carried out with an $^{241}\mathrm{Am}$ alpha source under low pressure atmosphere in a chamber. The distance between the alpha-source and the die is less than one millimeter.

Neutron irradiation test was conducted with spallation (wide spectrum) neutron beam in Research Center for Nuclear Physics (RCNP) at Osaka University. The beam and DUT configurations are illustrated in Fig. 2. This beam spectrum is similar as that of Los Alamos Neutron Science Center (LANCE) [14] and sea level spectrum which is indicated in JESD89A [15] as shown in Fig. 3.

In this paper, four test chips mounted on the first DUT board are analyzed to exclude neutron scattering and attenuation effects. The test chip includes SRAM arrays consisting of about 4 Mbit SRAM on each chip with double-well process. This SRAM consists of conventional six-transistor SRAM cells with the conventional layout as shown in Fig. 4. This SRAM was customized for ultra-low voltage operation. The Vth, width and length of transistors were optimized for enabling ultra-low voltage operation in 90 nm technology. The minimum transistor width was selected, whereas the length was enlarged to mitigate random Vth variation by increasing the gate area

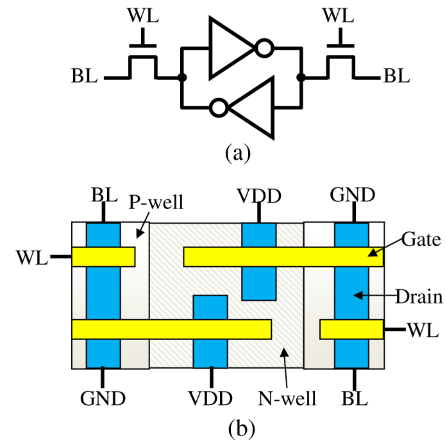

Fig. 4. (a) Shematic and (b) layout of SRAM for the irradiation tests.

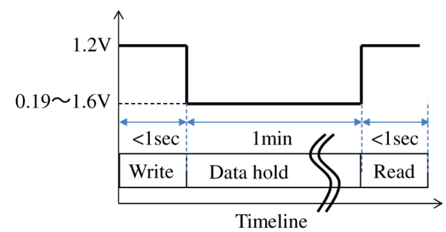

Fig. 5. Timeline of the irradiation test.

[16]. Consequently, the SRAM cell size is 1.4X larger than the normal cell size in the 90 nm technology generation. Power supply to the memory cell areas is separated from other areas.

We performed a quasi-static test for this irradiation experiment. A timing diagram of the SRAM operation and supply voltage is shown in Fig. 5. The DUTs were irradiated during data read and write as well as data hold. On the other hand, the duration of data hold was 1 minute while the data read and write were completed within 1 second. Therefore, the number of upsets during the data read and write is thought to be negligibly small compared to that during the data hold. The operation voltage for data read/write was 1.2 V. As for data hold, various supply voltages from 0.19 V to 1.6 V were given to the memory cell.

In this paper, we supposed that any two upset bits whose distance was three-cell or less were caused by an event. This classification was applied to all the combinations of two upset bits. The upset bits which were caused by the same event were recognized as an MCU event. This distance criterion was applied omnidirectionally.

III. Experimental Results

We first investigate neutron induced SER. Fig. 6 shows measured neutron induced SER. The SER is the minimum at 1.2 V, and it increases as the supply voltage increases and decreases from 1.2 V. The existence of the extremum, which corresponds to the local minimum at 1.2 V, is explained by two different phenomena on soft-error as illustrated in Fig. 7. Qc increase according to voltage increase decreases SER. The contribution of parasitic-bipolar-action (PBA), on the other hand, increases and consequently SER increases with voltage increasing. As a

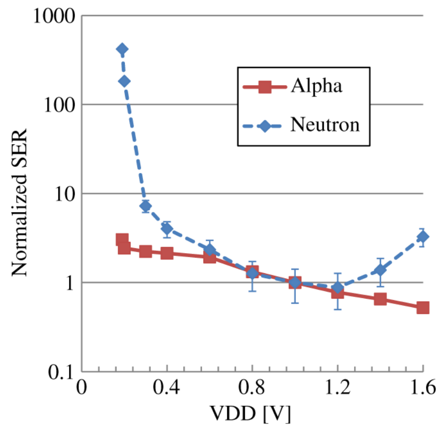

Fig. 6. Alpha and neutron SERs normilized by alpha and neutron SERs at 1.0 V, respectively.

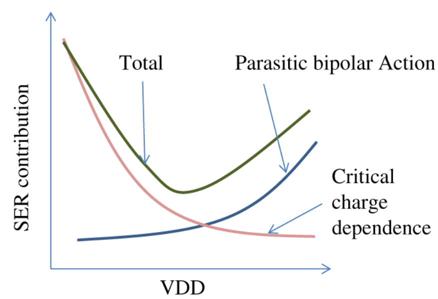

Fig. 7. A conceptual illustration of SER contribution.

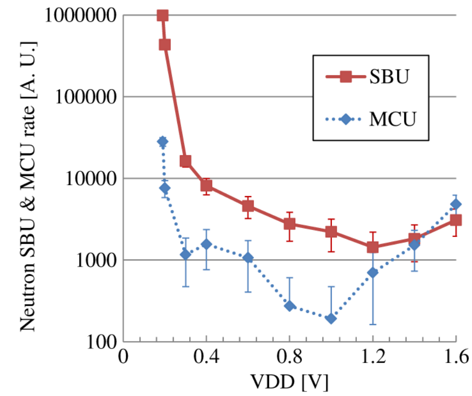

Fig. 8. Neutron induced SBU and MCU rates.

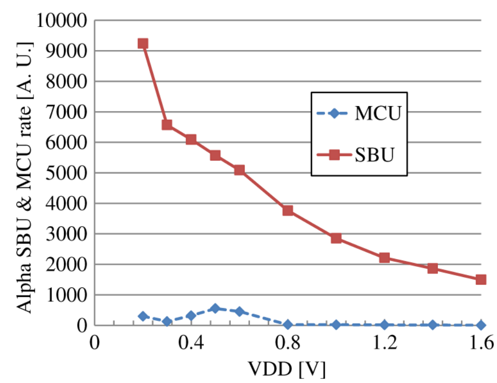

Fig. 9. Alpha induced SBU and MCU rates.

result, SER curve as a function of supply voltage has an extremum as shown in Fig. 6. The decreasing trend of SER with voltage increase is consistent with other papers [4]–[18]. On the other hand, the SER at voltages higher than the nominal voltage (1.2 V in this process) are not often reported in literature, while it is measured in this paper. By investigating the voltage dependency including such high voltages, we observed an increase in SER due to PBA. A flat voltage dependency of SER at high voltages is reported in [17], and it can be regarded as a cause that the voltage dependencies of PBA and critical charge are canceled out at these voltages.

Meanwhile, alpha induced SER, which is also plotted in Fig. 6, does not have such an extremum and it monotonically decreases roughly at an exponential rate with voltage increase. Even above 1.2 V, the alpha induced SER decreases in contrast with neutron induced SER, which suggests PBA is less influential in alpha induced SER. Ref. [11] observed that body voltage and well-tie interval, which affects neutron-induced SER [10], are not related to alpha induced SER and concluded that PBA hardly contributes to alpha induced SER. Our observation in this paper is consistent with [11].

Next, we focus on the difference in SER increase at low voltage. Neutron SER at 0.3 V is about seven times higher than that at 1.0 V, while the increase ratio from 1.0 V to 0.3 V reported in [10] was 7.8X. The SER increase measured in this work is consistent with [10]. On the other hand, at ultra-low voltages of 0.19 V and 0.20 V, neutron SER dramatically increases and its increase at 0.19 V from 1.0 V reaches 440X. SER at such low voltage has not been reported, and this is the first work that reports such a drastic increase in neutron SER.

In contrast, alpha SER at these ultra-low voltages increases by only 4X from SER at 1.0 V. This result naturally leads us to conclude that this dramatic increase at ultra-low voltage is caused by proton direct ionization from secondary protons, since [5] predicted that a drastic increase would be observed once proton direct ionization starts to contribute to SER. The contribution of the proton direct ionization will be further discussed with simulations in the next section.

Lastly, the contribution of PBA is discussed with MCU rate. Fig. 8 shows that neutron induced single-bit-upset (SBU) rate increases at above 1.2 V, and neutron induced MCU rate increases at above 1.0 V. While PBA contributes to both SBU and MCU, the impact on MCU has been more intensively discussed in literature [18][19] since some of MCUs could not be corrected by ECC and interleaving. Besides, at 1.6 V, the MCU rate is higher than the SBU rate, which means that more than half soft errors are MCU at 1.6 V. This result shows that MCU is more sensitive to PBA, while contribution ratios of PBA to SBU and MCU rates are different. On the other hand, alpha induced SBU and MCU rates decrease as voltage increases as shown in Fig. 9. This result again indicates that the contribution of PBA is not significant in alpha induced soft-error, because PBA activation is accompanied with an increase in MCU rate. It can be considered as a cause that high LET particles like heavy ions generated by neutron collision can trigger PBA although low

LET particle like alpha cannot trigger PBA in this SRAM. Another possible reason for the trend difference between alpha and neutron induced SBU and MCU could be the angular distribution of ionizing species between alpha irradiation and neutron secondary particles. Further investigations on the impact of the angular distribution with detailed simulations are included in our future work.

IV. Simulation

To further understand the soft-error mechanism at ultra-low voltage, we calculated contributions of secondary particles to soft-error. Here, the soft-errors are categorized and accumulated depending on the secondary particles (protons, deuterons, tritons, alpha and other heavy ions). In this simulation, Qc at each memory cell voltage (0.19 V to 1.6 V) was evaluated by circuit simulation with the conventional double exponential model [20], and a simple linear regression was carried out supposing $\mathrm{Qc} = 0$ at 0 V. The derived linear function was used for computing Qc at each supply voltage including the ranges below 0.19 V and beyond 1.6 V. SER for each Qc was calculated by Monte-Carlo simulation using PHITS [13] ver. 2.52[1] with the sensitive volume method [4]. Note that when Qc is 0, every penetration into the sensitive volume is assumed to cause an upset regardless of the deposited charge. The simulation assumed a neutron source whose energy spectrum was the same with the spallation neutron beam at RCNP shown in Fig. 3, and injected 1 million neutrons within $0.012\ \mathrm{cm}^2$ whose energy was 1 MeV to 400 MeV. Neutrons below 1 MeV were not considered.

The simulated structure, which is illustrated in Fig. 10, reproduces the SRAM structure used in the irradiation tests. The structure consists of a metal layer, which corresponds to interconnect layers, and a Si block. The length, width and depth of the Si block are about 500, 1100 and 500 um. The structure includes 500×500 bit cells, and the cell array are horizontally surrounded by 50 um Si. Si substrate is attached below the cells.

In this simulation, two types of sensitive volumes, which correspond to sensitive NMOS and PMOS, are placed. The areas of sensitive volumes are the same with the drain areas of sensitive NMOS and PMOS, and the depths of NMOS and PMOS volumes are 1.24 um and 0.29 um, respectively [21]. Besides, SER in this simulation does not include the contribution of PBA. Note that at ultra-low voltage, PBA is less visible as explained with Fig. 7 and hence this simulation is appropriate to discuss SER at ultra-low voltage.

Fig. 11 shows the contribution ratio of each secondary particle, and Fig. 12 presents the calculated SER originating from each secondary particle. As the supply voltage becomes lower, the contribution of proton direct ionization increases, and it becomes larger than that of alpha particles at 0.25 V and below. At voltage below 0.25 V, the critical charge is reduced to the point that secondary protons can cause SEU. Consequently, ultra-low voltage SRAM whose supply voltage is lower than 0.25 V is expected to significantly suffer from a drastic increase in SER due to secondary protons. Meanwhile, alpha is dominant in a wide voltage range of 0.25 V to 1.9 V, and other heavy ions become dominant at 1.9 V and higher.

There is a large difference between simulation and measurement in terms of the SER increase from 1.0 V to 0.19 V. Fig. 13 plots the measured and simulated SERs extracted from Fig. 6 and Fig. 12. The SER increase from 1.0 V to 0.19 V in the simulation is 4X whereas that in the measurement is 440X. For this underestimation in the simulation, there are two possible reasons.

The first possible reason is ignoring secondary protons coming from outside of the silicon die modeled in this simulation. Protons can travel a long distance compared to other

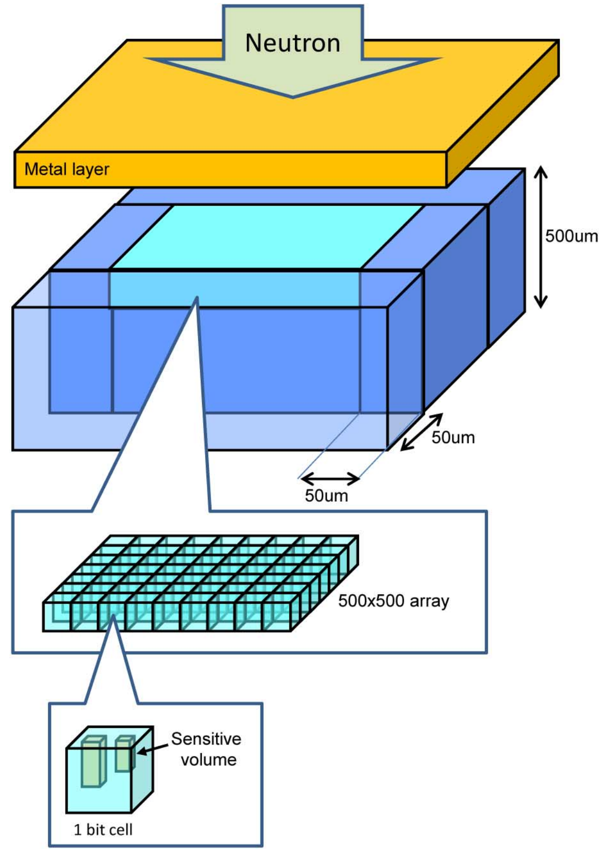

Fig. 10. Simulated structure.

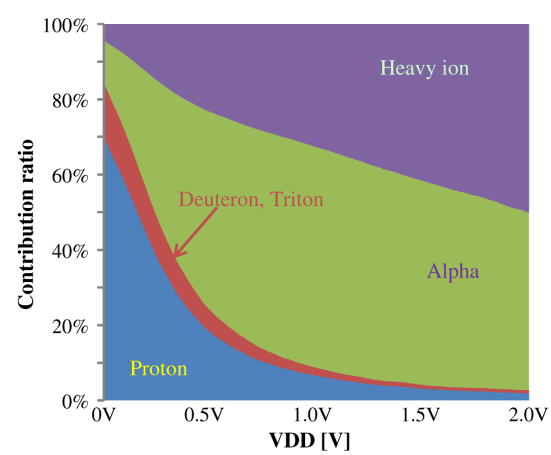

Fig. 11. Contribution ratio of each particle in SRAM.

[1]PHITS v2.52 includes ion-nucleus coulombic interactions. In addition, the simulation with PHITS referred to JENDL-4 for neutrons ($<$ 20 MeV), and then the impact of recoiled Si, which is considered in [6], is also included.

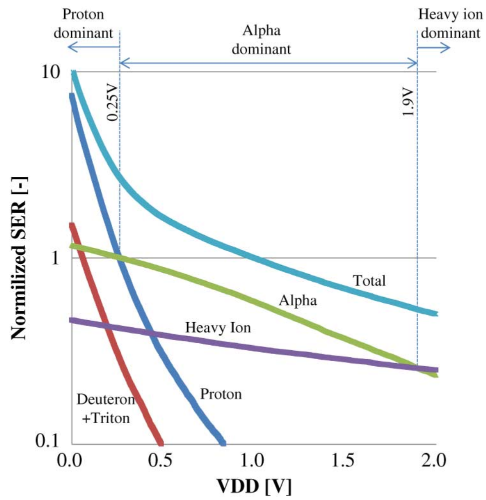

Fig. 12. Calculated SER originating from each secondary particle in SRAM. These SERs are normilized by the total SER at 1.0 V as 1.

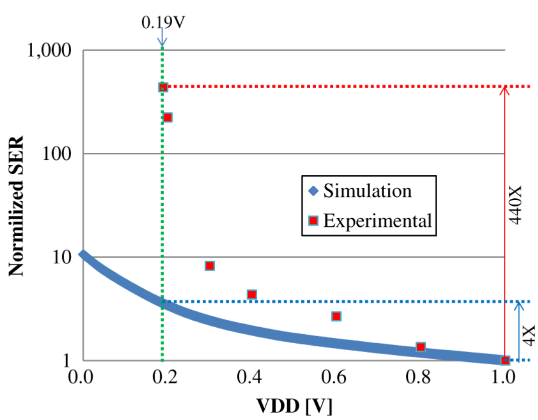

Fig. 13. SER comparison between measurement and simulation.

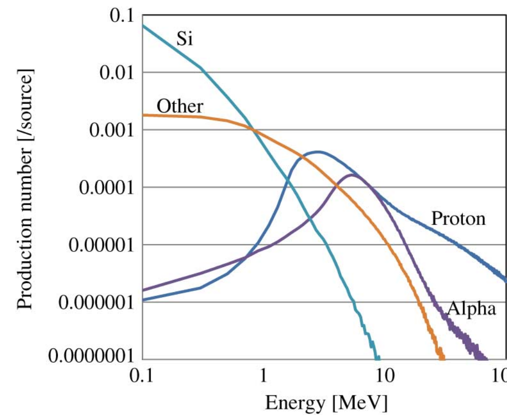

Fig. 14. Production numbers of proton, alpha, Si and other heavy ions calculated with PHITS as a function of particle energy. A neutron beam having RCNP energy spectrum (Fig. 3) is given to Si substrate.

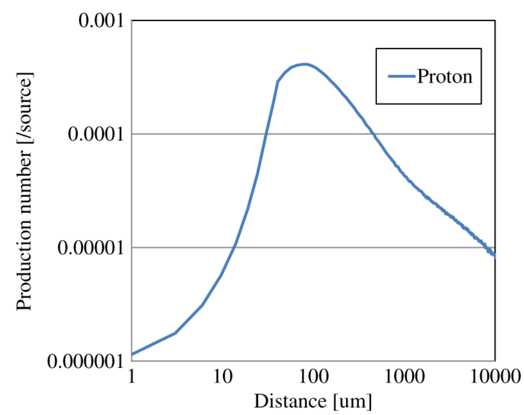

Fig. 15. Production probability as a function of proton travel distance calculated from Fig. 14 and SRIM [22].

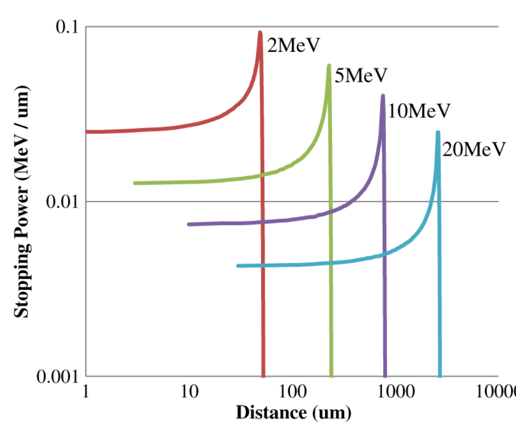

Fig. 16. Stopping power of 2.0, 5.0 and 10 MeV protons on silicon, caluculated by SRIM [22].

secondary particles. Fig. 14 shows the production numbers of proton, alpha, Si and other heavy ions as a function of particle energy, which is calculated with PHITS assuming a neutron beam having RCNP energy spectrum (Fig. 3) is given to Si substrate. Fig. 15 shows the production rate as a function of proton travel distance, where it is calculated from the data shown in Fig. 14 and the relation between proton travel distance in Si and proton energy obtained by SRIM [22]. The distribution has a long right tail, and the portion of protons that travel more than 50 um is more than 90%. On the other hand, the thickness of the metal layer is less than 20 um, and the width of Si surrounding the SRAM cells is 50um in our simulation as shown in Fig. 10. Meanwhile, the amount of charge deposited increases sharply just before the proton stopping, i.e. following Bragg-Curve, as shown in Fig. 16. Fig. 15 and 16 indicate that secondary protons generated even hundreds micrometers to a few millimeters away from the transistor of interest can contribute to SER at ultra-low voltage. Simulating the entire DUT including silicon-die, package and PCB is necessary to fully consider such proton contributions.

The second possible reason is the contribution of low-energy neutrons, which was not considered in the simulation. Our simulation assumed a neutron source that reproduced 1 MeV to 400 MeV RCNP spectrum and neutrons below 1 MeV were not included, because the information on the neutron flux below 1 MeV at RCNP was not available. Further investigations on the possible reasons are included in our future work.

V. Conclusions

We evaluated SER through neutron and alpha irradiation tests and simulations. The measurement results show that neutron induced SER at ultra-low voltage dramatically increases, and SER at around 0.2 V is by two orders of magnitude higher than that at 1.0 V. This result supported by simulation indicates that secondary protons generated by nuclear reaction with neutron collision are contributing to SER of ultra-low voltage SRAM dominantly in terrestrial environment.

In near future technologies such as 16 nm or finer, SER could dramatically increase at low voltage since Qc also decreases with technology advancing. In SRAMs manufactured with finer lithography such as 16 nm or finer, the contribution of proton direct ionization would be observed even at a voltage much higher than 0.2 V. In this case, soft-error can be a primary design concern for both high performance computing based on near-threshold computing [23] and low power consumer and biomedical products.

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