Mitigating Multi-Bit-Upset With Well-Slits in 28 nm Multi-Bit-Latch

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***Abstract*—This paper proposes a technique that mitigates multi-bit-upset (MBU) in multi-bit-latch (MBL) without performance degradation by applying well-slits. The area overhead in an MBL macro for processor design, which includes a clock buffer and a checker, is only 5.4% in a 28 nm technology. Sixty-hour accelerated neutron irradiation test observed no MBUs in the MBL with well-slits. The proposed mitigation technique achieved excellent robustness against MBU without any increase in SBU rate. The MBL with the proposed mitigation technique helps improve reliability of electronic devices.**

***Index Terms*—Latch, multiple cell upset, neutron, single event, soft-error.**

I. Introduction

RADIATION induced soft-error increases in modern electronic devices. Single-event-upset (SEU) in SRAM is often mitigated by error-correction-code (ECC) in electronic devices for reliability-demanding applications and large-scale applications. On the other hand, in logic circuits, it is generally difficult to apply ECC. Instead, triple-modular-redundancy (TMR) or double-modular-redundancy (DMR) is used for mitigating soft-error in logic circuits. These redundant techniques involve large area overhead, and it often exceeds 2X. For mitigating soft error induced failures with low area overhead, hard-instruction-retry (HIR) with checker and predictor is used for logic circuits in processors [1].

For HIR, checker bits and related circuit components (checker, predictor and comparator) are added to detect errors as illustrated in Fig. 1. The checker calculates a checker symbol from the output of a unit (e.g. data path and multiplier), and the calculated checker symbol is stored in the checker bits. The predictor predicts the check symbol from the unit input, and the comparator compares the calculated and predicted check symbols. Parity and residue checks are used for data transmission lines and multipliers, respectively. Once the comparator detects inconsistency, an error flag signal is generated and the running instruction is stopped and retried by HIR. An advantage of HIR is that an error can be detected with simple additional circuits, while other techniques often require large overhead. HIR is very effective for mitigating the impact of SEU in sequential elements to the processor operation. In addition, this technique can partially mitigate single-event-transient (SET) in combinational circuits. Thus, HIR can be applied to reliability-demanding processors with low overheads in area, performance and power consumption.

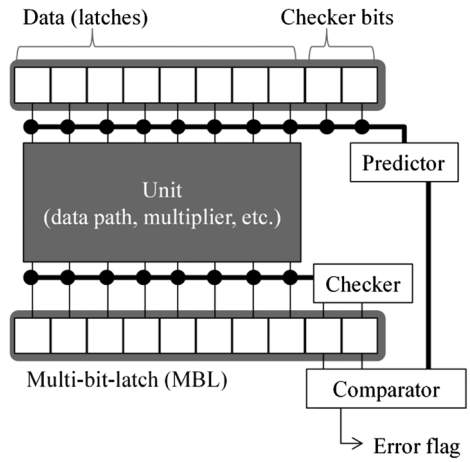

Fig. 1. Circuits necessary for HIR.

Multi-bit-latch (MBL), which consists of multiple latches, is used for storing a code word including data bits and checker bits. The circuit structure is shown in Fig. 2. The latches in an MBL share a clock buffer for saving area and power consumption and reducing clock-skew [1]. The predictor and checker in HIR can detect single-bit-upset (SBU) in the MBL. However, these may miss multi-cell-upset (MCU), which is multiple upsets caused by a single neutron strike ranging over one or more MBLs. An MCU that cannot be corrected by HIR is called multi-bit-upset (MBU) in this paper.

Table I, which comes from [2], lists four possible mechanisms of MCU. MCU increases with technology scaling because of a decrease in distance between bits [2], and hence MCU in MBL is becoming a critical concern for sustaining processor reliability. It is manifested that the main reasons of MCU were (C) and (D) in 130 nm technology [2]. Charge sharing (C) occurs due to charge drift and diffusion in a well. Parasitic bipolar action (D) is triggered by well potential elevation. Data bits which share a well are thus vulnerable to both (C) and (D). Furuta *et al.* [3] reported that in 65 nm flip-flops, 97% of MCUs occurred in the latches sharing the same Pwell, and this suggests that the main reasons of MCU in 65 nm technology are (C) and (D). The MBUs due to (C) and (D) occur in the same well, and hence splitting well areas for each latch is expected to mitigate MBUs

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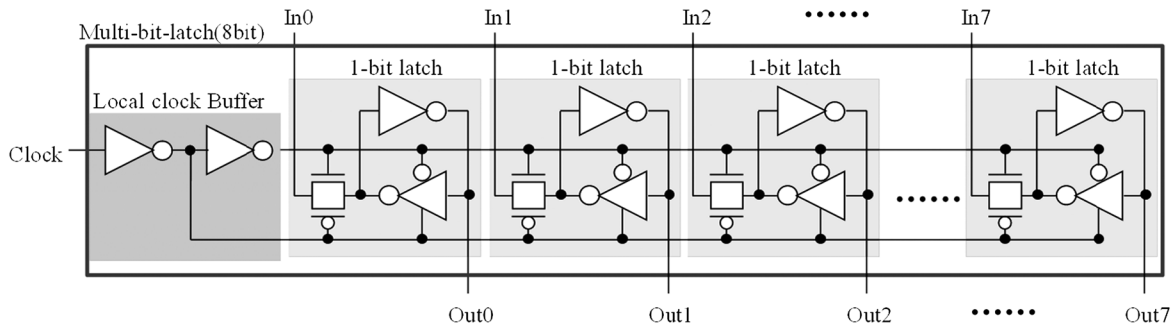


Fig. 2. Multi-bit-latch with clock buffer (8-bit).

TABLE I
POSSIBLE MECHANISUMS OF MCU [2]

Symbol	Name
(A)	Successive hits by one ion
(B)	Multi hits by multiple ions
(C)	Charge drift/diffusion (charge sharing)
(D)	Parasitic bipolar action

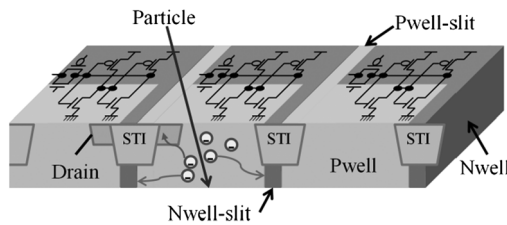


Fig. 3. Proposed MBU mitigation technique using well-slit for MBL.

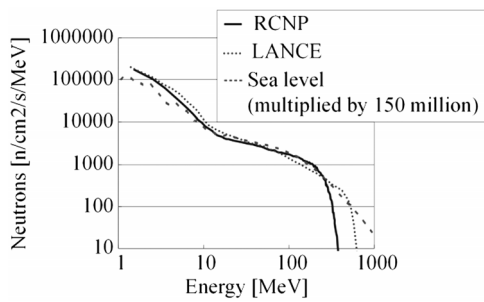


Fig. 4. Neutron spectrum at sea level (multiplied by 150 million) and spectrums on of spallation neutron beams at RCNP and LANCE [9].

that originate from (C) and (D). However, the latches of conventional MBL share a well. Therefore, the conventional MBL has higher MBU rate than SRAM without ECC because SRAM adopts interleaving [4]. Meanwhile, a latch-up prevention technique that uses well separation is proposed in [5][6], while this technique needs a special process option of deep trench (DT) and hence the applicability is limited.

In this work, we propose an MBU mitigation technique for MBL using well-slits. The inserted well-slits isolate wells of each latch for preventing charge diffusion and parasitic bipolar action. This well-slit technique can be applied to any bulk CMOS technologies without process customization, and MBU mitigation can be achieved only by design modification and consequently with low cost. We evaluate the area overhead of the proposed technique by designing an MBL macro including the predictor, checker and comparator for processors in 28 nm technology. The effectiveness of the proposed mitigation technique is validated through neutron irradiation tests on 28 nm test chips.

The rest of this paper is organized as follows. Section II presents the proposed mitigation technique with well-slits and its overheads. Accelerated test procedure is explained in Section III, and Section IV shows test results. Section V concludes with a brief summary.

II. PROPOSED MITIGATION TECHNIQUE WITH WELL-SLIT

Fig. 3 illustrates the proposed MBU mitigation technique that inserts well-slits into MBL. There are two types of well-slits; Pwell-slits and Nwell-slits. Nwell-slits split Pwell area and Pwell-slits partition Nwell area. The well-slits can mitigate MBUs which are caused by bipolar action and charge diffusion. The well potential fluctuation due to parasitic bipolar action is confined within a well area, resulting in fewer MBUs. Well splitting also prevents electrons and holes from diffusing to adjacent bits.

For preventing latch-ups, Vodman *et al.* [6] isolated a well from its neighboring wells by deep trenches, which are not included in standard CMOS processes, and the movement of electrons and holes across wells was prevented by the insulator. On the other hand, the proposed method restricts the drift and diffusion of electrons and holes within a well with reversely-biased PN junctions, and it can be used in any standard CMOS processes. In either case, the charge sharing and well potential fluctuation are confined within the isolated well while their process availabilities are different.

We designed an MBL with the proposed MBU mitigation technique in 28 nm technology. The width and length of well-slit are 0.22 um and 1.52 um in the MBL with the proposed MBU mitigation technique. As an MBL macro including a clock buffer and a checker, we have implemented this mitigation technique with only 5.4% area overhead in an MBL macro for SPARC processors [7].

III. IRRADIATION TEST PROCEDURE

We have performed a neutron irradiation test on MBLs for evaluating the efficiency of the proposed MBU mitigation technique. The neutron irradiation test was conducted with spallation (white) neutron beam in Research Center for Nuclear Physics (RCNP) at Osaka University. The beam spectrum is

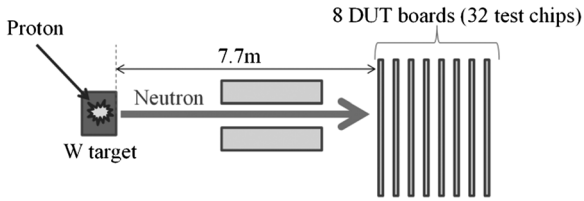


Fig. 5. Neutron test configuration at RCNP.

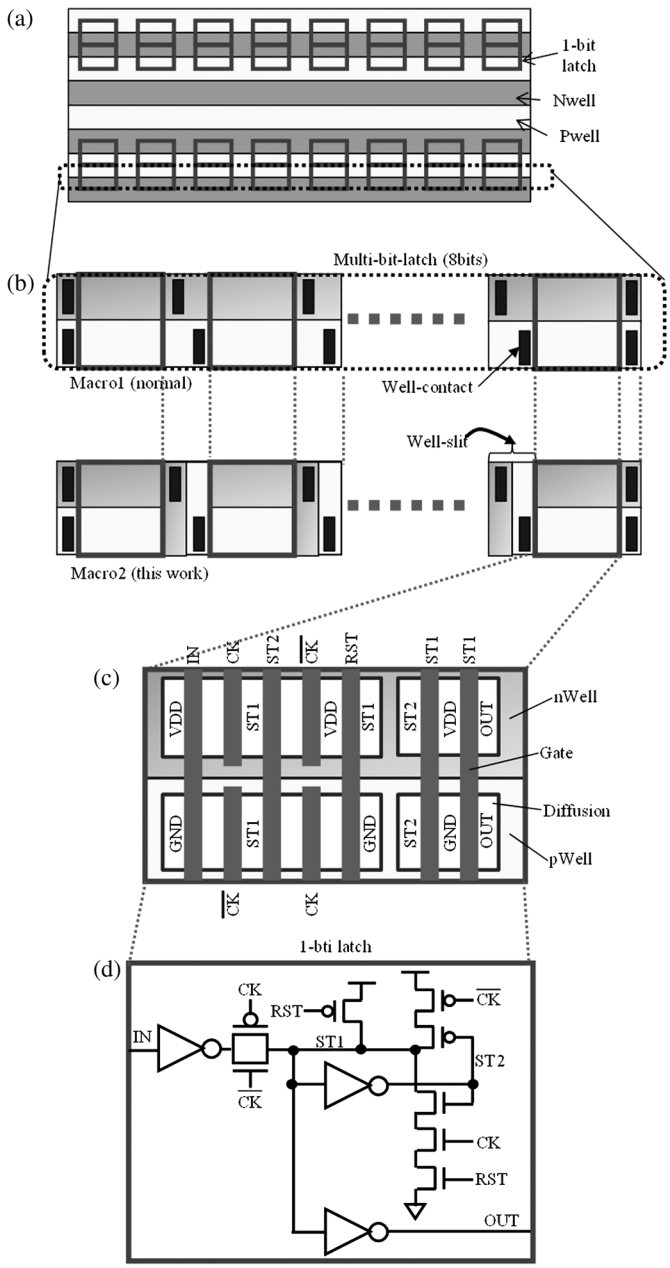


Fig. 6. (a) MBL macro placement on the test chip, (b) layout of 8-bit MBL of two madros on test chip, (c) latch layout and (d) schematic of 1-bit latch.

similar to that of Los Alamos Neutron Science Center (LANCE) and sea level spectrum indicated in JESD89A [8][9]. The average flux of neutrons whose energy is higher than 10 MeV is 2.01 billion neutron/hour/cm^2. Eight test boards were irradiated simultaneously as shown in Fig. 5. The test board has four test

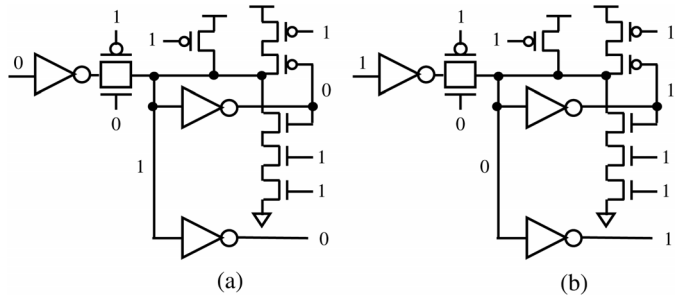


Fig. 7. Node values when retention data is (a) 0 and (b) 1. The input data of the latches are the same with written data during hold operation.

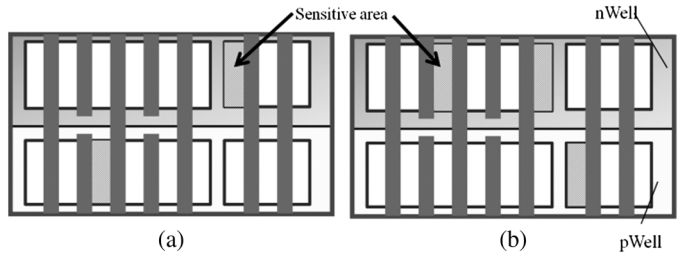


Fig. 8. Sensitive area when retention data is (a) 0 and (b) 1.

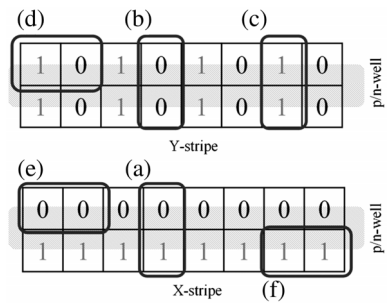


Fig. 9. Test patterns of X-stripe and Y-stripe.

chips and thirty-two test chips were irradiated simultaneously. The test chip includes latch arrays consisting of latches manufactured with double-well (i.e. without deep-Nwell) process in 28 nm bulk CMOS technology. The distance between the tungsten target and the first board is 7.7 meter as shown in Fig. 5. Total irradiation (beam) time is sixty hours, which corresponds to about 1.2 million years in real time. We performed this test aiming to measure upset counts during hold operation.

The chip includes two types of MBLs; Macro1 and Macro2 as illustrated in Fig. 6, and the test chip contains about 50 k bits for each macro. Macro1 is normal MBL and Macro2 is MBL to which the proposed mitigation technique is applied. Each MBL consists of eight-bit latches and one clock buffer as shown in Fig. 2. In Macro2, there are well-slits consisting of Nwell and Pwell between bit cells as explained in Section II. The spaces between latches inside Macro1 and 2 are the same, and for every space well-contacts are placed both in Macro1 and 2. Different from conventional MBL, Macro 1 is designed having the same spaces and well-contacts between latches so that the impact of well-slit is solely evaluated. For this reason, MBL sizes of Macro1 (normal) and 2 (this work) are the same in this test chip. Fig. 6(a) illustrates how the MBLs are laid out

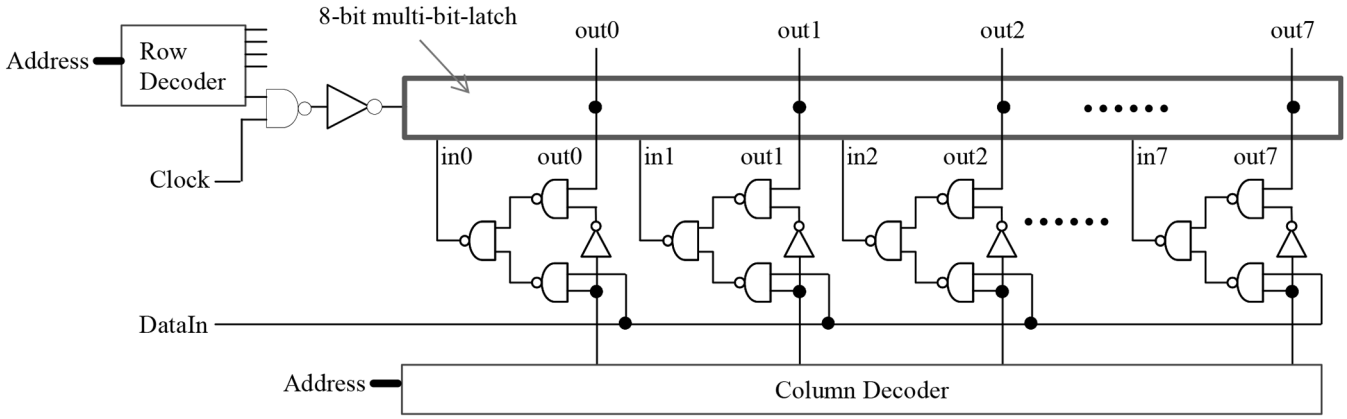


Fig. 10. Controll logic for 8-bit MBL in the test chip.

on the test chip. In this figure, four MBLs are placed, and each of two MBLs shares the well with double-back layout style. For example, the upper two MBLs share the Nwell, and the lower MBLs share the Pwell. These two MBLs that share the same well are called paired MBLs in the following. Note that this placement is done for the same MBL macro, and Macro1 and Macro2 are not mixedly placed.

We evaluated MCU counts in two cases that the same and different data were stored in neighboring bits in an MBL, since MCU occurrence depends on test patterns and corresponding positions of sensitive areas [10]. Fig. 7(a) and (b) show the node values, and Fig. 8(a) and (b) illustrate the sensitive areas when the retention data is "0" and "1", respectively. During hold operation, the input value of each latch is the same with the stored value through a feedback loop, which will be explained later. The test patterns selected for this evaluation are X-stripe and Y-stripe shown in Fig. 9. These test patterns include {0, 0}, {0, 1} and {1, 1} neighboring bits, and hence we can evaluate MCU occurrence against these neighboring bits.

Fig. 10 shows the circuit structure on the test chip for enabling tests with X-stripe and Y-stripe patterns. With the column decoder in this control logic, we can give different values to latches in an MBL although a clock buffer controls all the latches in the MBL simultaneously. A latch selected by the column decoder captures 0/1 from DataIn line, and the other latches not selected by the column decoder are overwritten with the current values. By these steps, we can write arbitrary data patterns into the MBL. In addition, in this structure, single-event-transient at a local clock buffer arising during the hold operation does not contribute to data upset in the MBL since only overwriting is performed [12].

Fig. 11 shows the timing chart of the test procedure. In write phase, we set X-stripe or Y-stripe patterns to the MBLs with 10 MHz clock signal. Then, the MBLs were kept in hold operation for 15 minutes, and the stored values were read out. The supply voltage was 0.75 V in read/write phases and 0.85 V in hold phase. The hold duration is over 1000 times longer than the read/write durations, and the measured upset counts can be regarded as the upset counts during hold operation.

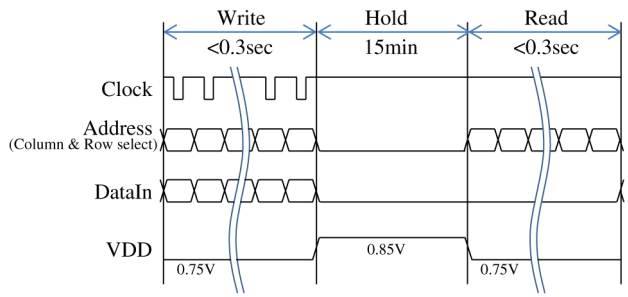


Fig. 11. Test timing chart.

TABLE II
SBU, MCU AND MBU ERROR-BIT COUNTS

		DATA0	DATA1
SBU	Macro 1	676	727
	Macro 2	721	655
MCU	Macro 1	4	92
	Macro 2	0	6
MBU	Macro 1	2	86
	Macro 2	0	0

IV. EXPERIMENTAL RESULTS

Table II lists the error-bit counts of SBU, MCU and MBU. The proposed MBU mitigation technique does not increase SBU rate as shown in Table II. An increase in SBU rate leads to frequent instruction retries in HIR and consequent performance degradation. This result demonstrates that the proposed mitigation technique does not involve performance overhead.

We observed totally twenty-seven MCU events in Macro 1 (normal) in this irradiation test. Table II. shows the number of bits flipped in total in the twenty-seven MCU events. There is MCU difference between DATA0 and DATA1, whereas SBU rates are not much different between DATA0 and 1 as shown in Table II. The MCU error-bit counts for DATA0 and DATA1 latches are separately shown, where DATA0/DATA1 latch means a latch whose retention data is "0"/"1".

A primary factor of soft-error in latches is charge collection to NMOS in DATA0 and to PMOS in DATA1 because the

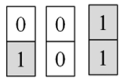
	Pattern	MCU count on Macro 1	MCU count on Macro 2
Vertical	(a) (b) (c) 	1	3
Horizontal	(d)  (e)  (f) 	1	0

Fig. 12. MCU counts (event) when stored value in neighboring bits are {0, 0}, {0, 1} and {1, 1} on vertical and horizontal sides as refer to Fig. 9.

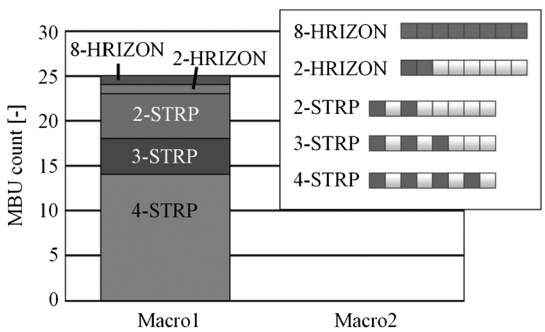


Fig. 13. MBU counts in neutron irradiation test on macro1 (normal) and macro2 (with well-slit) of 28 nm latches.

latch circuits consist of unbalanced feedback loop circuits [13]. These test results show that PMOS and NMOS equally contribute SBU rate, while PMOS contribute MCU rate more than NMOS in MBL. A possible reason is that single event upset reversal (SEUR) in NMOS decreased MCU. It is reported that SEUR is more influential in NMOS than in PMOS [14]–[16].

We next focus on the MCUs upsetting adjacent two latches, and count the number of MCUs separately depending on the stored values ({0, 0}, {0, 1} and {1, 1}) and their spatial direction. Fig. 12 shows the MCU counts, where the spatial classification was performed for paired 8 bit-MBLs (Fig. 6(a)). Only five MCUs were observed in adjacent two latches, while twenty-seven MCUs were observed in total. The MCU count is quite few, and unfortunately the pattern dependency cannot be discussed further. But, it should be noted here that vertical MCU patterns of (a), (b) and (c) are not MBU and do not contribute to fails of the processor with HIR, since each MBL includes only a single error. In this case, the error is detected by the checker and predictor, and the processor with HIR can retry the instruction.

The proposed MBU mitigation technique with well-slits dramatically reduced MBU in the MBL. The neutron irradiation test results of Fig. 13 and Table II show that no MBU was observed in Macro2 (this work), whereas 25 MBU events and consequent 88 bit-errors occurred in Macro1 (normal). Here, MCU spatial patterns resulting in MBU depend on the predictor and checker implementation. Parity and residue check whose divisor is three or seven are widely used for the predictor and checker implementation. The parity check can detect an even number of errors, but cannot detect an uneven number of errors in the MBL. Consequently, when the parity check is used, 8-HRIZON, 2-HRIZON, 2-STRP and 4-STRP shown in Fig. 13 are MBUs, and HIR is not invoked. The residue check can detect one error, but cannot always detect two or more errors. Accordingly, in case of the residue check, 3-STRP can be MBU and may not invoke HIR. The irradiation results in Fig. 13 clearly demonstrate that the MBL with the proposed mitigation technique contributes to reliability enhancement of electron devices.

V. Conclusion

We proposed a technique for mitigating MBU in MBL by inserting well-slits between latch bit cells. The area overhead is only 5.4% as an MBL macro for processors including clock buffer and checker. Neutron irradiation tests clarified that the proposed mitigation technique did not change SBU rate and consequently did not degrade processor performance. It is clearly demonstrated that the proposed mitigation technique can achieve robustness against MBUs, which cannot be detected by the checker and predictor, have not been observed in the proposed MBL even under sixty-hour accelerated irradiation. The MBL with the proposed mitigation technique helps attain excellent reliability of electronic devices.

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