Soft Error Immunity of Subthreshold SRAM

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***Abstract*—This paper discusses soft error immunity of subthreshold SRAM presenting neutron- and alpha-induced soft error rates (SER) in 65-nm 10T SRAM over a wide range of supply voltages from 1.0 to 0.3 V. The results show that the neutron-induced SER at 0.3 V is 7.8 times as high as that at 1.0 V. The measured multiple cell upsets (MCUs) included 8-bit MCU. With 0.4V operation of the SRAM under test, protons are not dominant secondary particles causing SEU, but this paper points out that protons must be considered for future near-threshold computing. The alpha-induced SER at 0.3V is 6x higher than that at 1.0V. These results can contribute to reliability estimation and enhancement in subthreshold circuit design.**

I. Introduction

Supply voltage scaling is a key to reduce the power dissipation in a CMOS digital circuit. Especially, an aggressive voltage scaling down to threshold voltage can achieve a significant reduction in power dissipation [1]. Therefore, subthreshold circuits that operate at a lower supply voltage than the threshold voltage are promising for ultra-low power applications, such as processors for sensor networks and medical applications. However, subthreshold circuits are extremely sensitive to manufacturing variability and environmental fluctuation. This sensitivity has been a major concern, and many researchers have investigated ways to cope with it [2], [3]. However, little attention has been paid to the vulnerability of subthreshold circuits to radiation particles.

Studies have shown that the neutron-induced soft error rate (SER) in static random access memory (SRAM) increases as the supply voltage is lowered [4], [5]. This is because reducing the supply voltage decreases the energy required to cause upsets. These studies, however, were done using a voltage between the nominal supply voltage and 0.8 V. If the SER in the subthreshold region was much larger than that in the super-threshold (nominal supply voltage) region, it would not be appropriate to use subthreshold circuits in actual applications. Therefore, subthreshold circuits, especially SRAM, need to be made immune to soft errors. Besides, in terrestrial environment, soft errors are induced by alpha particles emitted from package material and neutrons originating from cosmic ray. We thus need to understand alpha- and neutron-induced soft error mechanisms and characterize immunity of subthreshold SRAM.

This paper discusses soft error immunity of subthreshold SRAM to both neutron and alpha, and presents measurement results of alpha- and neutron-induced soft errors in 10T SRAM over a wide range of supply voltages between 1.0 and 0.3 V reported in [6]–[8]. This paper also mentions future trends on neutron-induced soft error.

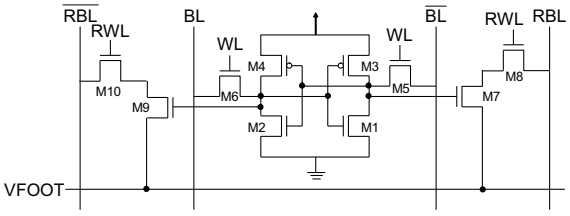

Fig. 1. Structure of 10T memory cell [8].

II. Test structure and experimental setup

A test chip including a 256 kb 10T SRAM was fabricated in a 65-nm CMOS process with triple well structure. Figure 1 shows the cell structure of the 10T SRAM. This SRAM can operate even at 0.3 V, because the cross-coupled inverters are large enough to mitigate threshold voltage variability. The size of a memory unit is 4.4 μm $\times$ 0.8 μm. In order to investigate the contribution of the parasitic bipolar action, which will be explained in the next section, to the occurrence of MCUs, we implemented two types of memory cell arrays having different distances between the well ties; 25.6 μm (wide) and 6.4 μm (narrow).

Vulnerability of a memory cell to radiation particles is often evaluated using critical charge, which is defined as the minimum charge required to flip the data stored in a memory cell. Figure 2 shows the critical charge obtained by circuit simulation with a double exponential current model. The critical charge decreases as the supply voltage is reduced, which means that a reduction in the supply voltage degrades immunity to radiation particles.

Radiation experiments were carried out as follows. Accelerated high-energy-neutron SER measurements were performed at the Research Center for Nuclear Physics (RCNP) at Osaka University, Japan [5]. The energy spectrum of the RCNP neutron source is similar to the terrestrial neutron energy spectrum [5], [9]. For alpha irradiation, we used an Am-241 foil as an alpha particle source. The main peak energy of the alpha particle is 5.49 MeV. The foil was placed immediately above the die in accordance with JEDEC standards.

III. Neutron-induced soft errors

A. Mechanism

Neutrons indirectly induce soft-error through reaction with atomic nucleus of transistor materials as shown in Figure 3. The nuclear reaction generates charged secondary particles like protons, alpha particles and heavy ions. The charged particle generates electron-hole pairs on the particle track and deposits

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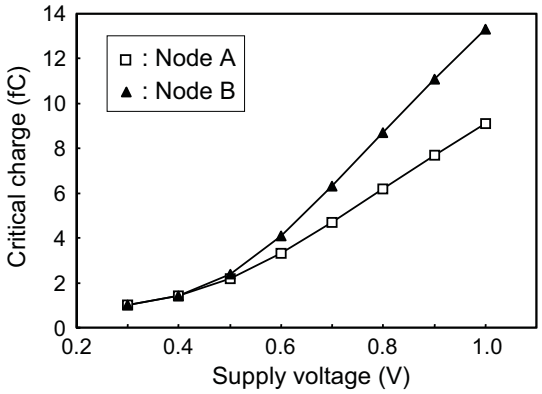


Fig. 2. Simulated critical charge of 10T memory cell as a function of supply voltage in 65nm CMOS process [8]. Nodes A and B represent two individual sensitive nodes in a memory cell.

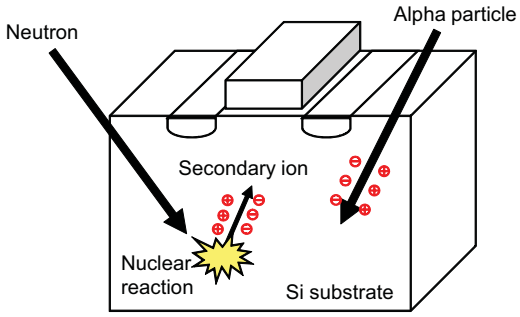


Fig. 3. Soft error mechanism due to neutron and alpha.

charge. The generated charge is collected to drain by drift and diffusion, and causes soft error.

Multiple cell upsets (MCUs) induced by a single neutron are becoming a serious concern [5], [9], [10]. MCUs can be mostly mitigated by interleaving and ECC (error correction code). On the other hand, as the number of upsets for an event becomes larger, MCU patterns which cannot be eliminated by interleaving and ECC are more likely to arise. Such critical MCUs are called MBU (multiple bit upsets), and they prevent massively-parallel high-performance computing systems and highly reliability-demanding applications from being implemented and operated. Besides, there are four possible mechanisms of MCU; (1) successive hits of an ion, (2) multi hits by multiple ions, (3) charge drift/diffusion (charge sharing), and (4) parasitic bipolar action. Among these, (3) charge sharing and (4) parasitic bipolar action are major mechanisms at the nominal supply voltage. Charge sharing causes MCU due to charge diffusion to multiple cells. Parasitic bipolar action triggered by changing well potential flips multiple cells in a well. Figure 4 illustrates the parasitic bipolar action. Holes generated by a neutron-induced nuclear reaction increase the voltage of the p-well, which is equivalent to the base-emitter voltages of the parasitic bipolar transistors, due to well resistance. Consequently, the collector-emitter currents of the parasitic bipolar transistors increase, which causes MCUs.

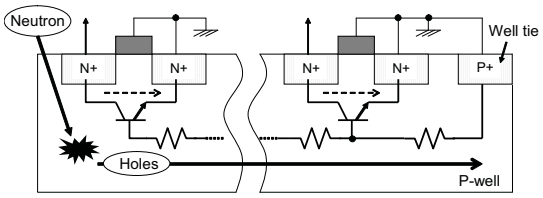


Fig. 4. Cross section of NMOSs in memory cells. Parasitic bipolar transistors cause multiple upsets due to increase in potential of p-well [8].

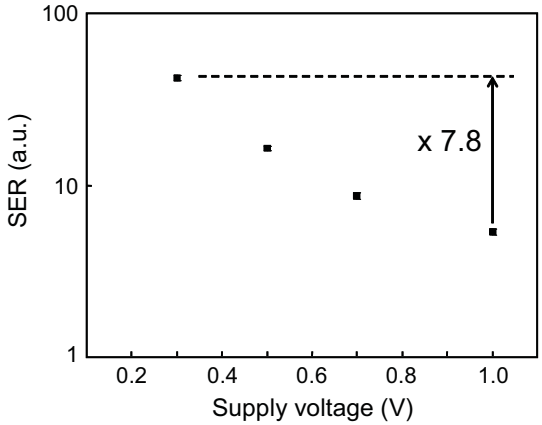


Fig. 5. SER as a function of supply voltage of memory cell array [8]. Each error bar indicates $\pm 3\sigma$, where σ is defined as the square root of the number of the observed upsets.

In terms of supply voltage, these two mechanisms have opposite tendencies. As the supply voltage becomes lower, the critical charge becomes smaller, which results in SER increase. On the other hand, parasitic bipolar action becomes less active, and consequently SER decreases. As a mixture of these two tendencies, the dependency of MCU on voltage is determined.

B. Measurement results

Figure 5 shows the neutron-induced SER as a function of the supply voltage. The SER increases as the supply voltage is reduced. The SER at 0.3 V is 7.8 times higher than at 1.0 V.

Figure 6 illustrates the dependence of the SBU and MCU rates on the supply voltage. The MCU rate was derived by dividing the number of failing bits (for example, a “2b MCU” was considered to be two errors) by the measurement period. The SBU rate dramatically increases as the supply voltage is reduced.

As described with Fig. 2, the decrease in the supply voltage reduces the critical charge. Ibe *et al.* [11] reported that SBU is dominated more significantly as scaling proceeds due to lighter particles such as protons and alpha particles, which are secondary particles produced by the nuclear reaction between neutrons and Si. Although rigidly speaking the reduction in the supply voltage and the device miniaturization are different in terms of the sensitive volume and the charge collection efficiency, the supply voltage reduction corresponds to the device miniaturization in terms of the critical charge. Decomposition of SEUs into their triggering secondary particles will be discussed in Section III-C.

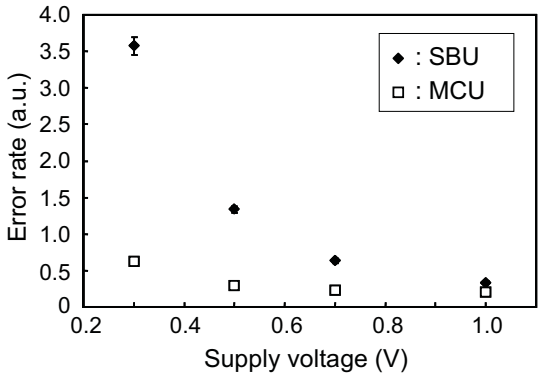
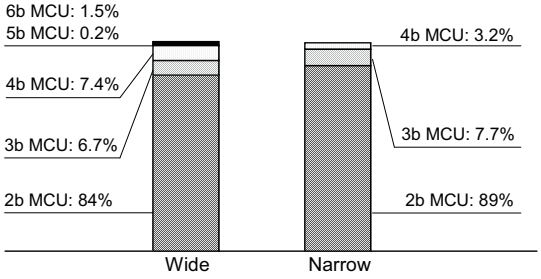


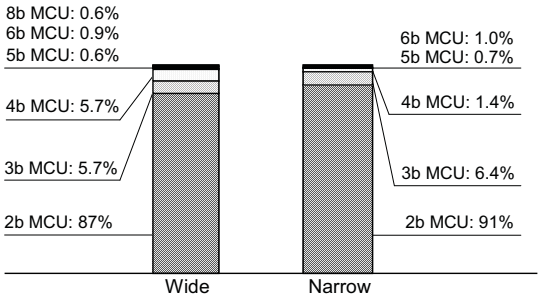
Fig. 6. SBU and MCU rates as a function of supply voltage of memory cell array [8]. SBU and MCU rates are plotted with error bars, where each error bar indicates $\pm 3\sigma$.

On the other hand, the dependence of the MCU rate on the supply voltage is smaller than that of the SBU rate. Contributions of lighter particles to MCUs are less than those to SBUs [11]. Previous work [9] has shown that the MCU rate is less sensitive to the supply voltage between 1.2 and 0.7 V and concluded that this is because most neutron-induced MCUs are caused by the parasitic bipolar action. Interestingly, however, the MCU rate shown in Fig. 6 slightly increases when the supply voltage is below 0.5 V. Remind that charge sharing and parasitic bipolar action have opposite directions in terms of supply voltage, as mentioned in Section III-A. While the parasitic bipolar action is the dominant mechanism of MCUs in the super-threshold region in our design, the effect of charge-sharing becomes larger in the subthreshold region, which results in the increase in the MCU rate between 0.3 and 0.5 V, as depicted in Fig. 6.

Finally, the MCU distributions in the memory cells with wide and narrow well-tie distances are shown in Fig. 7. Large-bit MCUs are likely to occur in memory cells with a wide well-tie distance compared to ones with a narrow well-tie distance. A decrease in the supply voltage also increases the probability of large-bit MCUs due to the decrease in the critical charge. 8-bit MCU was observed at 0.3V.



(a) $V_{DD} = 1.0\ V$



(b) $V_{DD} = 0.3\ V$

Fig. 7. Comparison of MCU distributions [8].

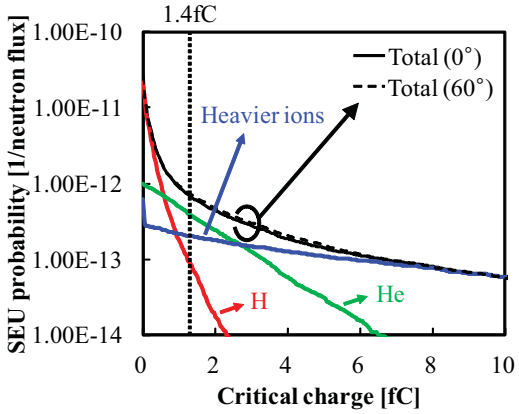


Fig. 8. Simulated SEU probability of each ion as a function of critical charge [7].

C. Simulation

To investigate the secondary particles contributing SEUs, a Monte-Carlo simulation was performed using PHITS (Particle and Heavy Ion Transport code System) [12]. PHITS was employed to simulate neutron-induced soft errors together with a 3-D TCAD (Technology Computer Aided Design) simulator [13]. In the present work, on the other hand, the collected charge is calculated by a sensitive volume model [14].

Figure 8 shows the simulated SEU probability including both SBU and MCU per neutron flux as a function of critical charge at the incident angles of 60° and 0°. Individual contributions from secondary H (proton), He (alpha), and heavier ions to the SEU are separated for the result of 0° in Figure 8. There is little difference between the SEU probabilities at the angles of 60° and 0°. On the other hand, the critical charge of our 10T SRAM in 0.4-V operation is estimated by circuit simulation to be 1.4 fC (Figure 2). Therefore, He and heavier ions are the dominant secondary ions causing SEUs in 0.4-V operation because these ions occupy 89 % of the SEU probability at 1.4 fC of critical charge.

At 0.4V operation, protons are not dominant, but an upcoming result with other SRAM at 0.19V will present a dramatic SEU increase, which is well explained by proton contribution [15].

IV. Alpha-induced soft errors

Alpha particles, which are charged particles unlike neutrons, directly cause electron-hole pairs and deposits charge, which induces soft error, as illustrated in Fig. 3. Energy of alpha particles attenuates even in air and they cannot penetrate

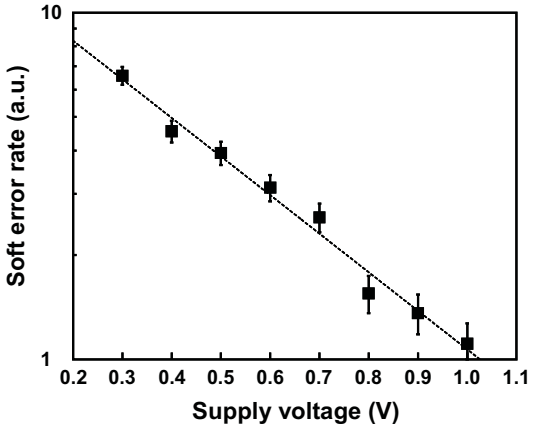


Fig. 9. SERs as a function of the supply voltage of the memory cell array [6]. The Y-axis is shown in log scale. Each error bar indicates $\pm 3\sigma$, where σ is defined as the square root of the number of the observed upsets. The dotted line represents the fitted curve by exponential approximation.

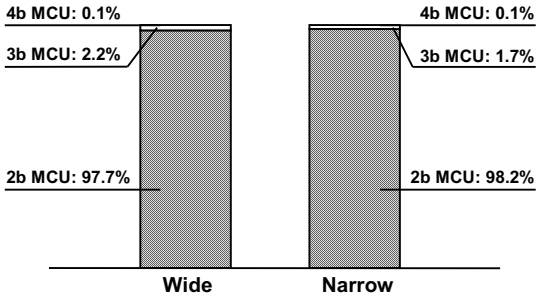


Fig. 10. Measured MCU distribution at $V_{DD} = 300$ mV [6].

deeply into materials.

Figure 9 shows the measured SERs as a function of the supply voltage of the memory cell array. SER has an exponential dependence on the supply voltage, and SER at 0.3 V is six times higher than that at 1.0 V.

Figure 10 shows the measured MCU distribution at $V_{DD} =$ 300 mV. Compared with the MCU distribution induced by neutron (Fig. 7), the number of bits of alpha-particle-induced-MCUs is smaller, and 98% of them are 2-bit MCUs.

V. Conclusion

This paper presented neutron- and alpha-induced soft errors in subthreshold SRAM. With the 10-T subthreshold SRAM designed for 0.3V read and write operations fabricated in 65 nm CMOS technology, we observed 8x and 6x soft error increases at 0.3V for alpha and neutron, respectively, compared to 1.0V operation. 8-bit MCU was induced by neutron at 0.3V, which suggests large-scale and/or reliability-demanding ultra low-voltage circuits need MCU mitigation techniques. While protons are not dominant secondary particles at 0.4V in this SRAM, a clear observation that secondary protons are causing SEUs will be presented soon [15], and designers must pay attention to drastic SER increase. Near-threshold computing at 11nm, which is drawing attention in exa-scale computing, is likely to face with this secondary proton problem.

Acknowledgement

The author thanks Prof. Hiroshi Fuketa of Univ. of Tokyo and Mr. Ryo Harada of Osaka University for their contributions to the measurement and analysis. The author also acknowledges simulations and fruitful discussions with Dr. Shinichiro Abe, Prof. Yukinobu Watanabe of Kyushu University and Mr. Taiki Uemura of Fujitsu Semiconductor Ltd.

References

[1] A.W. Wang, B.H. Calhoun, and A.P. Chandrakasan, *Sub-threshold Design For Ultra Low-Power Systems*, New York: Springer, 2006.

[2] H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "Adaptive Performance Compensation with In-Situ Timing Error Predictive Sensors for Subthreshold Circuits," *IEEE Trans. on VLSI Systems*, vol. 20, no. 2, pp. 333–343, Feb. 2012.

[3] H. Fuketa, D. Kuroda, M. Hashimoto, and T. Onoye, "An Average-Performance-Oriented Subthreshold Processor Self-Timed by Memory Read Completion," *IEEE Trans. on Circuits and Systems II*, vol. 58, no. 5, pp. 299–303, May 2011.

[4] P. Hazucha, T. Karnik, J. Maiz, S. Walstra, B. Bloechel, J. Tschanz, G. Dermer, S. Hareland, P. Armstrong, and S. Borkar, "Neutron Soft Error Rate Measurements in a 90-nm CMOS Process and Scaling Trends in SRAM from 0.25-mm to 90-nm Generation," in *Intl. Electron Device Meeting Tech. Dig.*, 2003, pp. 21.5.1–21.5.4.

[5] Y. Tosaka, H. Ehara, M. Igeta, T. Uemura, H. Oka, N. Matsuoka, and K. Hatanaka, "Comprehensive Study of Soft Errors in Advanced CMOS Circuits with 90/130 nm Technology," in *Intl. Electron Device Meeting Tech. Dig.*, 2004, pp. 38.3.1–38.3.4.

[6] H. Fuketa, R. Harada, M. Hashimoto, and T. Onoye, "Measurement and Analysis of Alpha-Particle-Induced Soft Errors and Multiple Cell Upsets in 10T Subthreshold SRAM," *IEEE Trans. on Device and Materials Reliability*, in press.

[7] R. Harada, S. Abe, H. Fuketa, T. Uemura, M. Hashimoto, and Y. Watanabe, "Angular Dependency of Neutron Induced Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM," *IEEE Trans. on Nuclear Science*, vol. 59, no. 6, pp. 2791–2795, Dec. 2012.

[8] H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "Neutron-Induced Soft Errors and Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM," *IEEE Trans. on Nuclear Science*, vol. 58, no. 4, pp. 2097–2102, Aug. 2011.

[9] T. Nakauchi, N. Mikami, A. Oyama, H. Kobayashi, H. Usui, and J. Kase, "A Novel Technique for Mitigating Neutron-Induced Multi-Cell Upset by means of Back Bias," in *Proc. Int. Reliability Phys. Symp.*, 2008, pp. 187–191.

[10] E. Ibe, S.S Chung, S. Wen, H. Yamaguchi, Y. Yahagi, H. Kameyama, S. Yamamoto, and T. Akioka, "Spreading Diversity in Multi-cell Neutron-Induced Upsets with Device Scaling," in *Proc. Custom Integr. Circuits Conf. (CICC)*, pp. 437–444, 2006.

[11] E. Ibe, H. Taniguchi, Y. Yahagi, K. Shimbo, and T. Toba, "Impact of Scaling on Neutron-Induced Soft Error in SRAMs From a 250 nm to a 22 nm Design Rule," *IEEE Trans. Electron Devices*, vol. 57, pp. 1527–1538, Jul. 2010.

[12] K. Niita, N. Matsuda, Y. Iwamoto, H. Iwase, T. Sato, H. Nakashima, Y. Sakamoto, and L. Sihver, "PHITS: Particle and Heavy Ion Transport code System, Version 2.23," JAEA-Data/Code. 2010-022, Japan Atomic Energy Agency, 2010.

[13] S. Abe, Y. Watanabe, N. Shibano, N. Sano, H. Furuta, M. Tsutsui, T. Uemura, and T. Arakawa, "Multi-scale monte carlo simulation of soft errors using PHITS-HyENEXSS code system," *IEEE Transactions on Nuclear Science*, vol.59, no.4, pp. 965-97, 2012.

[14] Y. Tosaka, H. Kanata, S. Satoh, and T. Itakura, "Simple method for estimating neutron-induced soft error rates based on modified BGR model," *IEEE Electron Device Letters*, vol.20, pp. 89-91, 1999.

[15] T. Uemura, T. Kato, H. Matsuyama, and M. Hashimoto, "Soft-Error in SRAM at Ultra Low Voltage and Impact of Secondary Proton in Terrestrial Environment," *IEEE Nuclear and Space Radiation Effects Conference*, to be presented.