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Robust Subthreshold Circuit Design to Manufacturing and Environmental Variability

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Subthreshold circuits are drawing attention for ultra-low power application. However, subthreshold circuits have inherent problems that their performance is extremely sensitive to manufacturing and environmental variability and they are susceptible to soft errors. This paper reviews characteristics and problems of subthreshold circuits, and discusses some works for improving the robustness of subthreshold circuits from device, circuit and CAD perspective.

Introduction

Supply voltage scaling is a key to reduce the power dissipation in a CMOS digital circuit. Especially, an aggressive voltage scaling down to threshold voltage can achieve a significant reduction in power dissipation (1). For a long time, this region, i.e. subthreshold region, has been considered as a troublesome region causing a leakage current of a transistor. However, recent researches have proposed to exploit subthreshold region for ultra-low power operation, since aggressive process scaling down to nano scale allows an operation with clock frequencies up to megahertz range. Figure 1 plots the VTC (voltage transfer characteristic) of a CMOS inverter in a 90-nm CMOS process at various supply voltages. Threshold voltages of NMOS and PMOS in this process are both 0.3–0.4 V. These VTCs indicate that the inverter can function correctly even when the supply voltage is 0.1 V which is deeply below the threshold voltage. A theoretical limit for the lowest operation voltage is estimated to 52 mV (2).

A circuit operating at lower supply voltage than the threshold voltage is called a subthreshold circuit. In this paper, near-threshold circuits are included in subthreshold circuits. Subthreshold circuits work just at low speed, while consuming ultra-low power. Thus, it is appropriate to apply subthreshold circuits to severely energy-constrained equipment with low demands for their operation speeds. Promising applications include processors for sensor networks such as habitat monitoring (3), health monitoring (4), and structural health monitoring (5), and biomedical equipment such as hearing aid (6).

For such ultra-low power applications, various subthreshold circuits have been proposed. At early research stage, basic circuit components such as adders, multipliers and filters are reported (6-10). Later, advanced processors operating in subthreshold region are implemented (11-20). Looking at recent two years, Intel developed an IA-32 microprocessor that operates at 280 mV to 1.2 V (21). TI designed a full DSP at 0.6 V (22). In addition as a new application, a cubic-millimeter wireless intraocular pressure sensor is proposed (23). A new trend with a small volume implementation and permanent operation by energy harvesting is expected.

This paper reviews characteristics of subthreshold circuits and introduces techniques for coping with manufacturing and environmental variability.

Characteristics and problems of subthreshold circuits

Characteristics in subthreshold region

A MOSFET operates in weak inversion or subthreshold region when its gate-source voltage V_{gs} is below its threshold voltage V_{th}. In this region, the drain current I_{ds} of NMOS can be written as (9)

$$I_{ds} = I_0 e^{\frac{V_{gs}-V_{th}}{nV_t}}, \quad [1]$$

$$I_0 = \mu C_{ox} \frac{W}{L}(n-1)V_t^2. \quad [2]$$

where μ is the mobility, C_{ox} is the gate-oxide capacitance, n is the subthreshold swing parameter, L is the channel length, W is the channel width, and V_t is the thermal voltage. Delay time T_d of a subthreshold circuit operating at supply voltage V_{DD} is proportional to the inverse of ON current Ion which is a drain current at $V_{gs} = V_{ds} = V_{DD}$.

$$T_d \propto \frac{1}{I_{on}} = \frac{1}{I_{ds}(V_{ds} = V_{gs} = V_{DD})} \propto \frac{1}{\mu \cdot e^{\frac{V_{DD}-V_{th}}{nV_t}}}. \quad [3]$$

This equation indicates that a circuit delay in a subthreshold circuit has the exponential dependence on supply voltage V_{DD}. Figure 2 plots a simulated oscillation frequency of a 17-stage RO (ring oscillator) as a function of the supply voltage in a 90-nm CMOS technology. The oscillation frequency drops exponentially as the supply voltage is reduced. The frequency at V_{DD} = 0.1 V is 1/3000 smaller than that at V_{DD} = 1.0 V which is a nominal supply voltage of this process.

Next the power dissipation of subthreshold circuits is discussed. Power dissipation P of a CMOS digital circuit with operating frequency f is calculated as

$$P = \alpha C V_{DD}^2 f + t_{sc} V_{DD} I_{sc} f + V_{DD} I_{leak}. \quad [4]$$

The first term represents a dynamic power dissipation, where α is the switching activity and C is the total capacitance of the circuit. The second term is a power dissipation by the direct path current I_{sc}, where t_{sc} represents the period when both PMOSs and NMOSs are conducting. The third term is a leakage power dissipation where I_{leak} is the total leakage current of the circuit. All the terms have the same directional dependence on V_{DD}, that is, lowering V_{DD} can reduce the power dissipation.

Figure 3 shows a relation between the power dissipation and the supply voltage in a 17-stage RO. The power dissipation at V_{DD} = 0.1 V is reduced by 1/10000 indeed in comparison with that at V_{DD} = 1.0 V.

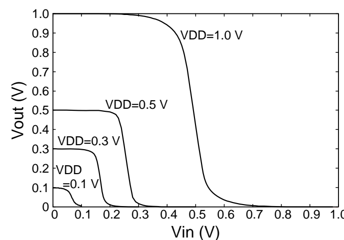

Fig. 1: Voltage transfer Curve of an inverter in 90 nm process.

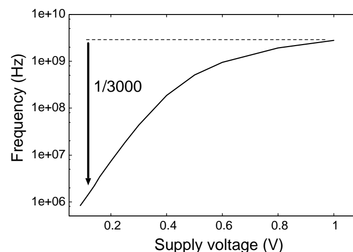

Fig. 2: Oscillating frequency a 17-stage ring oscillator in 90 nm process.

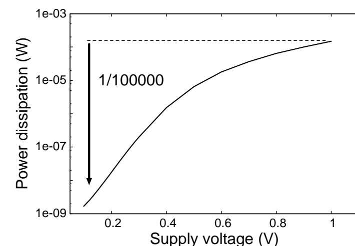

Fig.3: Power dissipation of a 17-stage ring oscillator in 90 nm process.

Optimal supply voltage

Equation 4 implies that an ultra-low-voltage operation can reduce the power dissipation extremely. Some previous works (2, 24-26) explored the minimum supply voltage by adjusting the body-bias voltages to balance threshold voltages of NMOSs and PMOSs. An FIR filter can achieve 85 mV operation in (25) and implementation using Schmitt-Trigger logic enables 62 mV operation (26).

On the other hand, many researches (9-11, 14–19, 27) have pointed out that the lowest supply voltage is not optimal in terms of energy efficiency. An energy per cycle E can be derived from Eq. 4 as

$$E = \frac{P}{f} = \alpha C V_{DD}^{2} + \frac{V_{DD} I_{leak}}{f}. \qquad [5]$$

where the power dissipation by the direct path current is ignored for simplicity. From Eq. 1, leakage current I_{leak} is derived as,

$$I_{leak} \propto I_{ds}(V_{ds} = V_{DD}, V_{gs} = 0\text{V}) \propto e^{\frac{-V_{th}}{nV_t}}. \qquad [6]$$

This equation implies that I_{leak} does not depend on V_{DD}. Strictly speaking, V_{th} is affected by V_{DD}, yet the influence is a secondary effect and it is small. In contrast, operating frequency exponentially drops as the supply voltage is lowered as shown in Fig. 2. Consequently, the leakage energy, the second term in Eq. 6, dramatically rises in subthreshold region. Since the first term, the dynamic energy, is reduced by a decrease in the supply voltage, the leakage energy becomes dominant below a certain supply voltage. For example, the dynamic and leakage energy of a ripple carry adder when the clock cycle is set to its delay are plotted in Fig. 4. As shown in this figure, the total energy becomes the smallest at 300 mV, and the operation at below this voltage is less meaningful in terms of energy efficiency.

The optimal voltage depends on a circuit structure, and measurement results in various subthreshold circuits (9–11, 14–19) show that the optimal supply voltages are between 250 mV and 400 mV.

Problems

Subthreshold circuits have a problem that their performances are extremely sensitive to manufacturing variability and environmental variability such as temperature and supply voltage fluctuations. In addition, subthreshold circuits have been thought to be vulnerable to soft errors. This paper focuses on manufacturing variability and environmental fluctuation.

Device parameters such as threshold voltage, channel length, and oxide thickness of every transistor in a circuit fluctuate due to manufacturing variability. Figure 5 shows oscillation frequencies of a 17-stage RO at SS (slow NMOS and slow PMOS) and FF (fast NMOS and fast PMOS) process corners in a 90-nm CMOS process. When the supply voltage is 1.0 V, the frequency at the best process corner is 1.7 times as fast as that at the worst corner. As the supply voltage is lowered down to 0.3 V, the frequency at the best process corner becomes 8 times faster. This means that manufacturing variability has a great impact on the performance fluctuation in subthreshold circuits.

In this thesis, temperature and supply voltage variations are considered as environmental variability. First, the sensitivity to temperature is described. The circuit delay depends on threshold voltage V_{th} and mobility μ according to Eq. 3. The rise in temperature decreases V_{th}, which causes speeding up the circuit, whereas the rise in temperature decreases μ, which results in the degradation of the circuit delay. This means that the influence of temperature on the circuit delay depends on the supply voltage (29). Figure 6 illustrates the simulated oscillation frequency in a 17-stage RO as a function of

temperature. When supply voltage VDD is 0.3 V, the frequency at 80 °C doubles comparing to that at 25 °C. On the other hand, when V_{DD} is 1.0 V, the frequency at 80 °C is lower by just 4%. This means that the circuit delay in the subthreshold circuits is also significantly sensitive to temperature.

As for the supply voltage fluctuation, many researchers have paid attention to power supply noise in super-threshold circuits. However, it is expected that power supply noise has a less impact on subthreshold circuits, because the current is reduced exponentially as the supply voltage is lowered and the noise magnitude becomes much smaller. On the other hand, applications powered by a battery or energy scavenging often suffer from the degradation in the supply voltage level due to low battery charge or bad environmental condition. Since the performance of subthreshold circuits is sensitive to the supply voltage as described in Fig. 2, the supply voltage is also taken into account as a factor of environmental variability.

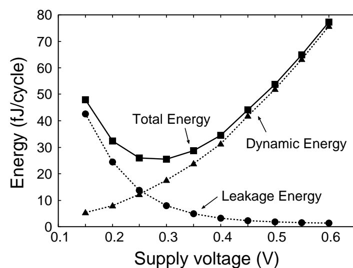

Fig. 4: Energy per cycle of carry propagation adder in 90nm process.

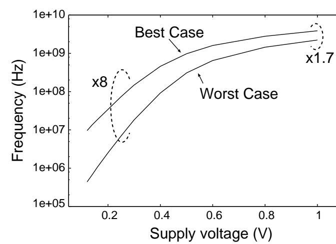

Fig. 5: Frequency of a 17-stage RO in best and worst corners in 90nm process.

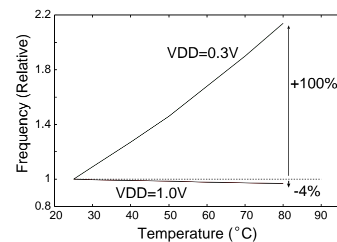

Fig. 6: Frequency and temperature of a 17-stage RO in 90nm process.

Robust subthreshold circuit design

We are working for putting subthreshold circuits robust to practical use at device, circuit and CAD levels. At device level, we constructed a transistor variability model that reproduces subthreshold circuit performance (29), and evaluated soft error immunity of subthreshold SRAM (30-32). At circuit level, adaptive performance control is studied parting from conventional worst-case design (33). For implementing efficient adaptive control, design methods are developed, such as a stochastic evaluation framework of timing error and power consumption (34) and body-bias clustering (35). Furthermore, we propose a self-timed processor to cope with large variation in memory access time (36). In this paper, adaptive speed control is introduced below.

V_{th} variation due to manufacturing variability and temperature fluctuation significantly varies speed and power consumption of subthreshold circuits. If adding up worst-cases for each variation factor, power dissipation may increase more than 10x. We therefore devise an adaptive speed control scheme shown in Figure 7 (33). The error predictive flip-flop causes a setup violation earlier than the main flip-flop due to the inserted delay element. This error signal is used as a warning signal indicating a shortage of timing slack, and the circuit is speeded up or down according to this signal.

This adaptive speed control is applied to a 32-bit Kogge-Stone adder. A test chip was fabricated in 65nm process. Figure 8 shows a measurement results under temperature variation. In this test chip, the circuit speed is adjusted by body-biasing. (a) corresponds to the proposed speed control, (b) is the power dissipation when 200 mV forward body-bias is given to satisfy the speed requirement at 25°C, and (c) is the power dissipation when the minimum body-bias is given at each temperature. This result shows that the

power dissipation of the proposed speed control is close to (c) and the speed control is well working. Compared to conventional adaption of (b), the power dissipation is reduced by 40%.

When this adaptive speed control is applied to run-time operation, there is a fundamental problem that timing errors cannot be completely eliminated. This is because the circuit could be slowed down excessively, if critical paths are not activated for a long time, the circuit could be slowed down excessively. The probability of timing error occurrence depends on the positions of error predictive flip-flops and the amount of delay element. In order to quantitatively evaluate the timing error probability and its dependence on design parameters, we developed a stochastic evaluation framework using Markov model (34).

A 32-bit ripple carry adder is analyzed by the proposed framework. Figure 9 shows an evaluation result when the location of error predictive flip-flop is varied. For each location, several points are plotted where the value of delay element is changed. This figure shows that there is a trade-off between timing error probability and power dissipation. In addition, depending on the target error probability, the optimal position and its delay value change, and they can be identified by the proposed framework.

Finally, a body-bias clustering is introduced which efficiently controls circuit speed. It generates several gate groups in each of which the same body voltage is shared, taking into account the timing slacks of gates. By changing the body voltage group by group, a finer performance control is realized. (35) proposes a tuning-friendly body-bias clustering method. In the clustering, timing and leakage after speed control are analyzed statistically, and an optimal clustering for minimizing the average leakage after adaptation is explored. The proposed method is applied to a multiplier (V_{DD}=300mV), and leakage power is reduced by 70% compared to non-clustering case.

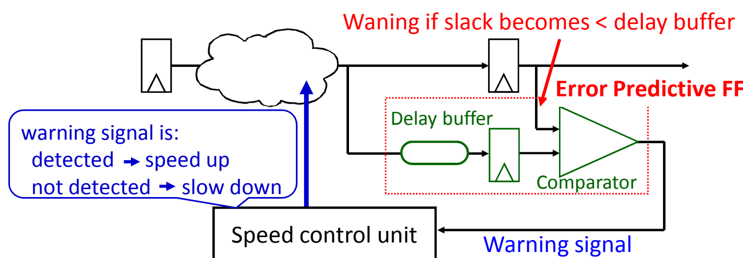

Fig7: Adaptive speed control using timing error predictive flip-flop.

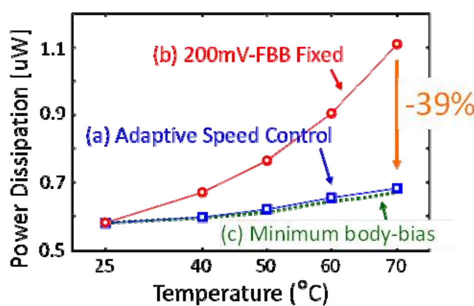

Fig. 8: Measurement result of adaptive speed compensation (65nm, 3MHz, 0.35V).

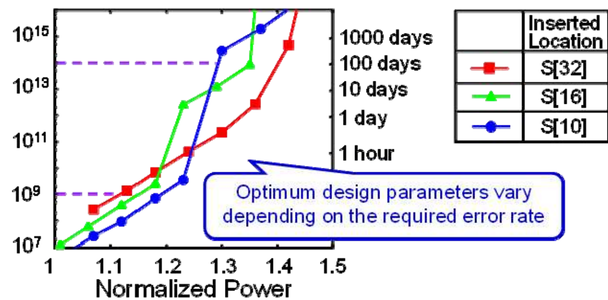

Fig. 9: An evaluation result on relation design parameters, MTBF and power dissipation.

Conclusion

This paper discussed the characteristics and problems of subthreshold circuits, and presented a solution based on adaptive speed control. Application-oriented development is one of future works in addition to improving design methodology.

Acknowledgments

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