Measurement and Analysis of Alpha-Particle-Induced Soft Errors and Multiple-Cell Upsets in 10T Subthreshold SRAM

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***Abstract*—This paper presents measurement results of alpha-particle-induced soft errors and multiple-cell upsets (MCUs) in 65-nm 10T SRAM with a wide range of supply voltage from 1.0 to 0.3 V. We reveal that the soft-error rate (SER) at 0.3 V is six times higher than that at 1.0 V and the MCU rate significantly increases in the subthreshold region. To investigate the reason for the MCU increase, the dependences of the MCU rate on the body-bias voltage and the distance between well ties are examined, and we conclude that the main cause of the MCU increase is not the parasitic bipolar effect but another mechanism, such as charge sharing. In addition, the dependence of the variation in the soft-error immunity of each memory cell on the supply voltage is examined, since SRAMs operating in the subthreshold region are sensitive to manufacturing variability. Measurement results indicate that the number of soft errors in each memory cell varies cell by cell, whereas the cause of the variation is explained by the spatial randomness of alpha-particle hits, and a distinct influence of manufacturing variability is not observed even in the subthreshold region.**

***Index Terms*—Alpha-particle-induced soft error, multiple-cell upset (MCU), soft-error rate (SER), subthreshold circuit.**

I. Introduction

SUBTHRESHOLD circuits can dramatically reduce power dissipation [1], and hence, they are suitable for power-constrained applications, such as sensor-node processors [2], [3] and medical applications [4]. Soft-error immunity of subthreshold circuits, however, has become a concern because the ultra-low voltage operation reduces the energy required to cause upsets [5], [6]. Especially, the soft-error rate (SER) in SRAM, which often characterizes SER of an entire circuit, must be carefully examined before subthreshold circuits are adopted for practical applications.

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According to [7], the neutron-induced SER in SRAM increases by 18% for every 10% reduction in the supply voltage. Tosaka *et al.* have reported a trend in which a decrease in the supply voltage makes the alpha-particle-induced SER dominant in SRAM [8]. However, these measurements were just performed between the nominal supply voltage and 0.8 V. As for soft errors in the subthreshold region, single-event transient (SET) was analyzed with ring oscillators in [5]. Although the critical charge in subthreshold SRAM was analytically modeled in [9], SER was not measured in radiation tests. Neutron-induced SER in subthreshold SRAM was measured in [10]. However, alpha-particle-induced SER in subthreshold region has not been measured.

This work presents measurement results of alpha-particle-induced SER and multiple-cell-upset (MCU) rate in SRAM over a wide range of supply voltages between 1.0 and 0.3 V. Measurement results show that 0.3-V operation increases SER six-fold compared with 1.0 V. The previous work about neutron-induced MCUs [10] indicates that the parasitic bipolar effect is a major mechanism of MCUs in the nominal supply voltage region, while the effect of another mechanism, such as the charge sharing, becomes larger in the subthreshold region. However, the dependence of alpha-particle-induced MCUs on the supply voltage has not been investigated. In this paper, the MCU rate under alpha radiation is measured. Measurement results show that the MCU rate in the nominal supply voltage region is significantly small and it increases below 0.5 V. To investigate the MCU increase, we measure the dependences of the MCU rate on the body-bias voltage and the distance between well ties. We conclude that the main cause of the MCU increase is not the parasitic bipolar effect but another mechanism, such as charge sharing [11], which is the charge diffusion to multiple nodes induced by a single alpha-particle hit. In addition, reducing the supply voltage possibly enlarges the variation in the soft-error immunity of each memory cell, since circuits become more sensitive to manufacturing variability as the supply voltage is reduced. Measurement results show that the number of soft errors in each memory cell varies cell by cell, whereas the cause of the variation is explained by the spatial randomness of alpha-particle hits and an influence of manufacturing variability is not distinguishably observed at both 1.0 and 0.3 V.

The preliminary work of this paper was presented in [12]. The contributions of this paper beyond the preliminary work are

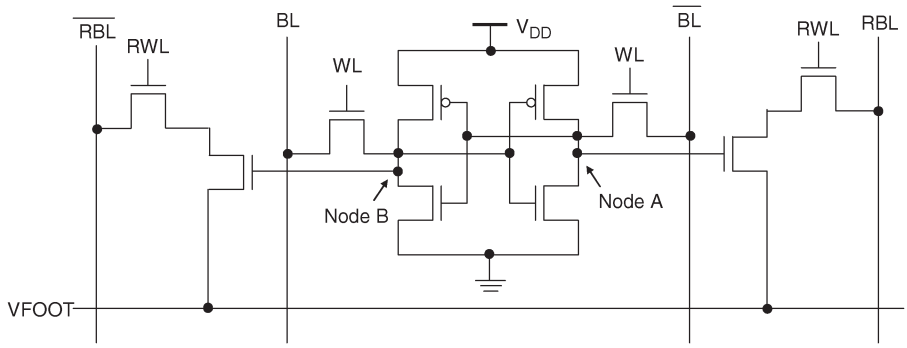


Fig. 1. Structure of 10T memory cell [12].

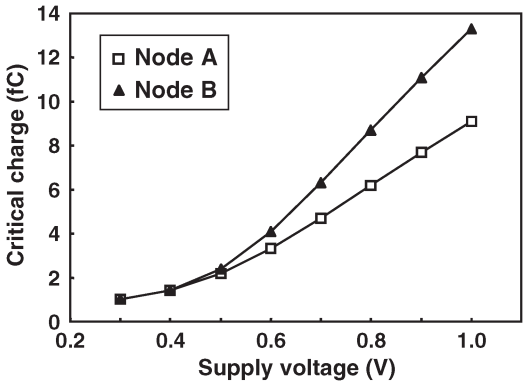


Fig. 2. Simulated critical charge of 10T memory cell [10]. "Node A" and "Node B" represent the critical charges when alpha particles strike Node A and Node B in Fig. 1, respectively.

as follows. 1) For more statistically accurate analysis, a larger SRAM (256 kb) is used than in the preliminary work (2 kb). 2) The dependence of the MCU rate on the distance between well ties is examined in order to investigate the parasitic bipolar effect, which has been considered the major mechanism of neutron-induced MCUs [13]–[16]. 3) The numbers of soft errors in each memory cell at 1.0 and 0.3 V are measured for a long time, and the variation in the soft-error immunity of each memory cell is observed.

The remainder of this paper is organized as follows. Section II describes the structure of the subthreshold SRAM used to measure the SER over a wide range of supply voltages. The measurement results are presented in Section III. Section IV concludes with a summary of the key points.

II. SRAM Structure

To measure the SRAM SER over a wide range of supply voltage, SRAM is required that can operate even in the subthreshold region. However, conventional 6T SRAM, which is used in commercial off-the-shelf SRAMs, can scarcely function in the subthreshold region due to weak writability and read instability [17], [18].

In this paper, 10T memory cell [12] shown in Fig. 1 was used to ensure the correct operation even in the subthreshold region. Fig. 2 illustrates the simulated critical charge of the 10T memory cell. The critical charge decreases as the supply voltage is reduced, and the critical charge at 0.3 V is 92% smaller than that at 1.0 V. This means reducing the supply voltage worsens the soft-error immunity.

Fig. 3 illustrates the circuit structure of the SRAM, which is identical to that used in the previous work for measuring neutron-induced SERs [10]. The circuit consists of an I/O circuit, a control logic, and 16 memory blocks. Each memory block consists of two 8-kb memory cell arrays. No bit-interleaving techniques are used in the memory cell arrays.

The supply voltage of the I/O circuit is set to the nominal supply voltage ("VDDH" in Fig. 3). The control logic, which connects signals between the memory cell arrays and the I/O circuit, operates at the intermediate supply voltage ("VDDM" in Fig. 3). The memory cell arrays operate over a wide range of supply voltages, from 0.3 to 1.0 V ("VDDL" in Fig. 3). For example, when VDDL was 0.3 V, VDDM and VDDH were set to 0.6 and 1.2 V, respectively.

The word lines (WLs) are driven at a higher voltage ("VWRITE" in Fig. 3) than the supply voltage of the memory cell arrays in order to attain strong writability, which is similar to the "boosted word line" technique [19], [20]. In this paper, VWRITE was consistently set to VDDL + 0.1 V. VFOOT (Fig. 1) is used to ensure correct read operation in the subthreshold region [19]. The VFOOT of the accessed word is set to low and those of the unaccessed words remain high.

Furthermore, to investigate how the parasitic bipolar effect contributes to the occurrence of MCUs, we implemented two types of memory cell arrays, as shown in Fig. 3. The distance between the well ties of the left memory cell arrays is wide (25.6 μm), while that of the right memory cell arrays is narrow (6.4 μm). Each memory array is 8 kb.

A 256-kb 10T SRAM was fabricated in a 65-nm CMOS process with a triple-well structure. The chip micrograph is shown in Fig. 4.

III. Experimental Results

A. Measurement Setup

We used an Am-241 foil, whose flux is 9×10^9 cm^{-2} h^{-1}, as an alpha particle source. The main peak energy of the alpha particle is 5.49 MeV. The linear energy transfer (LET) is 0.58 MeV $\cdot$ cm^2/mg, which is calculated by SRIM [21]. The foil was placed immediately above the die in accordance with JEDEC standards [22].

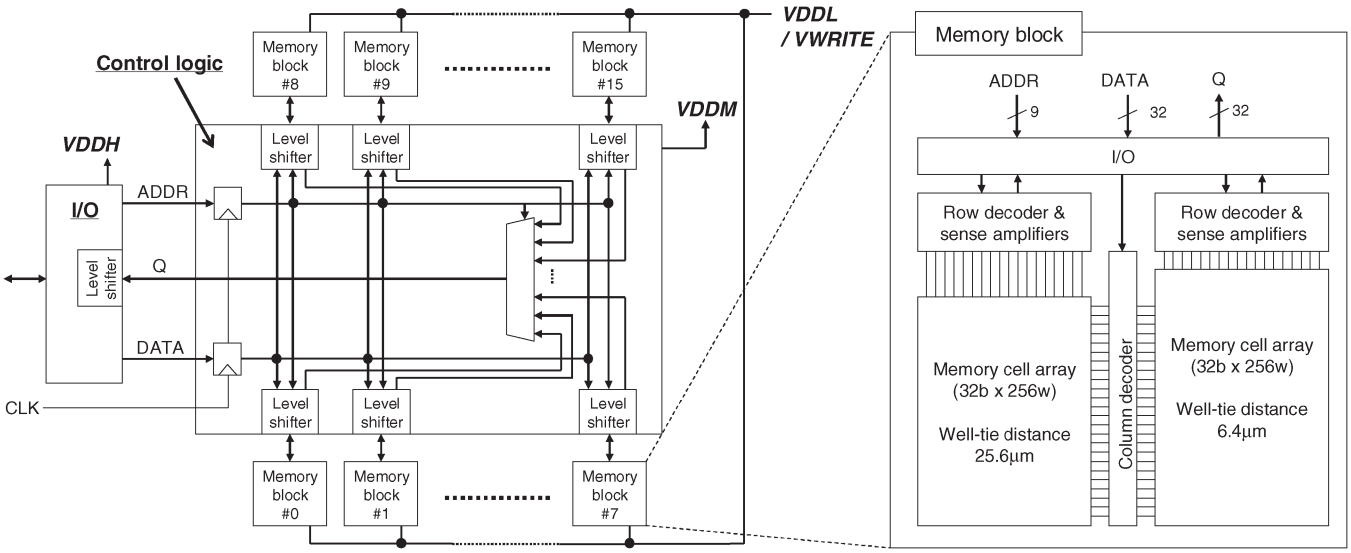


Fig. 3. Circuit structure of the test chip [10]. Two types of memory cell arrays are implemented; the distance between the well ties of the left memory cell arrays is wide (25.6 μm) and that of the right memory cell arrays is narrow (6.4 μm).

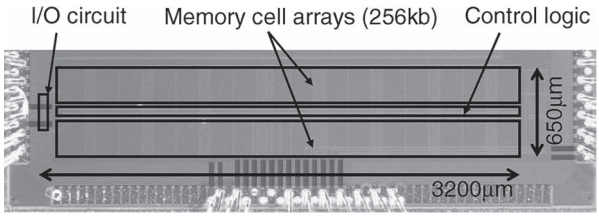


Fig. 4. Micrograph of test chip.

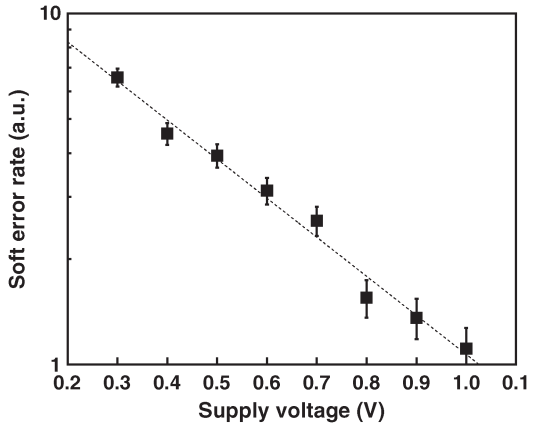


Fig. 5. SERs as a function of the supply voltage of the memory cell array. The Y-axis is shown in log scale. Each error bar indicates $\pm 3\sigma$, where σ is defined as the square root of the number of the observed upsets. The dotted line represents the fitted curve by exponential approximation.

B. Soft-Error Rate and Multiple-Cell Upset

Fig. 5 shows the measured SERs as a function of the supply voltage of the memory cell array. SER has an exponential dependence on the supply voltage, and SER at 0.3 V is six times higher than that at 1.0 V.

Next, the MCU rate is measured. As shown in Fig. 6, this paper defines the following two types of MCUs; 1) intra-word upset, which is a multiple upset occurring at adjacent cells in the same word, and 2) inter-word upset, which is a multiple upset occurring at adjacent cells in a different word. In this paper,

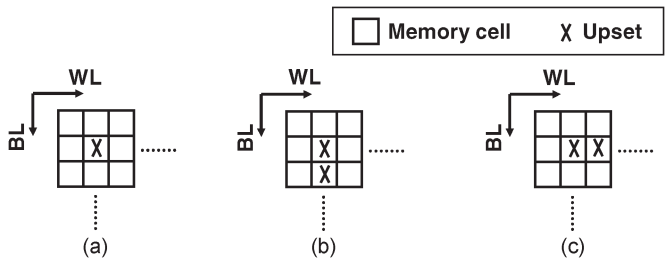


Fig. 6. Definition of MCU. (a) SBU. (b) Inter-word MCU. (c) Intra-word MCU.

only a multiple upset occurring at adjacent cells is defined as MCU.

As explained in Fig. 7, the occurrence of multiple upsets in adjacent bits depends on the written data pattern [13]. In our memory cell layout, the intra-word upsets might occur in data patterns "01" and "10," since the sensitive nodes of the adjacent cells are on the same well in these data patterns. Therefore, we periodically wrote the data pattern "1010$\cdots$" to all words and checked whether each bit was flipped or not.

Fig. 8 depicts the measured dependence of the intra-word and inter-word MCUs on the supply voltage. The MCU rate was derived by dividing the number of failing events (for example, a "2-bit MCU" was considered to be one event) by the measurement period. In subthreshold operation, the access time to SRAM is significantly large. In our measurement setup, one read operation of all memory cells takes four seconds to complete, and consequently data obtained by the read operation contains many upsets. In this case, multiple errors originating from different particles are possibly misjudged as an MCU. To remove such misjudgments statistically, the expected occurrence rates of such "pseudo" MCUs are calculated and compared with the measured MCU rates as shown in Fig. 8. The pseudo MCU rates are obtained by Monte Carlo simulations. The detailed procedure of the simulations will be explained in Section III-D. The simulations performed in this section assume that the occurrence probability of errors in each memory cell is

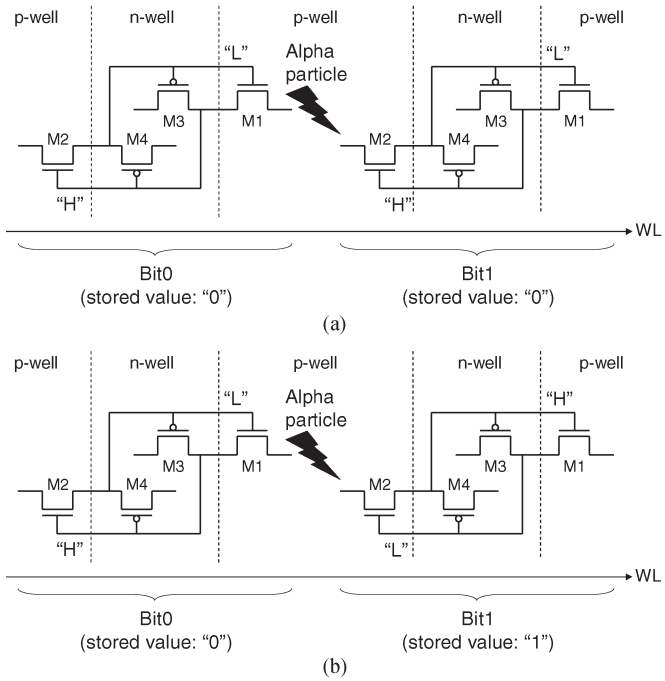


Fig. 7. Occurrence of multiple upsets in adjacent bits depends on the written data pattern [13]. Only cross-coupled inverters (M1–4 in Fig. 1) are illustrated in this figure. In our memory cell layout, intra-word upsets might occur in data pattern "01" and "10," and do not occur in "00" and "11." (a) Intra-word upsets do not occur. (b) Intra-word upsets might occur.

identical. This assumption will be experimentally validated in Section III-D.

Fig. 8 indicates that when the supply voltage is from 1.0 to 0.6 V, there is no significant difference between the measured and the pseudo inter-word MCU rates, while the measured inter-word MCU rates below 0.5 V obviously differ from the expected pseudo MCU rates. This indicates that the MCU rates in the nominal supply voltage region is significantly small, whereas the inter-word MCUs sharply increase in the subthreshold region. The reason of such increase will be discussed in Section III-C. Furthermore, as the supply voltage is reduced, the single-bit upset (SBU) rate increases more dramatically than the MCU rate for neutron-induced soft errors due to secondary particles produced by the nuclear reaction between neutrons and Si [10], whereas the MCU rate significantly increases for alpha-particle-induced soft errors.

For comparison, Fig. 9 shows the dependence of the intra-word and inter-word MCU rates on the written data patterns of "00$\cdots$" and "11$\cdots$" in addition to "01$\cdots$" at 0.3 and 1.0 V. Significant differences among the data patterns are not observed.

We here discuss the reason the MCUs only arose in inter-word adjacent bits in subthreshold operation as shown in Fig. 8. Fig. 10 illustrates the layout of the memory cell array. The drains of P/NMOSs in the cross-coupled inverter pair are sensitive to alpha particles. The distance between sensitive nodes for the inter-word MCUs is 0.8 μm for all data patterns. The distance between sensitive nodes for the intra-word MCUs is 8.8 μm for "00" and "11" data patterns, and it is 4.4 μm for "01" and "10" data patterns. This indicates that the distance between the sensitive nodes of the adjacent rows is 1/5 shorter

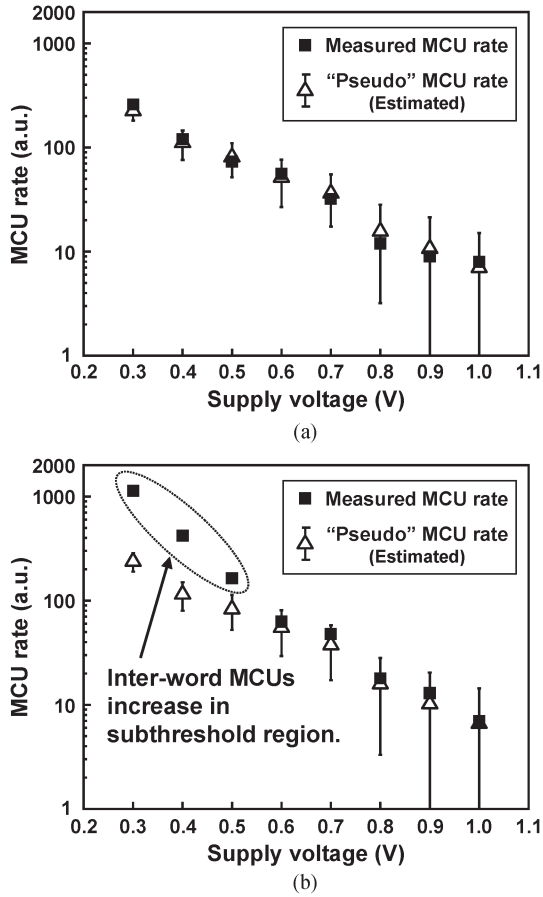


Fig. 8. Measured dependence of the intra-word and inter-word MCU rates on the supply voltage. The expected occurrence rates of "pseudo" MCUs are also shown. The "pseudo" MCU is defined as multiple errors misjudged as an MCU. Each error bar indicates $\pm\sigma$. (a) $V_{\rm DD}$ dependence of intra-word MCU rate. (b) $V_{\rm DD}$ dependence of inter-word MCU rate.

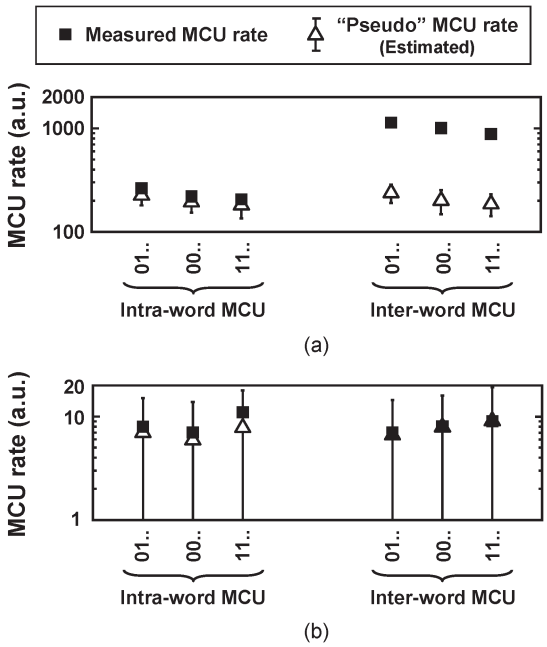


Fig. 9. Measured dependence of the intra-word and inter-word MCU rates on the written data patterns of "01," "00," and "11" when the supply voltages are 0.3 and 1.0 V. Each error bar indicates $\pm\sigma$. (a) $\rm V_{DD} = 0.3$ V. (b) $\rm V_{DD} = 1.0$ V.

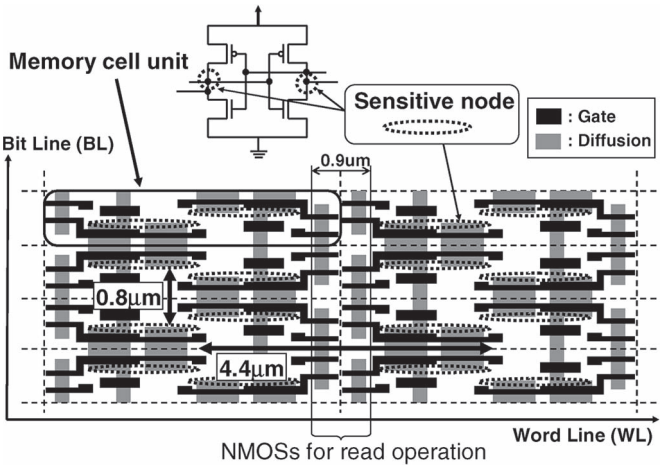


Fig. 10. Layout of the memory cell array. The dotted ellipses indicate sensitive nodes for alpha particles. The NMOSs for the read operation (M7–10 in Fig. 1) are located between the adjacent columns.

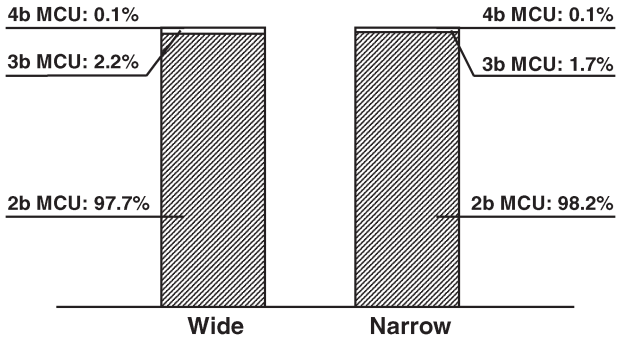


Fig. 11. Measured MCU distribution at $V_{\mathrm{DD}} = 300$ mV.

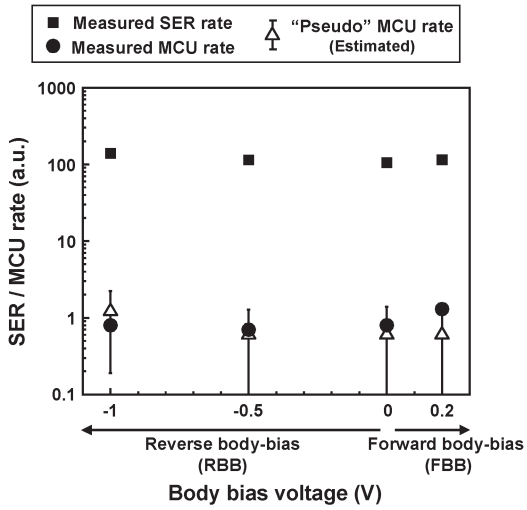
for "01" and "10" data patterns and 1/10 shorter for "00" and "11" data patterns than that of the adjacent columns. Furthermore, the NMOSs for the read operation (M7–10 in Fig. 1) are located between the adjacent columns, which makes horizontally-adjacent cells distant. Thus, the inter-word MCUs are more likely to upset.

As for the intra-word MCUs, the distance between sensitive nodes for "01" and "10" data patterns is shorter than that for "00" and "11" data patterns. On the other hand, the MCU rate for "01" and "10" data patterns is sufficiently small and we cannot observe a clear dependence of the MCU rate on the data patterns as shown in Fig. 9. As will be explained in Section III-C, the main cause of the MCU is charge sharing. According to [23], charge sharing strongly depends on the distance between devices, and its dependence is nonlinear. Therefore, the difference between the data patterns is less influential on the intra-word MCU rate.

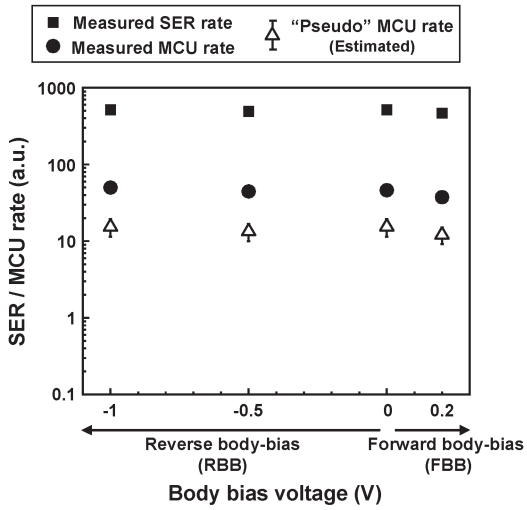
Finally, Fig. 11 shows the measured MCU distribution at $V_{\mathrm{DD}} = 300$ mV. Compared with the MCU distribution induced by neutron [10], the number of bits of alpha-particle-induced-MCUs is smaller, and 98% of them are 2-bit MCUs.

C. Discussion on MCU Increase in the Subthreshold Region

According to previous researches [13]–[16], the neutron-induced MCUs are mainly caused by the parasitic bipolar



(a)



(b)

Fig. 12. Measured dependences of the SER and inter-word MCU rate on the body-bias voltage. The expected occurrence rates of "pseudo" MCUs are also shown. Each error bar indicates $\pm\sigma$. (a) $V_{\mathrm{DD}} = 1.0$ V. (b) $V_{\mathrm{DD}} = 0.4$ V.

effect. This section investigates the reason the alpha-particle-induced MCUs increase below 0.5V, as shown in Fig. 8(b).

First, we measured the dependences of the SER and inter-word MCU rate on the body-bias voltage at $V_{\mathrm{DD}} = 1.0$ and 0.4 V. Fig. 12 shows the measurement results. Nakauchi *et al.* reported that the reverse body-bias (RBB) can reduce the MCU rate if the MCUs are induced by the parasitic bipolar effect [13]. Fig. 12 indicates, however, the RBB does not reduce the MCU rate.

Next, we examined the dependence of the MCU rates on the distance between well ties. The measured dependence is shown in Fig. 13. As explained in [10], the MCU rates depend on the distance between well ties if the MCUs are caused by the parasitic bipolar effect. The MCU rates shown in Fig. 13, however, barely depend on the distance.

From the results shown in Figs. 12 and 13, we conclude that the main cause of the MCU increase is not the parasitic bipolar effect but another mechanism, such as charge sharing [11]. In Fig. 8(b), the MCU rate increases as the supply voltage

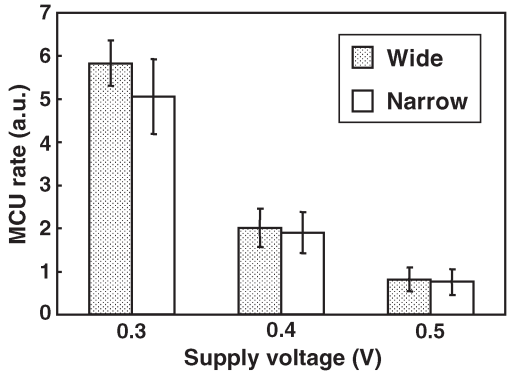


Fig. 13. Measured $V_{\rm DD}$ dependences of MCU rates on distance between well ties. Each error bar indicates $\pm 3\sigma$.

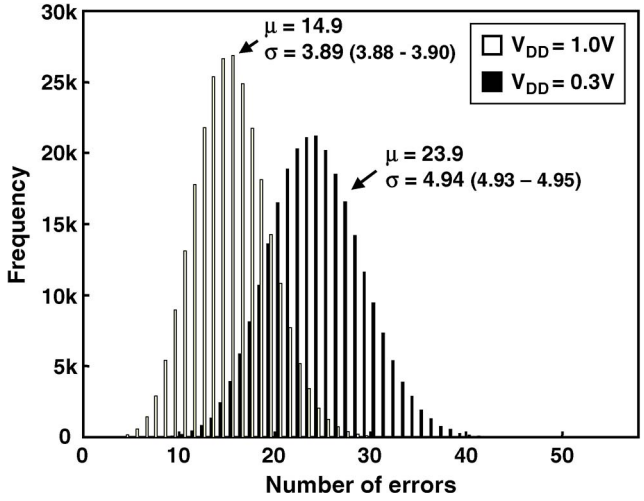


Fig. 14. Measured distributions of the number of soft errors in each memory cell in a single chip at 1.0 and 0.3 V. μ and σ denote the mean and standard deviation of the distribution, respectively. The values in parentheses represent the 95% confidence interval of the standard deviation.

decreases in subthreshold region, since the decrease in the supply voltage reduces the critical charge as shown in Fig. 2.

D. Variation in Soft-Error Immunity

As the supply voltage is reduced, the SRAM becomes more sensitive to manufacturing variability. In this section, we investigate the variation in the soft-error immunity of each memory cell by measuring the number of soft errors in each memory cell for a long time when the supply voltage is 1.0 and 0.3 V. In this measurement, we periodically wrote the data patterns "$00\cdots$" and "$11\cdots$" to all words and checked whether each bit was flipped or not. The total number of the measured errors was 4M for 1.0 V and 6M for 0.3 V, respectively. Fig. 14 shows the distributions of the number of soft errors in each memory cell in a single chip.

As indicated in Fig. 14, the number of errors varies cell by cell. To investigate the cause of the variation, we conducted a Monte Carlo simulation with the following procedure:

I) Let P_i be the occurrence probability of errors in the i th memory cell $(0 \leq i \leq 256$ k). P_i is possibly fluctuated due to manufacturing variability, and we here assume that the occurrence probability of errors $P = \{P_0 P_1 \cdots P_{256k}\}$ obeys the Gaussian distribution $N(0.5, \sigma_P^2)$.

II) An integer number n and a real number p are randomly generated. n and p satisfy $0 \leq n \leq 256$ k and $0 \leq p < 1$, respectively.

III) If p is less than $P_n (p < P_n)$, we consider that an upset occurs in the nth memory cell.

IV) Steps ii) and iii) are repeated. Consequently, the distribution of the number of errors in each memory cell is obtained.

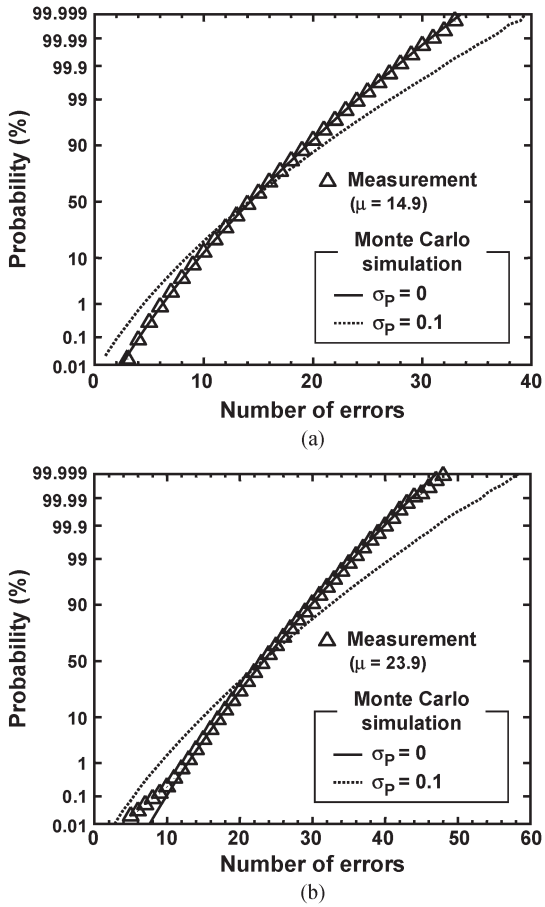


Fig. 15. Cumulative probability plots of the measured distributions of the number of soft errors in each memory cell shown in Fig. 14. μ is the mean of the measured distribution. σ_P represents the standard deviation of the variation in the occurrence probability of errors. (a) $V_{\rm DD} = 1.0$ V. (b) $V_{\rm DD} = 0.3$ V.

Fig. 15 shows the cumulative probability plots of the distributions of the number of soft errors in each memory cell when the supply voltage is 1.0 and 0.3 V. The open triangles in Fig. 15 denote the measured distribution shown in Fig. 14. The solid and dotted lines represent the distributions obtained by the aforementioned Monte Carlo simulation when the standard deviation of the occurrence probability of errors σ_P is 0 and 0.1, respectively.

If the variation in the number of errors is caused only by the spatial randomness of particle hits, the occurrence probability of errors in each memory cell is identical $(\sigma_P = 0)$. In this case, the distribution obeys the Poisson distribution [12]. Fig. 15 indicates that the measured distribution of the number of errors

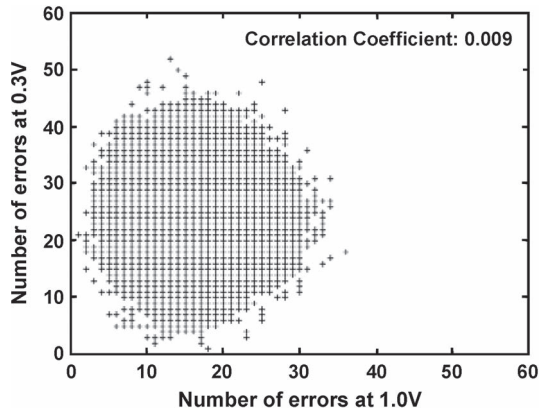


Fig. 16. Measured correlation between the numbers of soft errors in each memory cell in a single chip at 1.0 and 0.3 V shown in Fig. 14.

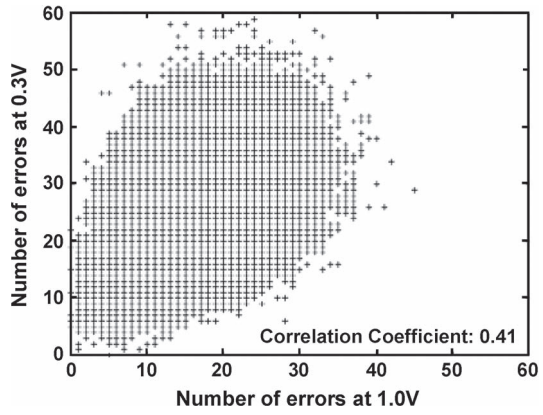


Fig. 17. Simulated correlation between the numbers of soft errors in each memory cell assuming that the occurrence probability is fluctuated due to manufacturing variability ($\sigma_P = 0.1$) and the probabilities at 1.0 and 0.3 V are identical.

is almost equivalent to the distribution obtained by the simulation with $\sigma_P = 0$ (Poisson distribution) both at $V_{\rm DD} = 1.0$ and 0.3 V. This means that the cause of the variation shown in Fig. 14 is explained by the spatial randomness of particle hits, and an influence of manufacturing variability is not distinguishably observed even at 0.3 V.

Finally, Fig. 16 depicts the measured correlation between the numbers of soft errors in each memory cell at 1.0 and 0.3 V shown in Fig. 14. Fig. 17 shows that the correlation obtained by the aforementioned Mote Carlo simulation assuming that the occurrence probability of errors in each memory cell fluctuates due to manufacturing variability and the probabilities at 1.0 and 0.3 V are identical. As shown in Fig. 17, if the occurrence probability correlates between 1.0 and 0.3 V, the number of errors also correlates. Fig. 16 indicates, however, that the correlation is not measured, which supports the conclusion that the variation shown in Fig. 14 is mainly caused by the spatial randomness of particle hits.

IV. Conclusion

In this paper, we presented alpha-particle-induced SERs and MCUs in the subthreshold region of a designed 10T SRAM in a 65-nm CMOS process. The measurement results showed that the SER increases as the supply voltage is reduced and the SER at 0.3 V is six times higher than the SER at 1.0 V. The MCU rate was also investigated in this paper. The previous work about neutron-induced MCUs indicates that the parasitic bipolar effect is a major mechanism of MCUs in the nominal supply voltage region, while the effect of another mechanism, such as the charge sharing, becomes larger in the subthreshold region. In this paper, alpha-particle-induced MCUs were measured. Measurement results showed that the MCU rate is significantly small in the nominal supply voltage region, while it increases in the subthreshold region. To find the reason for this, the dependences of the MCU rate on the body-bias voltage and the distance between well ties were examined. Measurement results indicated that the main cause of the MCU increase is not the parasitic bipolar effect but another mechanism, such as charge sharing. In addition, as the supply voltage is reduced, the SBU rate increases more rapidly than the MCU rate for neutron-induced soft errors, while the MCU rate significantly increases for alpha-particle-induced soft errors. Furthermore, we investigated the dependence of the variation in the soft-error immunity of each memory cell on the supply voltage because subthreshold circuits are sensitive to manufacturing variability. Results revealed that the number of soft errors in each memory cell varies cell by cell, whereas the cause of the variation was well explained by the spatial randomness of particle hits and an influence of manufacturing variability was not recognizably observed even in the subthreshold region.

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