2013 IEEE 27th International Symposium on Parallel & Distributed Processing Workshops and PhD Forum

Real-time Supply Voltage Sensor for Detecting/Debugging Electrical Timing Failures

Miho Ueno, Masanori Hashimoto, and Takao Onoye
Dept. Information Systems Engineering, Osaka University
{*ueno.miho, hasimoto, onoye*}*@ist.osaka-u.ac.jp*

***Abstract*—Debugging electrical timing bugs consumes a significant portion of validation efforts. The main cause of this problem is that electrical bugs appear as one-cycle bit-flips under only a certain operating condition such as voltage, temperature and frequency. In addition, run-time detection of a suspicious electrical bug is drawing attention for enabling voltage over-scaling and/or ensuring reliable operations. In this work, we focus on power supply noise as a primary cause of electrical bugs and propose a supply voltage sensor which achieves one-shot and every-cycle sensing. The proposed sensor can provide cycle-accurate voltage variation for detecting and debugging electrical bugs. The performance of the sensor is evaluated on an FPGA, and the measured voltage resolution is 29mV. An observed correlation between sensing results and a processor failure suggests the utility of the proposed sensor for debugging.**

***Keywords*-supply noise sensor, timing failure, electrical bug, time-to-digital converter, post-silicon debug, post-silicon validation**

I. Introduction

In the past decades, the integration density of integrated circuits (ICs) has grown exponentially, which brings amazing performance improvement and explodes IC usages. Microprocessors, which have good programmability, are used for various applications, but in some cases, the power consumption is too high or the computational performance is not high enough. In such situations, application-specific integrated circuits (ASICs) have been developed and used for particular applications. However, Non-Recurring Expense (NRE) costs including design and mask costs are increasing as technology advances, and now a small-quantity production cannot afford to pay the NRE costs. Due to this tendency, FPGAs, which have both high programmability and cost efficiency for a small-quantity production, are expected to be used not only for prototype implementation and low-performance products but also high-end products that require high clock frequency operation.

In pursuing the performance of a circuit implemented on an FPGA, the design margin should be minimized to exploit the inherent performance of FPGA devices. However, in such a situation, electrical timing failures sometimes happen. Once an electrical timing failure appears, time-consuming hardware debugging and validation must be carried out. Here, an electrical timing failure is a bug that arises even though the circuit is logically correct, and it is infrequently caused by dynamic events such as fluctuation of supply voltage and temperature. The electrical failure arises as a bit flip in a certain cycle, and is likely to appear in paths with small timing slacks. However, it arises only under a certain situation and its reproduction is difficult. Therefore, it is hard to debug the electrical timing failure.

There are many works that equip a sensor on a chip and use sensing results for run-time performance guarantees [7]–[10]. For power integrity verification, there are many proposals of on-chip noise sensors used for power grid analysis [1]–[4] and correlation analysis with timing failures [11]. On the other hand, for FPGAs, temperature is often measured by measuring ring oscillator frequency (such as [12]). The ring oscillator frequency also includes supply voltage information [13]. However, the ring oscillator tells us the average voltage while it is running, and cannot snap short-time voltage drops that cause electrical timing failures. Improved ring oscillator based sensors have been proposed in [5], [6]. However, they require repetitive noise production since they work as a sampling oscilloscope, and hence they cannot be used for detecting one-short voltage drops. Thus, a sensor which can sense voltage fluctuation every cycle and can be integrated on FPGAs is highly demanded to obtain helpful information for the debug of the electrical timing failure. In addition, such a sensor is also useful for detecting a suspicious operation and re-executing the operation similarly to [10].

This work proposes a real-time supply voltage sensor which can be easily implemented on ASICs and FPGAs and measure supply voltage fluctuation at every cycle. The proposed sensor can detect short-time one-shot voltage drops resulting in electrical timing failures. The proposed sensor is integrated on an FPGA and its performance and utility for debugging are experimentally demonstrated.

The rest of this paper is organized as follows. Section 2 describes structure and operation of the proposed sensor and analytically discusses the sensor resolution. Section 3 presents measurement results of the sensor. Concluding remarks are given in Section 4.

II. Real-time Supply Voltage Sensor

A. Sensor Structure and Operation

An electrical timing failure caused by environmental fluctuation, such as supply voltage drops, arise as a bit flip at a certain cycle. In order to investigate the correlation between environmental fluctuation and timing failures, a

978-0-7695-4979-8/13 $26.00 © 2013 IEEE
DOI 10.1109/IPDPSW.2013.126

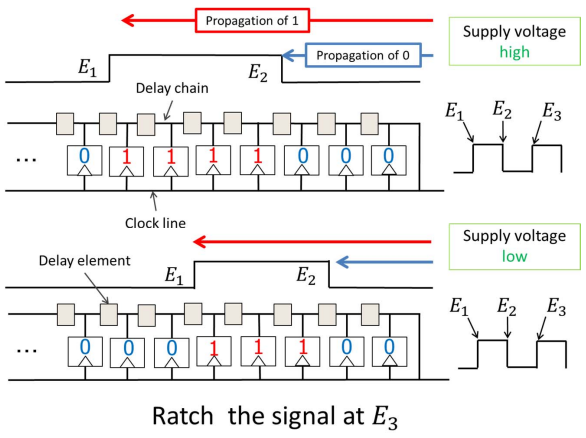

Figure 1. Proposed real-time supply voltage sensor and its operation.

supply voltage sensor that can measure cycle-by-cycle supply voltage fluctuation is required. In addition, the output of the supply voltage sensor can be used as a trigger signal to stop logging internal operations into trace buffer [14], or a retry signal suggesting a suspicious operation to re-execute [10]. Thus, the sensor is useful for debugging timing failures in silicon validation and detecting potential timing failures in concurrent error checking.

Figure 1 shows the proposed real-time (cycle-by-cycle) supply voltage sensor consisting of a delay chain and a time-to-digital converter (TDC). Flip-flops (FFs) in the TDC are connected in parallel. A clock signal that comes from a PLL is guided to the delay chain and the clock line. The output at each stage of the delay chain is connected to D terminal of an FF. The voltage sensing is performed as follows:

1) The first positive edge (E1) is given to the clock line and the delay chain. The edge propagates through the delay chain.
2) Subsequently, the negative edge (E2) is given and it propagates through the delay chain in the same way as E1.
3) When the next positive edge (E3) is delivered to CLK terminal of FFs, the stage outputs of the delay chain are latched into the FFs.

N_{passed}, which is defined as the number of FFs which E1 passed through, depends on the supply voltage because the propagation delay of each delay element in the delay chain is dependent on the supply voltage. When the supply voltage is high, N_{passed} increases due to the decrease in the propagation delay (Upper case in Figure 1). On the other hand, N_{passed} decreases when the supply voltage is low (Lower case in Figure 1). Therefore, N_{passed} includes the supply voltage information. We prepare a table describing a relation between N_{passed} and the supply voltage beforehand. In the sensing, N_{passed} measured at each clock cycle is converted into the supply voltage by looking up the table.

A feature of this sensor is that it senses the supply voltage at every cycle by only a single sensor. In this sensor, the clock signal is given to the delay line and latched in FFs, which makes it unnecessary to reset the latched value. Therefore, the proposed sensor can measure the voltage at every cycle.

Moreover, measuring N_{passed} has another good aspect. N_{passed} is determined by the average supply voltage in the duration when the edge of interest is propagating, and the duration is equal to the clock cycle. Therefore, N_{passed} means the average supply voltage within a clock cycle. On the other hand, the path delays of speed liming paths are close to the cycle time, and hence they are correlated with the average supply voltage. Thus, measuring N_{passed} is well suited to the purpose of detecting and debugging setup timing failures.

B. Voltage Resolution

Let us analytically discuss the performance of the proposed sensor, i.e. the voltage resolution. Here, the voltage resolution is defined as the voltage variation that is needed to increment N_{passed} from *n* to *n+1*. First, suppose N_{passed} = *n* under the following condition:

- Clock cycle time is *T*.
- Supply voltage is V_{dd}.

This situation can be expressed as below.

$$n = \lfloor \frac{T}{d} \rfloor = \lfloor \frac{T(V_{dd} - V_{th})^{\alpha}}{\beta} \rfloor, \tag{1}$$

where d is the propagation delay of a delay element, and it is approximately expressed as $d = \frac{(V_{dd} - V_{th})^{\alpha}}{\beta}$ CMOS gate delay [15]. V_{th} is threshold voltage of MOSFETs, and α and β are coefficients found in [15]. Equation (1) can be expressed as an inequality below.

$$n \leq \frac{T(V_{dd} - V_{th})^{\alpha}}{\beta} < n + 1. \tag{2}$$

By multiplying -1, the inequality becomes

$$-(n+1) < -\frac{T(V_{dd} - V_{th})^{\alpha}}{\beta} \leq -n. \tag{3}$$

We next suppose that N_{passed} become *n+1* due to a small voltage increase by Δ.

$$n + 1 = \lfloor \frac{T(V_{dd} + \Delta - V_{th})^{\alpha}}{\beta} \rfloor \tag{4}$$

$$n + 1 \leq \frac{T(V_{dd} + \Delta - V_{th})^{\alpha}}{\beta} < n + 2 \tag{5}$$

By adding Equations (3) and (5), we obtain an inequality below.

$$0 < \frac{T(V_{dd} + \Delta - V_{th})^{\alpha}}{\beta} - \frac{T(V_{dd} - V_{th})^{\alpha}}{\beta} < 2. \tag{6}$$

Equation (6) is transformed in terms of Δ.

$$(V_{dd}-V_{th})^{\alpha} < (V_{dd}+\Delta-V_{th})^{\alpha} < (V_{dd}-V_{th})^{\alpha}+\frac{2\beta}{T} \quad (7)$$

$$V_{dd}-V_{th} < V_{dd}+\Delta-V_{th} < \{(V_{dd}-V_{th})^{\alpha}+\frac{2\beta}{T}\}^{\frac{1}{\alpha}} \quad (8)$$

$$0 < \Delta < \{(V_{dd}-V_{th})^{\alpha}+\frac{2\beta}{T}\}^{\frac{1}{\alpha}}-(V_{dd}-V_{th}) \quad (9)$$

The right term of Equation (9) represents the voltage resolution of the proposed sensor. This expression indicates that the voltage resolution is less dependent on V_{dd} and V_{th} and it is mostly determined by β and T, where β is the technology and transistor specific parameter. This means that the proposed sensor is expected to have a good linearlity. Besides, we can see that the resolution becomes finer as T becomes large. This is because larger T corresponds to larger N_{passed} and the accumulated delay decrease in N_{passed} elements is easier to exceed the delay of a delay element. This analytic estimate of the voltage resolution is compared with measurement results in the next section.

III. Measurement Results

A. Voltage Resolution of Supply Voltage Sensor

We implemented the proposed supply voltage sensor on an FPGA and evaluated the voltage resolution. We used a custom Stratix Ⅲ device board as a DUT (device under test) board, which is shown in Fig. 2. The supply voltage given to the DUT board can be changed externally. On the DUT board, an A/D converter is integrated to measure the supply voltage outside the FPGA. The implemented supply voltage sensor consists of 256 FFs [1]. As for the delay elements, we did not insert additional elements intentionally, since switches and buffers are inserted unintentionally and behave as delay elements due to inherent FPGA structure. These FFs are placed manually to make the layout regular. A clock signal of 139.7 MHz is given.

To evaluate the voltage resolution, we derived the relation between N_{passed} and supply voltage. We varied the supply voltage from 0.9V to 1.4V by 10mV. Figure 3 shows the measurement results, and a linear fitting is also plotted with a dotted line. The voltage resolution of the proposed supply voltage sensor, which corresponds to the slope of the fitted line, is 29 mV. For an approximate measurement, this resolution can be used instead of the look-up table.

To validate the measurement result, we calculated the analytic estimates given in Equation (9). We supposed α = 1 and V_{th} = 0.2, where they are not disclosed by FPGA vendor. As for β, we estimated β = 1.5 10^{-10} from a measurement result. Another unknown factor in FPGA is the latency between the clock signal given to FFs and that given to the delay chain. We assumed that this latency was $0.3T$. While there are unknown factors in FPGA implementation,

[1]For experiments in this paper, 50 FFs are enough, though.

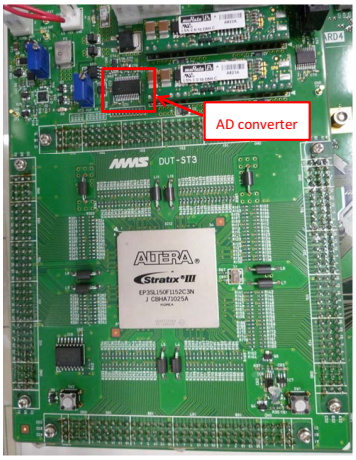

Figure 2. DUT board with Stratix Ⅲ FPGA.

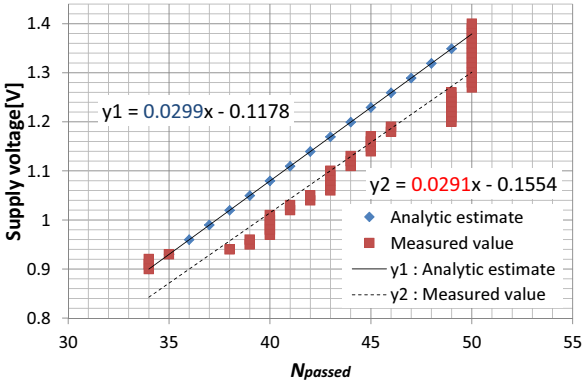

Figure 3. Measured values and analytic estimates of proposed sensor.

the analytic estimates are correlated with the measurement results. The stronger non-linearlity found in the measurement results might come from the assumed delay expression for CMOS gates, since it is not tailored for switches. Further analysis for SoC implementation, in which more information is available for the analysis, is one of our future works. On the other hand, it should be noted that such unknown factors are necessary to discuss the performance analytically, but the usage of the proposed sensor itself does not need such information, since a pre-characterized table between N_{passed} and the voltage gives all the necessary information for voltage sensing.

B. Voltage Measurement with Processor

We applied the proposed supply voltage sensor to sense the voltage fluctuation in a processor running, and compared the measurement result of the proposed sensor with that of A/D converter on the DUT board (Fig. 2). For this experiment, we used MIPS R3000 processor, which has five pipeline stage (instruction fetch stage, instruction decode

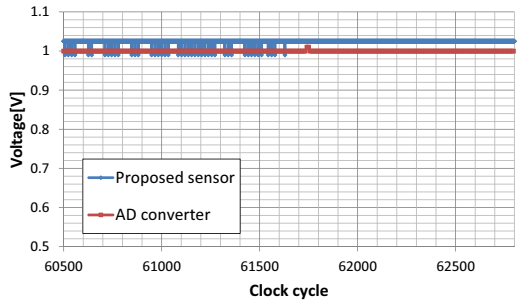

Figure 4. Measured supply voltage fluctuation without intentional noise.

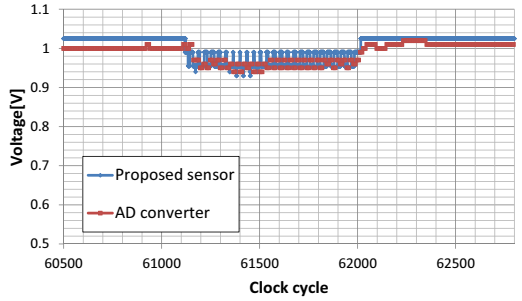

Figure 5. Measured supply voltage fluctuation with intentional noise.

stage, execution stage, memory stage and write back stage) and the same sensor in the previous subsection. CRC32 program was executed on the processor. Given 1.0V as an external supply voltage and 139.7 MHz as a clock frequency, the voltage sensing result of Fig. 4 was obtained.

We next added a noise generator into the FPGA to intentionally fluctuate power supply voltage. The noise generator consists of 40,000 FFs. All the FFs are connected in series like a shift register and an inverter is inserted between every two FFs. With this structure, by inputting many 0/1 transitions into the noise generator, this noise generator consumes large power and generates larger noise.

We measured the supply voltage in the same condition with the previous experiment except for exercising the noise generator. The noise was injected between 61118 and 61991 cycle as shown in Fig. 5. We can see that the proposed sensor captures this intentional noise well. This kind of one-shot noise is often found in mode transitions such as between sleep and active modes, and the proposed sensor is helpful to analyze such noise behaviors.

Moreover, when the intentional noise was injected, the computation result of the processor was wrong. This means that the noise made an electrical bug while the program running For debugging, it is very important to know when the electrical bug occurred, and the proposed sensor gives hints on suspicious cycles having unexpectedly large noises. In this example, the bug occurred between 61468 and 61485 cycle, and in this duration, *Branch Not Equal* (BNE) instruction was executed. In fact, TimeQuest Timing Analyzer, which is the tool for timing analysis in QuartusI I software, reported that the a path activated by the BNE instruction is included in the longest paths. While this is a simple and illustrative example, the information provided by the proposed sensor is helpful for localizing debugging electrical bugs. Our future works include the integration of the proposed sensor into the on-chip debugging structure such as IFRA [16] or on-chip logic analyzer.

IV. Conclusion

In this work, we proposed a real-time supply voltage sensor composed of delay elements and FFs. The proposed sensor implemented on an FPGA attained a resolution of about 29 mV and successfully sensed voltage fluctuation. A test case of MIPS R3000 exemplified that the measured supply voltage helps localize and debug electrical bugs.

Acknowledgment

This work was partly supported by NEDO.

References

[1] R.Petersen, P. Pant, P. Lopez, A Barton, J. Ignowski, and D. Josephson, gVoltage transient detection and induction for debug and test,h in *ITC*, pp.1–10, Nov. 2009.

[2] E. Alon, V. Stojanovic, and M.A. Horowitz, gCircuits and techniques for high-resolution measurement of on-chip power supply noise,h *IEEE Journal of Solid-State Circuits*, pp.820–828, vol. 40. no.4. Apr. 2005.

[3] Y. Takai, M. Hashimoto, and T. Onoye, gEvaluation of power gating structures focusing on power supply noise with measurement and simulation,h in *Proc. EPEPS*, pp.213–216, Oct. 2010.

[4] A. Muhtaroglu, G. Taylor, and T. Rahal-Arabi, gOn-die droop detector for analog sensing of power supply noise,h *JSSC*, vol 39, no. 4, pp. 651–660, Apr. 2004.

[5] Y. Ogasahara, M. Hashimoto, and T. Onoye, gAll-Digital Ring-Oscillator-Based Macro for Sensing Dynamic Supply Noise Waveform,h *IEEE J. Solid-State Circuits*, pp.1745–1755, vol.44, no.6, Jun. 2009.

[6] T. Sato, Y. Matsumoto, K. Hirakimoto, M. Komoda, and J. Mano, gA time-slicing ring oscillator for capturing instantaneous delay degradation and power supply voltage drop,h in*CICC*, pp. 563–566, Sep. 2006.

[7] S. Das, D. Roberts, S. Lee, S. Pant, D. Blaauw, T. Austin, K. Flautner, and T. Mudge, gA self-tuning DVS processor using delay-error detection and correction,h *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp.792–804, Apr. 2006.

[8] S. Das, C. Tokunaga, S. Pant, W. H. Ma, S. Kalaiselvan, K. Lai, D. M. Bull, and D. Blaauw, gRazor II: In situ error detection and correction for PVT and SER tolerance,h *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 32–48, Jan. 2009.

[9] H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, gAdaptive Performance Compensation with In-Situ Timing Error Predictive Sensors for Subthreshold Circuits,h *IEEE Transactions on VLSI Systems*, vol. 20, no. 2, pp. 333–343, Feb. 2012.

[10] J. Tschanz, K. Bowman, S. Walstra, M. Agostinelli, T. Karnik, and V. De, gTunable replica circuits and adaptive voltage-frequency techniques for dynamic voltage, temperature, and aging variation tolerance,h *Symposium on VLSI Circuits Digest of Technical Papers*, pp.112–113, Jun. 2009.

[11] M. Fukazawa, M. Kurimoto, R. Akiyama, H. Takata, M. Nagata, gExperimental evaluation of digital-circuit susceptibility to voltage variation in dynamic frequency scaling,h *VLSI Circuits, 2008 IEEE Symposium on*, pp.150–151, Jun. 2008.

[12] S. Lopez-Buedo and E. Boemo, gMaking visible the thermal behavior of embedded microprocessors on FPGAs: a progress report,h in *Proc. of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays, ser. FPGA f04. ACM*, pp.79–86, 2009.

[13] Y. Ogasahara, T. Enami, M. Hashimoto, T. Sato, and T. Onoye, gValidation of a Full-Chip Simulation Model for Supply Noise and Delay Dependence on Average Voltage Drop with On-Chip Delay Measurement,h *IEEE Trans. on CAS-II*, vol. 54, no. 10, pp. 868–872, Oct. 2007.

[14] M. Abramovici, P. Bradley, K. Dwarakanath, P. Levin, G. Memmi, D. Miller, gA reconfigurable design-for-debug infrastructure for SoCs,h in *Proc. of the 43rd annual Design Automation Conference*, pp. 7–12, Jul. 2006.

[15] T. Sakurai, A.R. Newton, gAlpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas,h *IEEE Journal of Solid-State Circuits*, vol.25, no. 2, pp.584-594, Apr. 1990.

[16] S. Park, T. Hong, S. Mitra, gPost-silicon bug localization in processors using instruction footprint recording and analysis (IFRA),h in *IEEE TCAD*, vol. 28, no. 10, pp.1545–1558, 2009.