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A 0.8-V 110-nA CMOS current reference circuit using subthreshold operation

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Abstract: This paper proposes a low voltage CMOS nano-ampere current reference circuit and presents its performance with circuit simulations in 180-nm technology. The proposed circuit consists of bias-voltage, current-source and offset-voltage sub-circuits with most of MOSFETs operating in subthreshold region. Simulation results show that the circuit generates a stable reference current of 110-nA in supply voltage range of 0.8–1.8-V with line sensitivity of 9250 ppm/V. The proposed circuit is useful for composing a voltage reference circuit for ultra-low power applications.

Keywords: nano-ampere current reference, low voltage, subthreshold, low power

Classification: Integrated circuits

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1 Introduction

Nowadays, a larger percentage of mixed-signal applications are built under very strict requirements on power consumption. For example, for sensor networks and biomedical implants, power consumption is the most critical design factor to make the lifetime of the system long enough for a practical use [1]. For digital circuits in a mixed-signal chip, subthreshold and near-threshold circuits, which are intensively studied, can be adopted for low power operation, and the chip integration with energy scavenging and low voltage regulation is explored [2]. However, low voltage design for analog circuits is not straightforward compared to digital circuits. To operate a mixed-signal chip at low voltage, developing a new circuit structure for each analog building component is necessary.

One of basic and indispensable components is voltage reference circuits that can provide sub-1V voltage reference, and several circuit proposals are reported in literature [3, 4, 5, 6, 7, 8]. A reference voltage is generated using CMOS bandgap reference (BGR) circuit which requires a stable reference current, and thus a basic component of CMOS BGR circuit is current reference circuit. The BGR can operate at nano-watt power if the current reference circuit generates a current of nano-ampere order. Motivated by this, [3] proposed to generate sub-1V voltage reference by dividing the BGR voltage by two with a source-follower circuit. This sub-BGR requires a low voltage nano-ampere current reference circuit that is tolerant to process and supply voltage variations of [3], and in the current implementation, the minimum operating voltage of the current reference circuit is limiting that of the entire sub-BGR. To enable the sub-BGR circuit to operate at sub-1V supply voltage, we need to develop a nano-ampere current reference circuit that can operate at sub-1V voltage.

In this work, we propose a nano-ampere current reference circuit which can operate at 0.8 to 1.8-V generating 110-nA reference current in 180-nm CMOS technology. The temperature coefficient of the voltage is 9770 ppm/°C in the range from −20 to 100°C. The line sensitivity is 9250 ppm/V in the supply voltage range of 0.8–1.8-V. It should be noted that the smaller temperature coefficient is not necessary for this purpose, since the following PTAT voltage generation circuit will compensate the temperature depen-

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dence. This work therefore focuses on lowering supply voltage.

2 Current reference circuits

Subthreshold current I_D of a MOSFET is an exponential function of gate-source voltage V_{GS} and drain-source voltage V_{DS}, can be expressed as

$$I_D = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right), \tag{1}$$

where K $(= W/L)$ is aspect ratio of transistor, I_0 $(= \mu C_{OX} V_T^2(\eta - 1))$ is pre-exponential factor of the subthreshold current, μ is carrier mobility, C_{OX} is gate-oxide capacitance, V_T $(= k_B T/q)$ is thermal voltage, k_B is the Boltzmann constant, T is absolute temperature, q is elementary charge, V_{TH} is threshold voltage and η is subthreshold slope factor. For $V_{DS} > 0.1V$, current I_D is almost independent of V_{DS}.

Fig. 1 shows the proposed nano-ampere current reference circuit with large output resistance yet low minimum power supply voltage, which consists of three subcircuits; current source and bias voltage generation circuits for a MOS resistor and cascode transistors. The proposed current reference circuit adopts the current mirror circuit shown in Fig. 2, which is suitable for low voltage operation compared to single or cascade current mirrors [9]. The diode-connected MOSFETs in cascode bias voltage generation subcircuit generate a voltage for M3-M4 in the current-source subcircuit, which set up the output current.

In this circuit, the current I_{REF} flowing in the circuit is determined by the characteristics of NMOS MR resistor that is operating in the strong-inversion and deep-triode region. When drain-source voltage $V_{DS,R}$ is small enough $(V_{GS,R} - V_{TH} \gg V_{DS,R})$, the current is given by

$$I_{REF} = \mu C_{OX} K_R (V_{GS,R} - V_{TH}) V_{DS,R}. \tag{2}$$

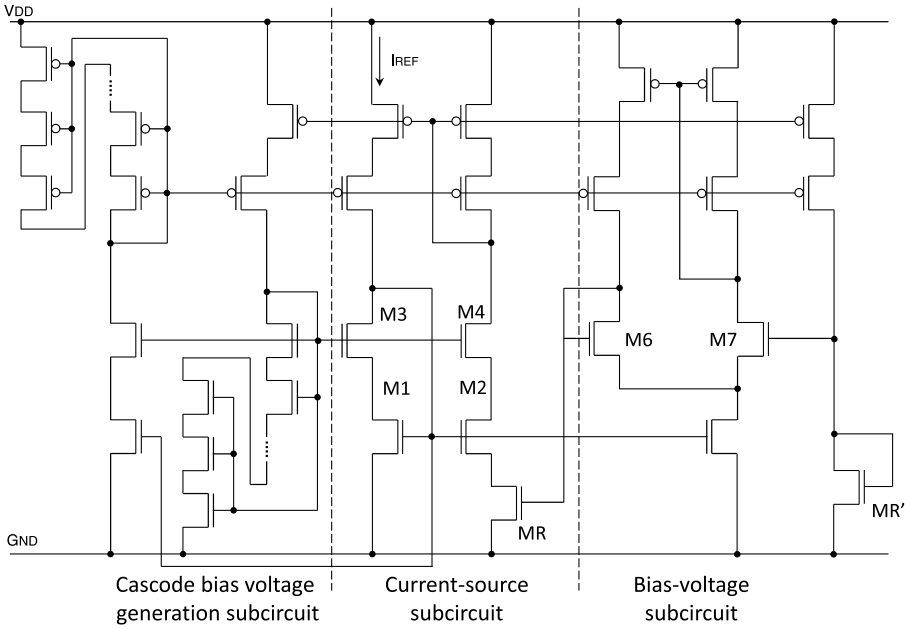

Fig. 1. Proposed current reference circuit.

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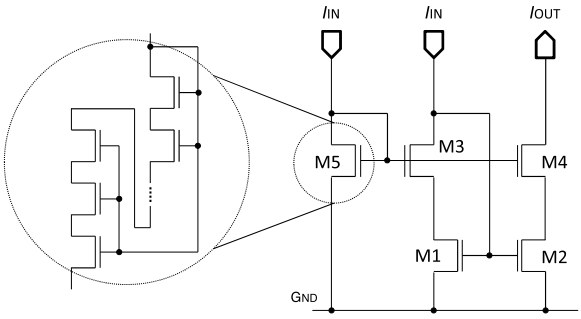

Fig. 2. Schematic of wide-swing cascode current mirror.

Using a linear resistor to set the bias current of the current-reference circuit makes the current sensitive to supply voltage and temperature [10]. Additionally, subthreshold operation requires a very large resistance value, since the current amount is very small. We thus adopt a MOS resistor instead of a linear resistor.

The characteristics of MOS resistor MR is controlled by the bias-voltage subcircuit. The voltages $V_{DS,R}$ $(= V_{GS,1} - V_{GS,2})$ and $V_{GS,R}$ $(= V_{GS,R'} - V_{GS,7} + V_{GS,6})$ are expressed as

$$V_{DS,R} = \eta V_T ln\left(K_2/K_1\right), \tag{3}$$

$$V_{GS,R} = V_{GS,R'} + \eta V_T ln\left(K_7/K_6\right), \tag{4}$$

where $V_{GS,i}$ is the gate-source voltage of M_i and K_i is the aspect ratio of M_i $(K_6 < K_7,\ K_1 < K_2)$. From Eq. (2), (3) and (4) the current I_{REF} can be expressed as

$$I_{REF} = \mu C_{OX} K_R \eta^2 V_T^2 ln\left(\frac{K_7 I_{REF}}{K_{MR'} K_6 I_0}\right) ln\left(\frac{K_2}{K_1}\right), \tag{5}$$

We can see that V_{TH} is excluded in Eq. (5) by assuming the threshold voltage of MR matches that of MR'. The matching is improved by layout proximity, layout topology and larger transistor size. Thus, the output current I_{REF} of the proposed circuit is robust to process variations.

In circuit design, we equally designed the channel lengths of transistors pairs (M_6-M_7, M_1-M_2) to mitigate the threshold voltage mismatch that arises from geometry differences of devices. Each pair of these two transistors was designed as subthreshold MOS resistor ladder consisting of 10 transistors connected in series.

3 Simulation results

SPICE simulations were carried out to evaluate the performance of the proposed circuit designed for a 180-nm technology with 1.8-V supply voltage. Fig. 3 shows the supply voltage dependence of the output reference current I_{REF} at room temperature. For a comparison, we designed two current reference circuits with single current mirror and cascode current mirror. This figure shows that the current reference circuit with single current mirror can operate at low $V_{DD,min}$, but due to low output resistance I_{REF} increases

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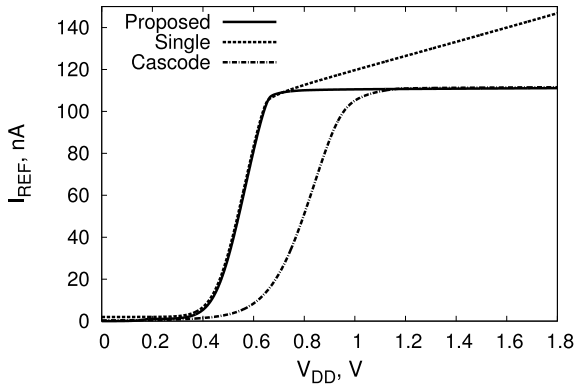

Fig. 3. Simulated output current I_{REF} at room temperature as a function of supply voltage.

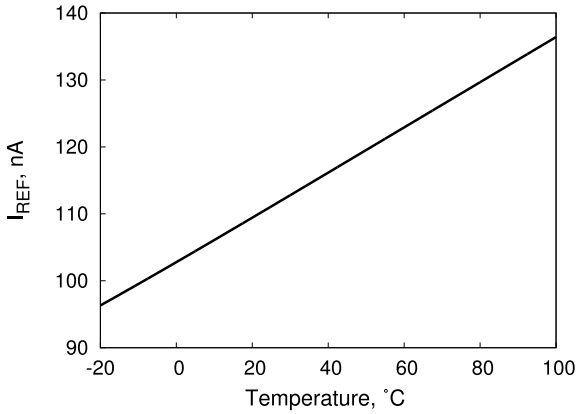

Fig. 4. Temperature dependence of output current I_{REF}.

linearly as V_{DD} increases. The line regulation of that with cascode current mirror is much better, compared to the single current mirror. However, the $V_{DD,min}$ is almost two times higher. The line regulation of the proposed circuit is 9250 ppm/V over the wide range of supply voltage from 0.8 to 1.8-V. The circuit can also operate at 0.75-V supply voltage, but then line regulation coefficient drops to 13300 ppm/V. The proposed circuit is comparable to reference circuit with single current mirror in low-voltage operation, and to reference circuit with cascode current mirror in line regulation.

Fig. 4 shows the simulated output current I_{REF} as a function of temperature. The average current was 116-nA and the temperature variation was 0.398-nA in the temperature range from -20 to 100°C. The temperature coefficient is 9770 ppm/°C.

To evaluate the dependence of the output current on process variations, we performed Monte Carlo simulations assuming random mismatch with ΔV_{TH} as a parameter. We assumed that ΔV_{TH} follows Gaussian distribution whose standard deviation depends on the device area ($A_{V_{TH}}/\sqrt{LW}$, where $A_{V_{TH,P}} = 4.432 \cdot 10^{-9} \frac{V}{m}$ and $A_{V_{TH,N}} = 3.635 \cdot 10^{-9} \frac{V}{m}$). Fig. 5 shows the histogram of the simulated output current for 1000 Monte Carlo simulations at room temperature. The mean (μ) and standart deviation (σ) of I_{REF} were 111 nA and 6.2 nA respectively.

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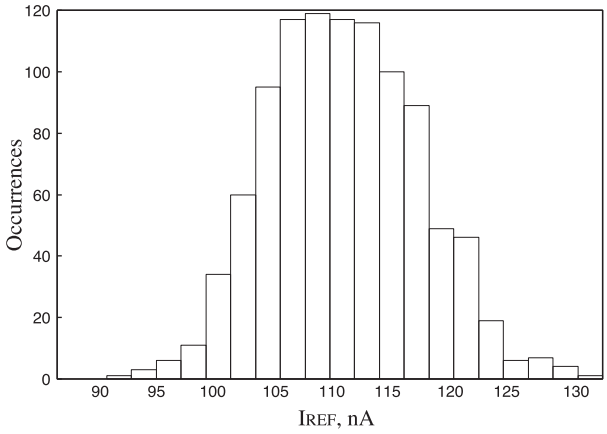

Fig. 5. The distribution of the output current I_{REF} at room temperature (Monte Carlo simulations: 1000 runs).

Table I. Performance summary and comparison with conventional current reference circuits.

	This work	Single	Cascode	[4]	[5]	[6]	[7]
Process (μm)	0.18	0.18	0.18	0.18	0.18	0.18	0.18
I_{REF} (nA)	110	110	110	7810	10000	40	2.05
Power (nW)	585	433	848	1400	80000	2.6	5.1
Temp. (°C)	−20–100	−20–100	−20–100	0–100	−20–120	−20–100	0–150
TC (ppm/°C)	9770	8890	9440	24.9	170	127	91
Min. supply (V)	0.8	0.8	1.4	1	2	0.6	0.85
Line reg. (ppm/V)	9250	278000	8650	1300	30000	27300	13500
Area (mm^2)	N/A	N/A	N/A	0.123	N/A	0.004	N/A

Table I summarizes circuit performances in comparison with other CMOS current reference circuits. The minimum supply voltage of the proposed reference circuit is 0.8-V and lower than those of [4] and [5]. Compared to low voltage circuits presented in [6] and [7], the proposed circuit attained better line regulation. Note that the temperature coefficient is compensated in the voltage reference circuit and hence it is not a matter in this work.

4 Conclusion

In this paper, we proposed a nano-ampere current reference circuit that can operate at a wide range of supply voltage, and the performance was simulated in 180-nm CMOS technology. The proposed circuit generates a stable reference current of 110-nA. The line sensitivity was 9250 ppm/V in supply voltage range of 0.8–1.8-V. The proposed circuit is useful for designing ultra-low power voltage reference circuit.

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