# Impact of NBTI-Induced Pulse-Width Modulation on SET Pulse-Width Measurement

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***Abstract*—This paper gives an explanation that SET pulse-width modulation in bulk CMOS devices happens due to negative bias temperature instability (NBTI). To investigate this, we propose and implement a stress adjustable pulse-width measurement circuit. Measurement results of test chips fabricated in a 65nm bulk CMOS process clearly show that pulse-width broadening and shrinking depend on the condition of static and dynamic stress before the pulse propagation. The measured dependency of pulse-width modulation on supply voltage is well correlated with that of NBTI model. We also point out that soft error rate computed from SET pulse-width distribution measured under static stress is pessimistic.**

***Index Terms*—Negative bias temperature instability, pulse-width measurement, pulse-width modulation, pulse-broadening, pulse-shrinking, single-event-transient.**

## I. Introduction

As technology advances, single-event-transient (SET) has become a serious issue in designing highly reliable circuits. When an SET occurs in combinational logic, the SET pulse propagates to sequential elements and causes errors when captured at clock edges. In this propagation process, there are three masking effects that may extinguish SET pulses; logical, electrical and latching-window masking. Logical masking happens when one of the other inputs of a gate is in controlling state (e.g., 0 for a NAND gate) and it blocks a pulse. Electrical masking is an effect that vanishes a pulse when propagating through a logic gate whose delay is comparable or larger than the pulse-width. Latching-window masking means the arrival transient pulse is outside of the latching window for the sequential elements.

Here, the probability of latching-window masking depends on the SET pulse-width, and hence the pulse-width affects soft error rate (SER) [1]. Besides, it is known that pulse-width modulation effects such as mismatch between rise and fall delays [2] broaden or shrink SET pulse-width. These effects also prevent researchers from precisely measuring SET pulse-width distribution.

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Recently, propagation-induced pulse-broadening (PIPB), which was first reported in [3], and its impact on SET pulse-width have been analyzed [3]–[6]. Reference [4] observed PIPB in heavy-ion SETs provoked in SOI and bulk inverter chains. Reference [5] explained that MOS memory effect, especially floating body effect (FBE), causes PIPB in silicon-on-insulator (SOI) and even in bulk devices. FBE causes hysteretic modulation in the threshold voltage $V_T$ of MOS according to the "ON" state condition of MOS devices. This memory effect causes not pulse-shrinking but pulse-broadening under the static "stress" condition because induced $V_T$ shift always reinforces pulse-broadening.

On the other hand, negative bias temperature instability (NBTI) is intensively studied. It increases the absolute value of PMOS threshold voltage depending on the stress history. A feature of NBTI is the recovery phase in which degraded threshold voltage partially recovers once the stress is eliminated. We found a similarity between the MOS memory effect discussed in [5] and NBTI. If NBTI would cause pulse-width modulation effect like as MOS memory effect, the impact of NBTI on SET pulse-width and its stress dependency must be clarified. In fact, when measuring SET pulse-width under radiation tests, the target circuit is usually under static stress condition, since SET pulses do not happen so frequently even under accelerated test especially in neutron case. This means the measured SET pulses are different with SETs in actual circuit. To precisely evaluate SET-induced soft error rate, we need to understand the NBTI mechanism behind pulse-width modulation and assess the impact of NBTI on SET pulse-width.

In this work, we presume that NBTI causes the propagation-induced modulation effect in bulk CMOS device and explain the mechanism of NBTI-induced pulse-width modulation. To measure the pulse-width difference originating from dynamic and static stress conditions, we propose a measurement circuit which is mainly composed of stress controller, pulse generator, modulation target (inverter chain), and pulse-to-digital converter. The stress controller can give multiple stress conditions to the inverter chain before pulse propagation. We can therefore measure the pulse-widths under the static and dynamic stress for pulses identically injected to the same inverter chain. The proposed circuit using a 2100-stage inverter chain as the modulation target was fabricated in a 65nm bulk CMOS process. Experimental results with 2-state stress control show that the measured pulse-width is dependent on the stress condition before the pulse propagation as we expected, and the pulse-width modulation under dynamic stress is up to 0.113 ps per inverter. We also validate that the dependency of the measured pulse modulation on supply voltage agrees with that of NBTI reported in [1]. Furthermore, we apply the measured modulation difference between static and dynamic stress to the SET pulse-width distri-

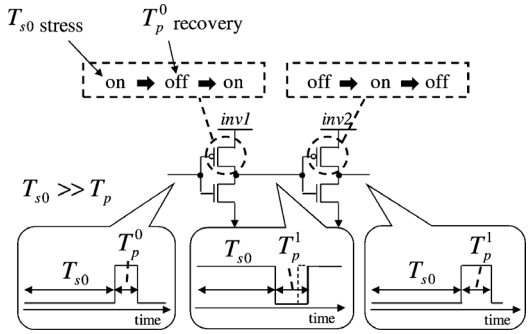


Fig. 1. Mechanism of static NBTI-induced pulse-width modulation.

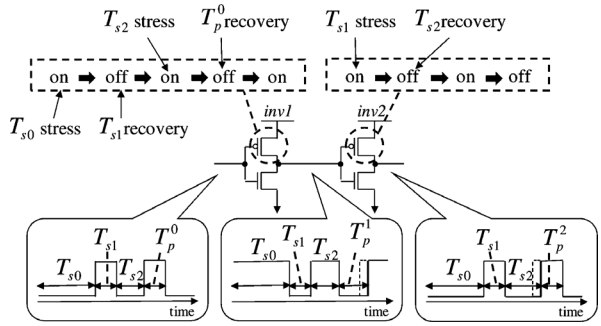


Fig. 2. Mechanism of 2-state dynamic NBTI-induced pulse-width modulation.

bution obtained in [7], and estimate SET pulse-width distribution under the dynamic stress. The estimated results show that NBTI-induced pulse-width modulation could reduce SER by 16.5% at maximum in 100-stage logic under the dynamic stress, and point out that SET pulse-width measured under the static stress gives pessimistic SER estimation without taking into account NBTI-induced modulation.

## II. Mechanism of NBTI-Induced Pulse-Width Modulation

NBTI causes PMOS $V_T$ degradation (increase in absolute value) during stress phase when the PMOS is ON-state and the degraded $V_T$ partially recovers during recovery phase when the PMOS is OFF-state [8]. For the sake of simplicity, we here discuss static and 2-state dynamic NBTI effects before pulse propagation, although NBTI aging effect depends on earlier history of stress and recovery.

First, Fig. 1 illustrates the NBTI-induced pulse-width modulation when a low-high-low pulse propagates through 2-stage inverters. Here, only NBTI effects affecting pulse-width $T_p$ are highlighted. When the static stress condition holds, i.e., $T_{s0} \gg T_p$, the PMOS of the first inverter $(\mathrm{inv1})$ is stressed during $T_{s0}$ and slightly recovers during $T_p$ before the PMOS drives the rise transition. On the other hand, looking at the second inverter $(\mathrm{inv2})$, NBTI does not affect $T_p$, since the first rise transition is driven by the PMOS that has recovered enough and the latest fall transition is not driven by the PMOS. In the static case, the amount of modulation in static stress $\Delta T_{p,\mathrm{static}}$ is expressed by

$$\Delta T_{p,\mathrm{static}} = \Delta T_{\mathrm{str}}(T_{s0}) - \Delta T_{\mathrm{rec}}(T_p) + \Delta T_{\mathrm{other}}, \quad (1)$$

where $\Delta T_{\mathrm{str}}(t)$ is delay increase of rise transition as a function of stress time, $\Delta T_{\mathrm{rec}}(t)$ is delay decrease of rise transition as a function of recovery time and $\Delta T_{\mathrm{other}}$ is sum of the other modulation effects, such as floating body effect.

Under the static stress condition, $\Delta T_{p,\mathrm{static}}$ increases with $T_{s0}$ and decreases with $T_p$. Note that even when $T_p$ becomes larger, pulse-broadening arises while the impact becomes smaller, because the recovery of $\mathrm{inv1}$ cannot exceed the degradation of $\mathrm{inv1}$.

We next extend the discussion above to 2-state dynamic stress and recovery scenario. Fig. 2 illustrates the 2-state dynamic NBTI-induced pulse-width modulation. In this dynamic scenario, the PMOS of $\mathrm{inv1}$ is stressed during $T_{s0}$, then recovers during $T_{s1}$, again is stressed during $T_{s2}$, and recovers during $T_p$ before the PMOS contributes to the final pulse propagation. In contrast to the static stress, PMOS of $\mathrm{inv2}$ is also stressed during $T_{s1}$ and recovers during $T_{s2}$. The amount of modulation due to dynamic stress $\Delta T_{p,\mathrm{dynamic}}$ is given by

$$\begin{aligned}\Delta T_{p,\mathrm{dynamic}} = {} & \Delta T_{\mathrm{str}}(T_{s0}) - \Delta T_{\mathrm{rec}}(T_{s1}) + \Delta T_{\mathrm{str}}(T_{s2}) \\ & - \Delta T_{\mathrm{rec}}(T_p) - (\Delta T_{\mathrm{str}}(T_{s1}) \\ & - \Delta T_{\mathrm{rec}}(T_{s2})) + \Delta T_{\mathrm{other}}. \end{aligned} \quad (2)$$

Under the dynamic stress condition, $\Delta T_{p,\mathrm{dynamic}}$ increases with $T_{s0}$ and $T_{s2}$, and decreases with $T_{s1}$ and $T_p$ by $\mathrm{inv1}$. In contrast to the static stress, $T_p$ may shrink if $T_{s1}$ is large enough compared to other stresses, i.e., $\Delta T_{\mathrm{str}}(T_{s1})$, NBTI-induced degradation of $\mathrm{inv2}$, dominates other terms in (2). In fact, this pulse-shrinking was observed in the measurement. An important point is that this pulse-shrinking can be clearly explained by NBTI. Extending the discussion to positive bias temperature instability (PBTI), which causes NMOS $V_T$ degradation in contrast to NBTI, is kept as a future work, since PBTI is not visible in the 65 nm technology used for chip fabrication in this work.

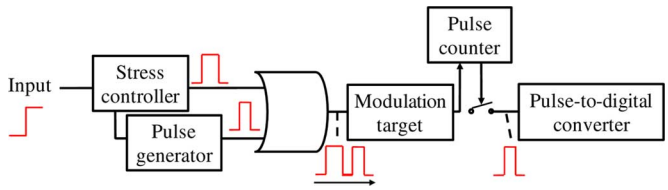


Fig. 3. Proposed circuit structure for pulse-width measurement.

## III. Pulse-Width Measurement Circuit

Fig. 3 shows the proposed structure for pulse-width measurement to confirm the mechanism of static and dynamic NBTI-induced pulse-width modulation. The measurement circuit consists of stress controller, pulse generator, modulation target (inverter chain), pulse counter, and pulse-to-digital converter. We briefly explain the operation of each module below.

Stress controller

It controls static/dynamic stress before the pulse propagation of our interest and sends a trigger signal to the pulse generator. The duration of each dynamic stress is configured by selecting internal delay elements or directly injecting an external signal.

Pulse generator

It generates a pulse whose width can be varied by selecting internal delay elements.

Modulation target

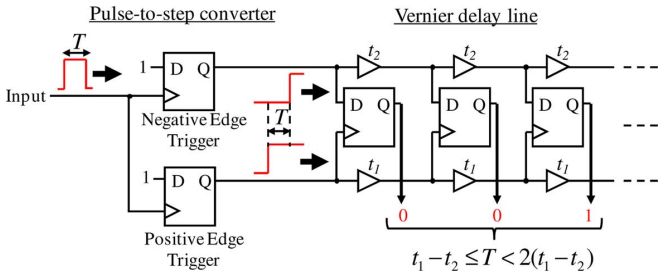


Fig. 4. Circuit configuration of vernier delay line measurement circuit.

The pulse-width modulation in this modulation target is measured by the proposed structure. Among a number of possible candidates, inverter chain, which is the simplest yet suitable for our purpose, is adopted for the analysis. To measure the pulse-width modulation accurately, it consists of a large number of inverters, since they accumulate pulse-width modulation and improve the measurable pulse-width modulation per stage. The inverter chain is carefully laid out with dense well contacts to suppress the FBE-induced modulation.

Pulse counter

To guide only the target pulse to pulse-to-digital converter, a switch and its control logic are implemented.

Pulse-to-digital converter

The pulse-width is measured using pulse-to-digital converter. One of possible implementations is vernier delay line (VDL) measurement circuit with a pulse-to-step converter [9] shown in Fig. 4. The pulse-to-step converter first transforms a pulse into two step signals whose time difference is equal to the original pulse-width, and they are given to the two buffer chains in VDL, whose buffer delay is $t_1$ and $t_2 (< t_1)$, respectively. Then these two signals race and finally the second signal overtakes the first signal because of the difference in the buffer delay $(t_1 - t_2)$. As a result, the inputted pulse-width is digitalized by the number of latches which the first signal passed before the overtaking. It should be noted that the stress condition for the two buffer chains in VDL can be equalized for any target pulses with any stress configurations because only the target pulse is given to VDL and then dynamic stress condition has no impact on the stress in VDL. Therefore, NBTI effect in VDL measurement circuit is not considered in this work.

## IV. Measurement Results

We fabricated a test chip in a 65 nm bulk CMOS process. A micrograph of the test chip is shown in Fig. 5. In this test chip, we implemented a 2-state stress controller which can control $T_{s1}$ and $T_{s2}$ shown in Fig. 2, a 2100-stage inverter chain, and a 3600-stage VDL measurement circuit which was designed to achieve 3.3 ps time resolution. The 2-state stress controller of this test chip can generate 100 ps, 500 ps, 1 ns, and 10 ns internal stress time for $T_{s1}$ and $T_{s2}$. Also, we can externally give stress time longer than 100 ns. The pulse generator of the test chip can also generate 100 ps and 500 ps pulse. Note that the absolute value of each internal stress time and pulse-width could

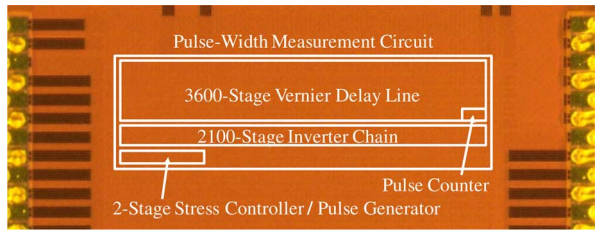


Fig. 5. A micrograph of the test chip in a 65 nm bulk CMOS process.

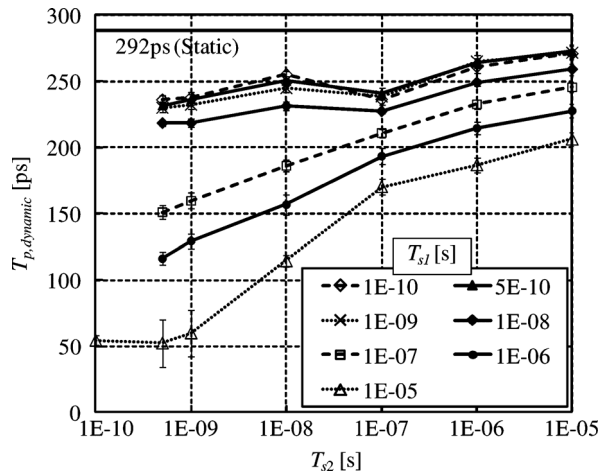


Fig. 6. Measured pulse-width modulation under static and dynamic stress condition.

be different because no measurement circuits for delay elements were implemented.

Static and dynamic NBTI-induced pulse-width modulation was measured in 1.2 V operation at room temperature. Fig. 6 shows the pulse-width under the static and dynamic stress condition in which both $T_{s1}$ and $T_{s2}$ were varied from 100 ps to 10 us. Under both the static and dynamic stress conditions, a 100 ps pulse was injected. The topmost horizontal line represents the measured 292 ps pulse under the static stress. This corresponds to 0.09 ps broadening per inverter, which is smaller than the FBE-induced broadening of 1.25 ps per inverter reported in [4] and the total ionizing dose (TID)-induced broadening of 0.25 ps per inverter in [6]. In this test chip, well contacts are densely placed in the modulation target, which mitigates FBE-induced broadening and consequently NBTI-induced broadening becomes visible. For each measurement, $T_{s0}$ was set to be larger than 1 s. Each plot represents the average of ten measured results and each error bar indicates $\pm\sigma$, where $\sigma$ is the standard deviation of the measured pulse-widths. Fig. 7 shows the modulation difference between $\Delta T_{p,\mathrm{dynamic}}$ and $\Delta T_{p,\mathrm{static}}$.

The results clearly indicate that pulse-width is modulated by dynamic NBTI stress. We can explain the decrease and increase of pulse-width according to the increase of $T_{s1}$ and $T_{s2}$ by (2), respectively. By decreasing $T_{s1}$ and increasing $T_{s2}$, the pulse-width on the dynamic stress becomes close to that of the static stress. On the other hand, by increasing $T_{s1}$ and decreasing $T_{s2}$, the pulse-width becomes smaller. Note that the width of injected pulse could not be measured on silicon, and hence the existence of NBTI-induced pulse-shrinking cannot be precisely discussed. Nevertheless, Fig. 6 suggested that NBTI-induced modulation

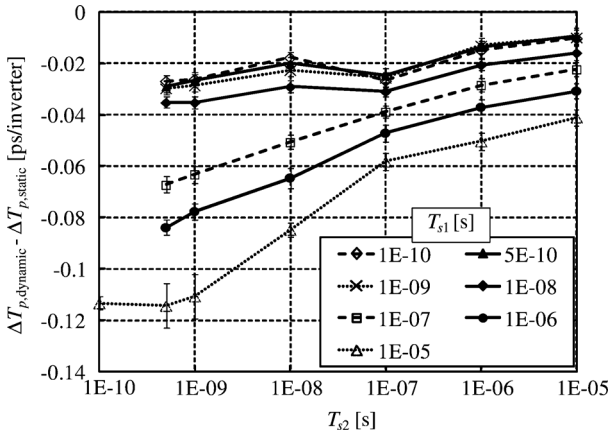


Fig. 7. Difference of pulse-width modulation between dynamic and static NBTI stress conditions.

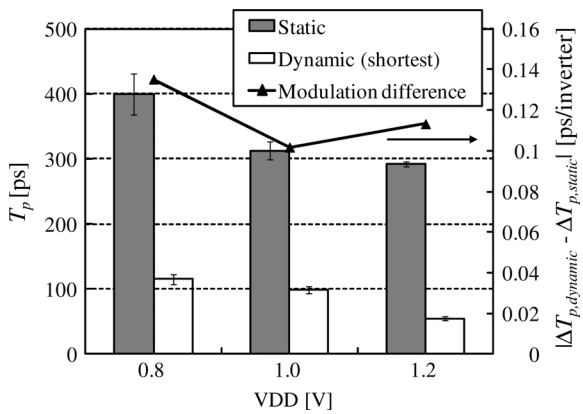


Fig. 8. Dependency of pulse-width modulation on supply voltage.

could shrink pulse-width to less than 100 ps. Further study is necessary on this point.

Besides, it is well known that NBTI depends on the supply (gate) voltage, temperature, and stress time, and the dependency is modeled in literatures, such as [10]. NBTI-induced $V_T$ shift can be expressed by [10]

$$\Delta V_T = A \cdot \exp(B \cdot V_{dd}) \cdot \exp(-C/T) \cdot t^{0.25} \qquad (3)$$

where $A, B$, and $C$ are constants, $V_{dd}$ is supply voltage, $T$ is temperature, and $t$ is stress time. Equation (3) indicates that $\Delta V_T$ has an exponential dependence on supply voltage $V_{dd}$.

To validate that NBTI causes the measured pulse-width modulation, the dependency of pulse-width modulation on supply voltage was measured. Fig. 8 shows the measured pulse-width under the static stress and the shortest pulse-width under the dynamic stress at each supply voltage, where the shortest width was obtained with $T_{s1} = 10\ \mu$s and $T_{s2} = 500$ ps. It also shows the modulation difference between static one and dynamic one, which corresponds to the largest modulation difference. Here, only the supply voltage of modulation target is varied. The modulation difference is non-monotonic in terms of supply voltage in our measurements.

Supposing that $\Delta V_T$ in the static stress is much larger than $\Delta V_T$ in the dynamic stress and $\Delta V_T$ in the dynamic condition is close to zero, the modulation difference comes from $\Delta V_T$ in static stress. The dynamic stress condition adopted for computing the modulation difference in Fig. 8 is thought to satisfy this criterion. We then translated the modulation difference into $\Delta V_T$ according to circuit simulation. In the simulation, we derived $\Delta V_T$ such that the pulse-width variation due to $\Delta V_T$ matched the measured modulation difference at each supply voltage. Fig. 9 shows that the derived $\Delta V_T$ increases exponentially as supply voltage becomes higher, where the curve represents the fitted exponential function. The $\Delta V_T$ values that reproduce the measured pulse-width modulation are consistent with the NBTI model, which clarifies that the measured modulation was caused by NBTI. This results point out that NBTI-induced pulse-width modulation is necessarily involved when measuring SET pulse-width distribution.

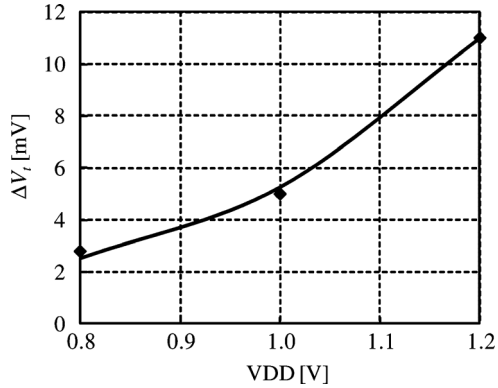


Fig. 9. The relation between the derived $\Delta V_T$ and supply voltage, where the curve represents the fitted exponential function.

Let us explain the reason on the non-monotonicity of the modulation difference in Fig. 8. The sensitivity of $\Delta V_T$ on inverter delay is different at each supply voltage, since the overdrive voltage of $V_{dd} - V_T$ determines the on-current. As the supply voltage becomes higher, $\Delta V_T$ increases but the sensitivity becomes smaller. As the mixture of these two tendencies, the modulation difference becomes the smallest at 1.0 V.

We also evaluated the temperature dependency of pulse-width modulation similar to the voltage dependency. The measured pulse-width modulations at 30°C and 80°C were translated to the $\Delta V_T$ values. $\Delta V_T$ at 80°C was 0.6 mV higher than that at 30°C, which suggests that the pulse-width modulation in this test chip is less dependent on temperature.

## V. Impact on Soft Error Rate

This section evaluates the impact of NBTI-induced pulse-width modulation on soft error rate. Using the modulation differences in Fig. 7, we can estimate the SET pulse-width distribution under the dynamic stress condition from the SET pulse-width distribution measured under the static stress. As an example, the SET pulse-width distribution reported in [7] is used.[1] In [7], 10-stage inverter chains are used as SET target circuits. As a comparison, we apply the largest modulation difference of 0.113 ps per inverter, which corresponds to the situation where $T_{s1}$ equals 10 $\mu$s and $T_{s2}$ equals to 500 ps. Fig. 10 shows cumulative distribution functions of SET pulse-width distribution measured under both static and dynamic stress conditions. For

[1]The distribution was obtained at 0.8V in [7] while NBTI-induced pulse modulation was measured at 1.2 V. Therefore, the discussion here is for a demonstration purpose.

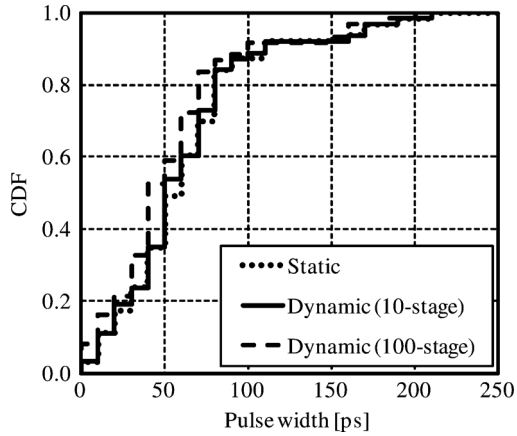


Fig. 10. Cumulative distribution functions of SET pulse-width distribution measured under the static stress and SET pulse-width distributions calculated supposing the dynamic stress condition.

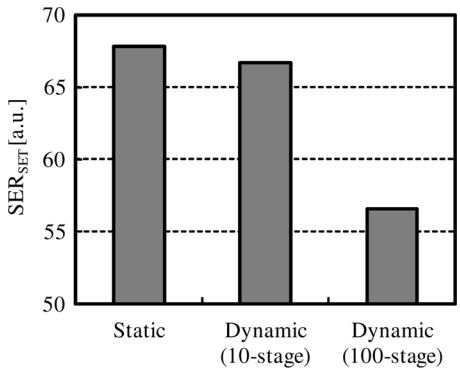


Fig. 11. Calculated SER of SET under the static/dynamic stress conditions.

the dynamic stress condition, two cases are considered by supposing all the SETs are propagating through either 10-stage or 100-stage inverter chain. For example, in case of 100-stage inverter chain under the dynamic stress, SET pulse-width distribution is shifted to the left by 11.3 ps.

Then, the impact of the modulation difference induced by NBTI on SER of SET $(\mathrm{SER_{SET}})$ is evaluated using the relation below [1]

$$\mathrm{SER_{SET}} = \sum_{i=1}^{n} f(X_i) * T_{p,i}/T_{\mathrm{clk}} * T_{\mathrm{der}} \tag{4}$$

where $T_{p,i}$ is interval of pulse-width, $f(X_i)$ is a probability density function of SET, $T_{\mathrm{clk}}$ is clock time for sequential elements, and $T_{\mathrm{der}}$ is derating factor decided by logical and electrical masking of combinational circuit. Because $T_{\mathrm{clk}}$ and $T_{\mathrm{der}}$ depend on the configuration of logic combinational circuit, we suppose $T_{\mathrm{clk}}$ and $T_{\mathrm{der}}$ are constant. Fig. 11 shows the $\mathrm{SER_{SET}}$ of each SET pulse-width distribution. The modulation difference of 0.113 ps per inverter decreases SER by 16.5% compared to the static stress in 100-stage inverter chain, in other word, SER computed from SET pulse-width distribution measured under the static stress is overestimated by more than 20% comparing to the distribution under the actual dynamic circuit operation. This results point out that NBTI has a significant impact on SET-originating SER and should be considered in SER estimation.

## VI. Conclusion

We revealed the mechanism of NBTI-induced pulse-width modulation under the static and dynamic stress condition. We proposed a pulse-width measurement circuit which can adjust 2-state stress. Using the test chip fabricated in 65 nm CMOS bulk process, we observed pulse-width broadening and shrinking under the static and dynamic stress conditions. The measurement results showed that the largest modulation difference between the static and dynamic stress is 0.113 ps per inverter. The dependency of measured pulse-width modulation on supply voltage is well explained by the exponential dependency of $\Delta V_T$ on supply voltage in NBTI model. We further estimated SER under the static and dynamic stress, and showed that the static SET characterization overestimates SER by 20%.

## Acknowledgment

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