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Representative Frequency for Interconnect R(f)L(f)C Extraction

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SUMMARY This paper discusses the frequency to extract RLC values from interconnects. In circuit design, frequency-independent equivalent circuit is widely used, and many design and analysis techniques based on this equivalent circuit are proposed so far. However in reality, characteristics of interconnects are frequency-dependent. Also pulse waveforms in digital circuits contain multiple frequency components. The frequency used for RLC extraction affects the accuracy of interconnect characterization, and hence careful determination of extraction frequency is critical. We propose a representative frequency for RLC extraction. Conventionally, representative frequencies are determined by input pulse. The proposed method decides the representative frequency based on the interconnect length, whereas conventional representative frequencies are determined by input pulse shape, period and patterns. We verify that the extraction at the proposed frequency provides the most accurate transition waveform against various input signals and interconnect structures in digital circuits.

key words: *interconnect, extraction, frequency-dependent*

1. Introduction

As increasing operating frequency, frequency-dependence of interconnect characteristics is becoming significant. Interconnect characteristics, especially resistance and inductance depend on frequency because of skin-effect and proximity effect. In frequency-dependent interconnects, the behavior of interconnects depends on frequency e.g. attenuation and phase velocity dispersion. In digital circuits, common input waveforms of interconnects are trapezoidal pulses. A trapezoidal pulse contains frequency components from DC to ∞. Moreover, the input pulse pattern is not entirely periodic. The frequency spectrum varies depending on the width of pulse and the period. The minimum pulse width and period are determined by system clock. But on signal line, the pulse pattern depends on the circuit behavior.

To treat frequency-dependent interconnects, several frequency-dependent circuit models are proposed [1]–[3]. The frequency-dependent models improve simulation accuracy [2], [4], [5], but in circuit design, frequency-dependent models are not used so commonly. Because most of conventional design methods are based on the frequency-independent model.

If interconnect characteristics can be modeled well by a single frequency, we can use the design techniques proposed so far, e.g. circuit reduction, buffer insertion and timing analysis [6], [7]. Furthermore, frequency-independent RLC values can intuitively predict fundamental interconnect characteristics such as characteristic impedance. However, determination of a single extraction frequency is difficult.

Conventionally, it is a common way to decide the representative frequency from signal patterns. However, voltage waveforms also depend on the interconnect structure, such as the length of interconnects. So in the frequency components that dominately characterize the interconnect characteristics, there are some frequencies determined by the interconnect length. The representative frequency determined by the interconnect structure has not been discussed so far. This paper focuses on the representative frequency decided by interconnect length.

In Ref. [8], the necessity of frequency-dependent model is discussed. Reference [8] compares a frequency-dependent model with an equivalent circuit extracted at DC from viewpoint of signal delay, crosstalk noise and so on. The interconnect structures that Ref. [8] discusses have weak frequency dependence, and hence the authors conclude that DC extraction is good enough for signal delay evaluation. However in actual chips, there are wide interconnects whose frequency dependence becomes significant in lower frequency of 1 to 2 GHz. We experimentally observe that DC extraction causes considerable error for such interconnects. As for crosstalk noise, Ref. [8] reports that frequency dependence model is necessary. However the authors examine only DC extraction and frequency dependence model. Therefore it is not clear whether crosstalk can be estimated using a certain representative frequency for RLC extraction.

In this paper, the extraction frequency based on the interconnect length is proposed. It is commonly adopted to determine the representative frequency from the shape of an input signal waveform, especially from the rise time, focusing on the spectrum of the input signal. This is natural and reasonable when we analyze the incident waveform to the near-end of the interconnects. On the other hand, our main interest is the analysis of the waveform at the far-end. As signals are propagating through an interconnect, high-frequency components are easy to attenuate. The dominant

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frequency components that determine the far-end waveform are different from those for the near-end waveform. We observe that accurate estimation of attenuation behavior is crucial to obtain accurate far-end waveforms. An on-chip transmission-line with CMOS receiver can be regarded as a resonator. From the theory of a resonator, the frequency where attenuation becomes minimum is decided by the interconnect length. We reveal that this resonance frequency is the dominant frequency to characterize far-end waveforms, and then propose to adopt it as the representative frequency used for interconnect RLC extraction. We experimentally verify that the most accurate waveform is obtained when the proposed frequency is used for extraction. We show that the maximum errors in our experiments are below 8% in the voltage amplitude, signal delay and the amplitude of crosstalk noise. Therefore the proposed frequency enables accurate transient analysis using frequency-independent interconnect model.

In Sect. 2, interconnect modeling and its problems are described. We next discuss the extraction frequency in digital circuits. We then show the experimental results in Sect. 4. Section 5 discusses the tolerance to the extraction frequency variation. Section 6 concludes the discussion.

2. Problem Description

This section describes the problem discussed in this paper. We first show frequency-dependence of interconnects and demonstrate its impact to transient analysis. Then the extraction frequencies in digital circuits are explained.

2.1 Frequency-Dependence of Interconnect Characteristics

Frequency-dependence of interconnects is caused by skin-effect and proximity effect. So the characteristics variation is strongly related with the frequency and the interconnect structure. Skin effect and proximity effect are remarkable on wide and thick interconnects. Because, skin depth becomes comparable to the interconnect size in relatively lower frequency.

Figure 1 shows an example of resistance and inductance characteristics. The resistance and inductance values are calculated by a field-solver [9]. The assumed interconnect structure is co-planar, and the width of the signal line is $10\,\mu$m, the width of the ground line is $40\,\mu$m and their spacing is $2\,\mu$m. In this case, the resistance increases by 10% from DC to 1.2 GHz, and the inductance decreases by 10% from DC to 1.9 GHz. The resistance and the inductance change in relatively low frequency of 1 to 2 GHz, and thus frequency-dependence is not negligible to model interconnects in current high-performance circuits any longer.

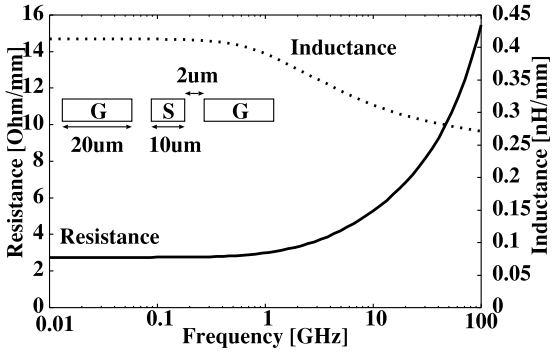

Fig. 1 Frequency-dependence of resistance and inductance. (co-planar structure, signal line width $10\,\mu$m, ground line width $40\,\mu$m, spacing $2\,\mu$m)

2.2 Interconnect Models and Their Impact on Transition Waveform

Generally, interconnects in VLSIs are expressed by lumped RLC for circuit design. To model long interconnects that have transmission line characteristics, RLC ladder circuit as Fig. 2 is used. This ladder model cannot consider the frequency-dependence of interconnect characteristics. A number of frequency-dependent models are proposed [1]–[3]. In this paper, we use the model of Ref. [10] as the frequency-dependent model. It is implemented in HSPICE [11] as w-element model.

Figure 3 shows the impact of frequency-dependence on transient analysis. The simulated circuit is shown in Fig. 3. Interconnect characteristic impedance Z_0 is $55\,\Omega$ and the output impedance of the driver $R_{\rm d}$ is $10\,\Omega$. The solid line labeled "FD" shows the voltage waveform at the far-end by the frequency-dependent model. In this paper, we use "FD" as the abbreviation of "Frequency-Dependent model." The dashed lines labeled "DC" and "$f_{\rm sig}$" are the results of frequency-independent models. "DC" means the RLC ladder model extracted at DC, and "$f_{\rm sig}$" corresponds to RLC extraction at the significant frequency [7]. The number of ladder is 51. Significant frequency is one of the representative frequency defined from the frequency components of

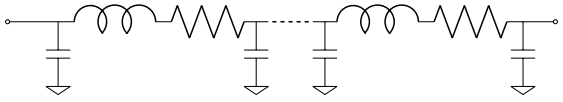

Fig. 2 RLC ladder circuit model.

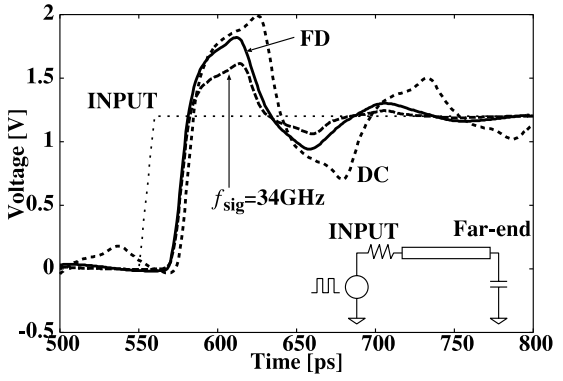

Fig. 3 The impact of frequency-dependence. ($Z_0 = 55\,\Omega$, $R_{\rm d} = 10\,\Omega$)

a trapezoidal pulse, and it is explained in the next section. As you see, both waveforms of the conventional frequency-independent models ("DC" and "$f_{\rm sig}$") are far from that of frequency-dependent model ("FD"). When R and L are extracted at DC, the extracted resistance is too low, and, the resistance extracted at significant frequency is too high. From the above observations, we can expect that a frequency between DC and significant frequency provides the waveform that is close to the waveform of the frequency-dependent model. If the representative frequency can be determined systematically, we can model interconnects by a single frequency. In the following section, we discuss the way to determine the representative frequency to model interconnects at a single frequency.

3. Representative Frequency for Extraction

In this section, we discuss the representative frequency to extract interconnect RLC. Conventionally, frequency determined from input pulse is used for interconnect extraction. We first explain some representative frequencies conventionally used for extraction, and we then propose the representative frequency calculated from interconnect length.

3.1 Conventional Methods

In digital circuits, a trapezoidal pulse that contains multiple frequency components is a common waveform. An example of frequency components are shown in Fig. 4. $T_{\rm p}$ is the period of the pulse, $T_{\rm w}$ is the width of the pulse. In order to derive frequency-independent model of Fig. 2, we have to choose a single extraction frequency.

There are several representative frequencies of periodic pulse waveform. One of them is the frequency of pulse. As shown in Fig. 4, this frequency is the maximal component of the frequency spectrum. Other one is significant frequency [7]. Significant frequency is expressed by signal transition time $t_{\rm r}$. The significant frequency $f_{\rm sig}$ is defined such that the signal energy from DC to $f_{\rm sig}$ becomes 75% of all signal energy. In the range $7 \leq T_{\rm w}/t_{\rm r} \leq 13$, $f_{\rm sig}$ is given by $0.34/t_{\rm r}$ [7]. On the other hand, DC is often used for extraction. Reference [8] concludes that the extraction at DC is accurate enough to estimate signal delay and overshoot/undershoot. DC extraction is enough when frequency-dependence is weak, e.g. narrow interconnects or low frequency. But as shown in Fig. 3, RLC ladder extracted at DC or the significant frequency causes considerable amount of errors in transient analysis.

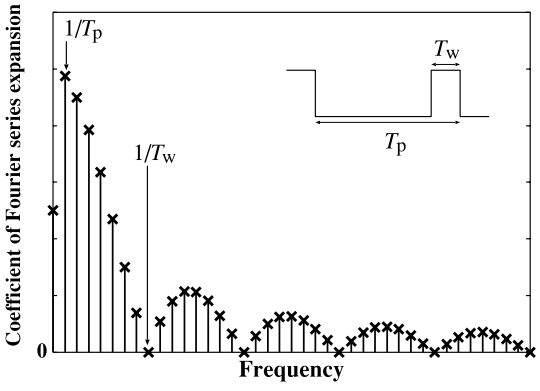

Fig. 4 Frequency spectrum of periodic rectangle pulse.

3.2 Proposed Method

Conventional methods based on input pulse shape focus on the frequency components at the near-end of interconnects. However the far-end waveform is more important for circuit designer because the waveform directly affects signaling delay. The far-end waveform becomes totally different because of attenuation and reflection. We propose an extraction frequency that aims to express accurate far-end waveforms. Figure 5 shows step responses obtained with a FD model and a ladder extracted at significant frequency $f_{\rm sig}$. The interconnect structure and driver impedance $R_{\rm d}$ are the same as Fig. 3. As shown in Fig. 5, the ladder extracted at $f_{\rm sig}$ models the incident wave of interconnects well, but a remarkable error occurs at the far-end. This error is mainly caused by overestimation of attenuation. The balance of driver resistance $R_{\rm d}$ and characteristic impedance Z_0 determines the incident wave. Characteristic impedance is expressed as

$$Z_0 = \sqrt{\frac{R + {\rm j}\omega L}{G + {\rm j}\omega C}} \simeq \sqrt{\frac{L}{C}}. \tag{1}$$

Approximately, characteristic impedance is proportional to square root of inductance $\sqrt{L}$. The attenuation of interconnect affects the waveform at the far-end. The attenuation constant α is expressed as

$$\alpha = {\rm Re}\left[\sqrt{(R + {\rm j}\omega L)(G + {\rm j}\omega C)}\right] \simeq \frac{R}{2}\sqrt{\frac{C}{L}}. \tag{2}$$

Attenuation constant is roughly proportional to resistance R and square root of inductance $\sqrt{L}$. From the above equations, variation of resistance strongly affects waveform propagation. Moreover, as shown in Fig. 1, the variation of

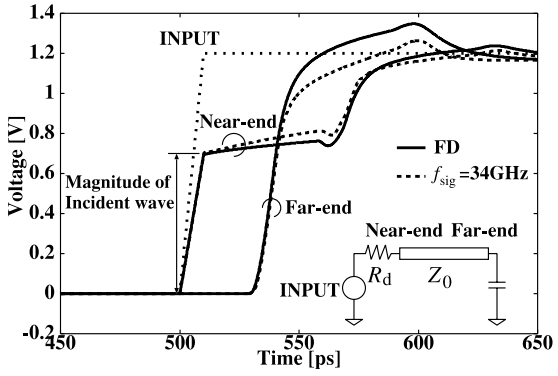

Fig. 5 Waveform at near-end and far-end. (interconnect structure is shown in Fig. 1, $Z_0 = 55\,\Omega$, $R_{\rm d} = 10\,\Omega$)

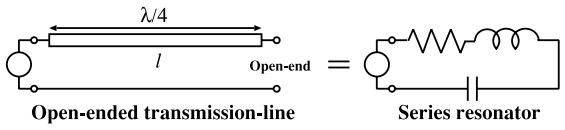

Fig. 6 Open-ended transmission-line and equivalent series resonator.

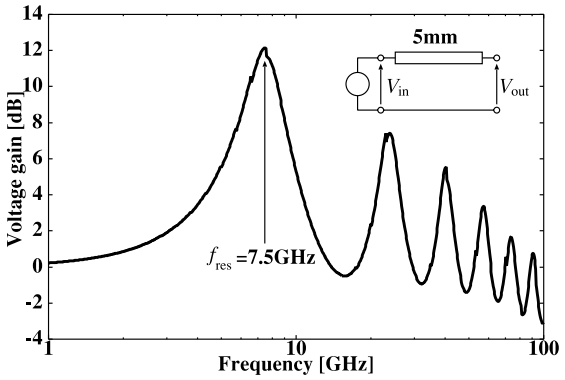

Fig. 7 Transfer characteristics of a transmission-line shown in Fig. 1, interconnect length is 5 mm.

resistance is larger than that of inductance. At 34 GHz of Fig. 1, inductance decreases by about 30% from DC and resistance increases by about 230% from DC. The inductance decreases because of proximity effect and the internal-inductance decreasing. Therefore the inductance value saturates at high frequency. On the other hand, resistance increases exponentially as frequency become higher. Therefore the estimation of resistance is critical to model far-end waveform. The attenuation strongly depends on interconnect structure such as interconnect length. From above discussion, we have to consider interconnect structure when determining an extraction frequency.

To determine an extraction frequency from the far-end of interconnects, we have to specify the dominant frequency component at the far-end. From the theory of open-ended transmission-line resonators, when the quarter wavelength $\lambda/4$ is equal to interconnect length l, transmission-lines are equivalent to a series resonator shown in Fig. 6. When quarter wavelength $\lambda/4$ is equal to interconnect length l, the frequency $f_{\rm res}$ is expressed by

$$f_{\rm res} = c/\lambda = c/4l, \tag{3}$$

where c is the velocity of electromagnetic wave. When the frequency is $f_{\rm res}$, the impedance of series resonator become minimum and the attenuation of frequency component $f_{\rm res}$ is minimum. Figure 7 shows a transfer characteristic of a transmission-line. The interconnect structure is the same as Fig. 1 and interconnect length is 5 mm. The relative permittivity of SiO_2 is 4.0, so the velocity of electromagnetic wave is 1.5×10^8 m/s. In this case, resonance frequency $f_{\rm res}$ is 7.5 GHz. The voltage gain becomes maximum at the resonance frequency $f_{\rm res}$. Therefore the frequency component $f_{\rm res}$ strongly affects the waveform at the far-end. The frequency spectrum at the far-end is as shown in Fig. 8 when a

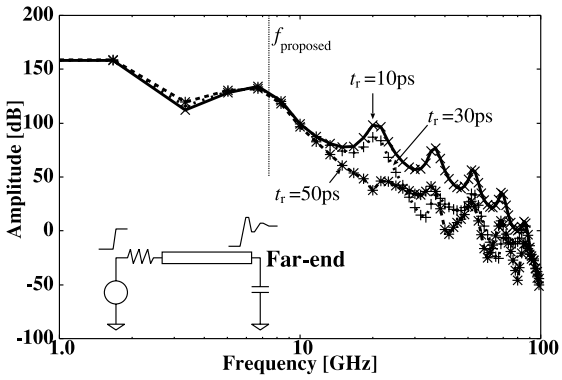

Fig. 8 Frequency spectrum of waveform at the far-end.

transmission-line is driven by a voltage source and a resistor. The frequency $f_{\rm res}$ is the first peak of frequency components regardless of various transition times. We hence consider the frequency $f_{\rm res} = c/4l$ as a representative frequency. The phase velocity of electromagnetic wave c is determined by the permittivity and permiability of insulator. Therefore in LSIs, we assume phase velocity c is constant. Frequency $f_{\rm res}$ is determined only by interconnect length. We propose this $f_{\rm res}$ as an extraction frequency. In following sections, we rewrite $f_{\rm res}$ to $f_{\rm proposed}$.

In Sect. 4, we experimentally verify the accuracy of several extraction frequencies; DC, proposed frequency $f_{\rm proposed}$ and significant frequency $f_{\rm sig}$.

3.3 Limitations of the Proposed Method

We here examine the limitation of the proposed method. The proposed method assumes that transmission-line characteristics of interconnects. This assumption at first seems to make a limitation. However, on reflection, we do not have to extract inductance of the interconnects without transmission line characteristics, because those interconnects can be treated as RC lump model. Therefore the assumption of transmission line behaviors does not limit the application area of the proposed method at all.

There are several methods to characterize the importance of transmission-line effect [7], [12], [13]. For example, from Ref. [12], when an interconnect length l satisfy

$$\frac{t_{\rm r}}{2v} = \frac{t_{\rm r}}{2\sqrt{LC}} < l < \frac{2}{R}\sqrt{\frac{L}{C}}, \tag{4}$$

transmission-line effect should be considered. Parameter $t_{\rm r}$ is the transition time of an input pulse. The lower limit is decided by signal transition time. Equation (4) means if twice of time-of-flight is smaller than the signal transition time, transmission-line effect could be ignored. The upper limit is depends on the attenuation.

The second assumption is that the resonance frequency is uniquely decidable, which means that the proposed method can not treat the interconnects with branches. But in general, interconnects exploiting transmission line effects are designed without branches. Therefore this assumption

does not reduce the application area of the proposed method so much. The proposed method is valid for the most of high-performance interconnects.

The third assumption is the termination of transmission-lines. The proposed method is based on open-ended transmission-line resonator. In most CMOS circuits, transmission-lines are terminated by input capacitance of receivers, which is small enough to assume open-ended. However on transmission-lines terminated by large capacitor or so, the resonance frequency $f_{\rm res}$ is not equal to $c/4l$. In such case, we have to decide resonance frequency by other way.

4. Experimental Results

This section shows some experimental results. We verify the modeling accuracy of each representative frequency by circuit simulation. We first explain experimental conditions and some metrics of accuracy. We then verify the accuracy under various experimental conditions, and we show that the proposed frequency $f_{\rm proposed}$ provides the most accurate modeling. We also reveal that the ladder extracted at frequency $f_{\rm proposed}$ is accurate enough to simulate interconnect behaviors.

4.1 Experimental Conditions and the Metrics of Accuracy

In this section, we explain experimental conditions and metrics of accuracy.

To cover all possible situations in digital circuits, we have to verify under various frequency-dependence and various waveforms. Frequency-dependence of interconnects is determined by the interconnect structures. Waveform variation is expressed by pulse period, duty ratio and transition time. We therefore vary the following parameters and evaluate the proposed and the conventional representative frequencies.

- pulse period and duty ratio ($f_{\rm p}$ changes and others are fixed).
- pulse transition time ($f_{\rm sig}$ changes and others are fixed).
- interconnect length ($f_{\rm proposed}$ changes and others are fixed).
- interconnect structure and driver strength.

We first discuss the variation of input pulse pattern. We vary pulse period and duty ratio, that is, this situation corresponds various input pulse pattern on signal interconnects. In this experiment, pulse frequency $f_{\rm p}$ changes according to pulse period, and other extraction frequency is fixed. Next, variation of pulse transition time is discussed. Transition time decides significant frequency, so $f_{\rm sig}$ varies and others are fixed in this experiment. We then verify the case that interconnect length changes. Frequency $f_{\rm proposed}$ varies as changing interconnect length, and other frequencies are fixed. The ranges of each parameter are listed in Table 1. When a parameter is changed, corresponding one of the representative frequencies also change. The range of the representative frequencies are also listed in Table 1.

Table 1 Range of parameters and representative frequencies.

Parameter range	Corresponding freq. range
500 ps $\leq T_{\rm p} \leq$ 5ns	200MHz $\leq f_{\rm p} \leq$ 2 GHz
10 ps $\leq t_{\rm r} \leq$ 100 ps	3.4 GHz $\leq f_{\rm sig} \leq$ 34 GHz
0.5 mm $\leq l \leq$ 10 mm	3.75 GHz $\leq f_{\rm proposed} \leq$ 75 GHz

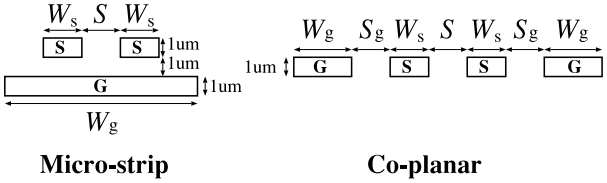

Fig. 9 Cross-sections of interconnects.

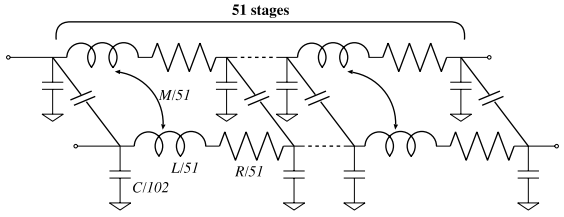

Fig. 10 Equivalent circuit of coupled transmission-line.

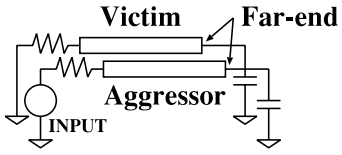

Fig. 11 Experimental circuit for transient analysis.

We experiment the above conditions in various interconnect structures and driver output impedance. On transmission-lines, a waveform strongly depends in the relation between characteristic impedance of the interconnect and output impedance of the driver. As the interconnect structure, two popular interconnect structures; micro-strip and co-planar are used. The cross-sections of two interconnect structures are shown in Fig. 9. $W_{\rm s}$ is the width of signal interconnect, $W_{\rm g}$ is the width of ground line, S is the spacing between signal interconnects and $S_{\rm g}$ is the spacing between the signal interconnect and the ground line. The structure parameters are varied in $1\,\mu{\rm m} \leq W_{\rm s} \leq 8\,\mu{\rm m}$, $8\,\mu{\rm m} \leq W_{\rm g} \leq 40\,\mu{\rm m}$, $2\,\mu{\rm m} \leq S \leq 8\,\mu{\rm m}$ and $2\,\mu{\rm m} \leq S_{\rm g} \leq 8\,\mu{\rm m}$. For circuit simulation, we extract RLC value from interconnect structures by a field-solver [9]. The interconnects are expressed by the equivalent circuit shown in Fig. 10. The number of ladder is 51. The equivalent circuit is synthesized using the RLC values at the extraction frequency. We create the equivalent circuits for each extraction frequency well as for each interconnect structure.

In transient analysis, we evaluate the voltage waveform of the experimental circuit as shown in Fig. 11. One of two lines is stimulated by the input pulse, and the other is quiet.

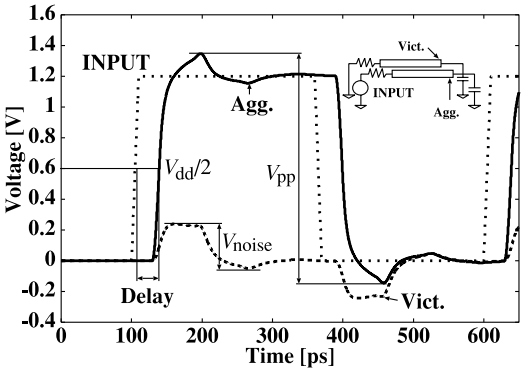

Fig. 12 Definition of delay time, peak-to-peak voltage and crosstalk.

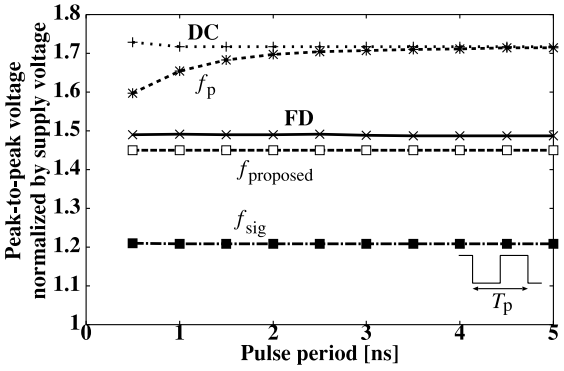

Fig. 13 Voltage peak-to-peak when the period of pulse changed.

We call the stimulated line as "Aggressor," and the quiet line as "Victim." The near-end of each line are held by a resistance, which represents the output impedance of the driver. The driver output impedance is varied from 10 Ω to 100 Ω. The far-end of each line is connected to the capacitor load that corresponds to the input capacitance of a receiver. The value of capacitor loads is fixed to 50 fF.

To verify accuracies of modeling, evaluation metrics are necessary. We use $V_{\rm dd}/2$ propagation delay time (Delay), amplitude of overshoot/undershoot ($V_{\rm pp}$) and amplitude of far-end crosstalk noise ($V_{\rm noise}$) as evaluation metrics. Figure 12 shows the definition of delay time, peak-to-peak voltage and crosstalk. We evaluate these metrics of the ladder extracted at each representative frequencies and frequency-dependent model. We consider the result of the frequency-dependent model as reference data. This means that the evaluation results that are close to those of frequency dependent model are accurate.

4.2 Pulse Pattern vs. Accuracy

We discuss the accuracy in the case that the input pulse pattern changes. In digital circuits, the width and period of pulse depend on the applied input pattern. As discussed in Sect. 3, frequency spectrum changes when width $T_{\rm w}$ and period $T_{\rm p}$ vary. The minimum $T_{\rm p}$ is determined by the clock frequency. $T_{\rm w}$ and $T_{\rm p}$ depend on input pulse pattern. When the logic state of the interconnect does not change, $T_{\rm w}$ and $T_{\rm p}$ become large and the duty ratio changes. For digital circuits, the model of interconnects have to be accurate even when $T_{\rm p}$ and $T_{\rm w}$ change. In this experiment, we use voltage peak-to-peak and signal delay time as evaluation metrics because crosstalk is not assumed to depend on the pulse period.

The errors in peak-to-peak voltage and delay time are shown in Fig. 13 and Fig. 14. We use a co-planar interconnect structure with 8 μm signal wire width, 20 μm ground wire width, 4 μm spacing between each interconnects and 5 mm length. The output impedance of the drivers is 50 Ω. The transition time of the input pulse is 10 ps, and the period is 500 ps. X-axis is the period of the pulse $T_{\rm p}$, where the duty ratio is set to be 50%. As you see, the errors of

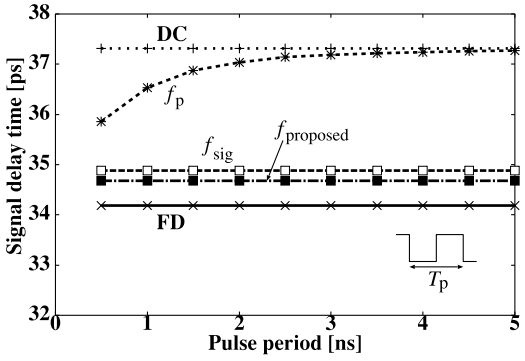

Fig. 14 Delay time when the period of pulse changed.

Table 2 Maximum errors when the period of input pulse changed.

Extraction Freq.	DC	$f_{\rm p}$	$f_{\rm proposed}$	$f_{\rm sig}$
Error in $V_{\rm pp}$	+9.0%	+9.0%	−1.7%	−11.5%
Error in Delay	+9.1%	+9.1%	+2.0%	+1.4%

DC, $f_{\rm proposed}$ and $f_{\rm sig}$ are almost constant when the pulse period is changed. The proposed method achieves the most accurate modeling and its error is within 2%. The error of $f_{\rm p}$ get close to the error of DC as the period become large. This is because the pulse frequency $f_{\rm p}$ becomes lower as the period becomes larger.

The maximum errors are listed in Table 2. From Table 2, the maximum errors when using $f_{\rm proposed}$ is 2% both in the peak-to-peak voltage and in the delay time. The maximum errors of DC and $f_{\rm p}$ is the same, and their errors are about 10% in peak-to-peak voltage and signal delay. The ladder extracted at $f_{\rm sig}$ achieves the smallest error in signal delay, but the error in peak-to-peak voltage exceeds 10%.

The similar results are observed even if the duty ratio of input pulse is varied from 10% to 50%. Then the maximum error of $f_{\rm proposed}$ is about 3% both in the peak-to-peak voltage and in the delay time.

We here show one example of the typical waveforms at the aggressor and the victim. The figures are results when the pulse period $T_{\rm p}$ is 5ns. In this case, the ladder extracted at DC and that extracted at $f_{\rm p}$ product almost same results. Figure 15 shows the waveform at the far-end of the aggres-

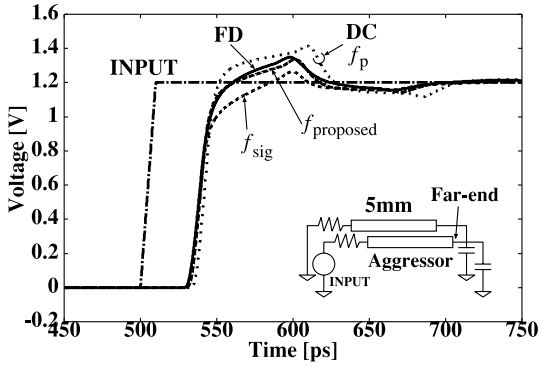

Fig. 15 The waveform at the far-end of the aggressor.

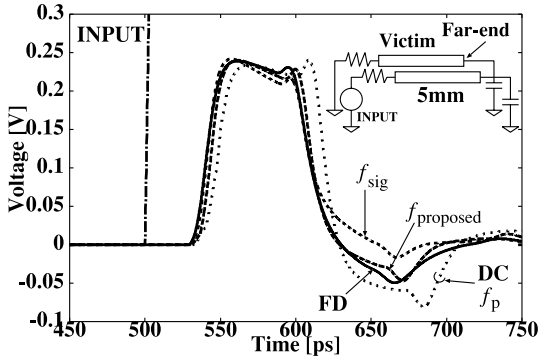

Fig. 16 The waveform at the far-end of the victim.

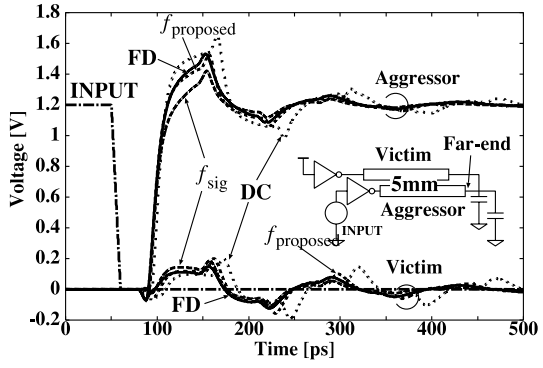

Fig. 17 The waveform driven by transistors. (Transistor $W/L = 720$)

sor interconnect. From Fig. 15, the overshoot is overestimated on the ladder extracted ad DC, and is underestimated on the ladder extracted at $f_{\rm sig}$. From viewpoint of the signal delay, we can see that DC overestimate the delay time. Figure 16 shows the waveform at the far-end of the victim interconnect. From the observation of waveforms, the equivalent circuit extracted at $f_{\rm proposed}$ is most accurate to the frequency-dependent model.

As a more realistic case, we evaluate the interconnect driven by MOS transistors. The waveforms at the far-ends of aggressor and victim are shown in Fig. 17. We use transistor model of 130 nm technology and the W/L value of driver is 720. From Fig. 17, DC extraction overestimates overshoot,

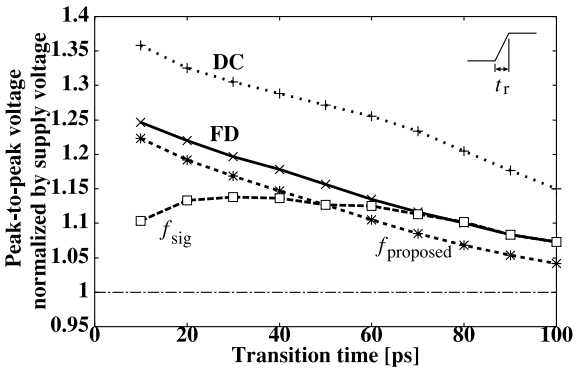

Fig. 18 Voltage peak-to-peak when the transition time is changed.

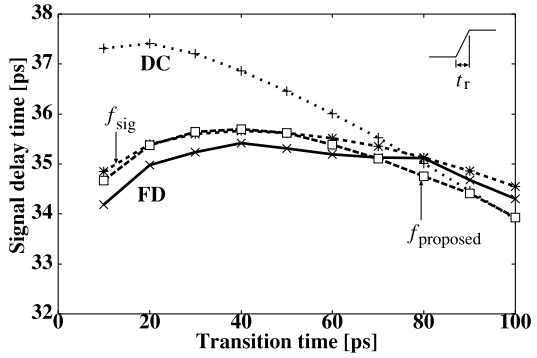

Fig. 19 Delay time when the transition time is changed.

delay and crosstalk. In contrast, $f_{\rm sig}$ extraction underestimates them. $f_{\rm proposed}$ extraction achieves the most accurate modeling even when the interconnect is driven by transistors.

4.3 Transition Time vs. Accuracy

We here show the results when transition time is changed. Significant frequency $f_{\rm sig}$ is decided by transition time. When transition time $t_{\rm r}$ is 10 ps, $f_{\rm sig}$ is 34 GHz and when $t_{\rm r}$ 100 ps, $f_{\rm sig}$ becomes 3.4 GHz. Figure 18 and Fig. 19 show the errors in the peak-to-peak voltage and delay time. The simulation condition is the same as Sect. 4.2. The error in crosstalk noise is also shown in Fig. 20. Table 3 shows the maximum errors when the transition time varied. From Fig. 18, extraction at DC causes about 9% error constantly in the peak-to-peak voltage. The extraction at $f_{\rm sig}$ cause over 10% error when the transition time is small. Significant frequency $f_{\rm sig}$ becomes extremely high when transition time is small. Therefore attenuation on interconnect is overestimated. From Fig. 19, the ladder extracted at DC causes about 9% error in the delay time. DC extraction overestimate the inductance value, so the velocity of signal is underestimated. Therefore delay time is overestimated especially when transition time is small. The extraction at $f_{\rm proposed}$ achieves less than 3% errors in the peak-to-peak voltage and the delay time. From Fig. 20, there is the same trend as the peak-to-peak voltage in the amplitude of crosstalk noise.

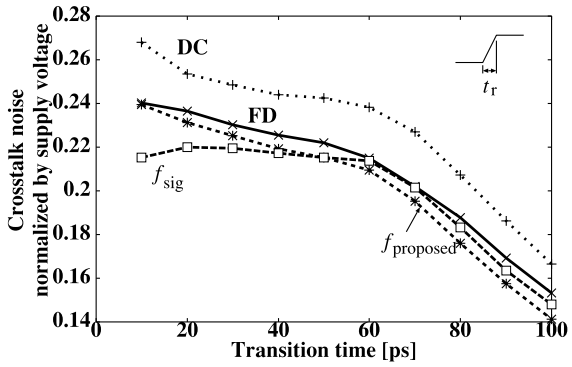

Fig. 20 Crosstalk noise peak-to-peak when the transition time changed.

Table 3 Maximum errors when the transition time changed.

Extraction Freq.	DC	$f_{\rm proposed}$	$f_{\rm sig}$
Error in $V_{\rm pp}$	$+9.0\%$	-3.0%	-11.5%
Error in Delay	$+9.2\%$	$+1.9\%$	-1.2%
Error in $V_{\rm noise}$	$+11.8\%$	-7.9%	-10.4%

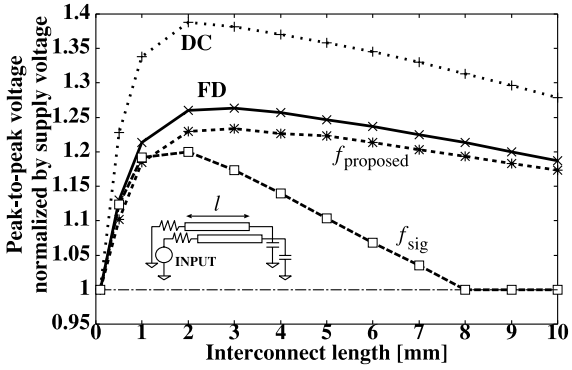

Fig. 21 Voltage peak-to-peak when the interconnect length changed.

DC extraction causes error constantly and $f_{\rm sig}$ causes remarkable error when the transition time is small. As seen in Table 3, DC extraction causes about 10% overestimation in $V_{\rm pp}$, delay and $V_{\rm noise}$. Resistance and inductance extraction at $f_{\rm sig}$ causes over 10% underestimation in $V_{\rm pp}$ and $V_{\rm noise}$. The ladder extracted at $f_{\rm proposed}$ steadily provides the most accurate estimation, and the maximum error is about 8%.

4.4 Interconnect Length vs. Accuracy

Here, the accuracy versus the interconnect length is discussed. Frequency $f_{\rm proposed}$ depends on the interconnect length and the wave velocity. The wave velocity is determined by relative permittivity. Therefore we can assume that the velocity is constant in the same technology. The peak-to-peak voltage error is shown in Fig. 21, and the delay time error is shown in Fig. 22. Figure 23 shows the delay time normalized by the delay time of FD model. Figure 24 shows the amplitude of the crosstalk noise. The simulation condition is the same as Sect. 4.2. As seen in Fig. 21, the ladder extracted at $f_{\rm proposed}$ achieves the minimum error in peak-to-peak voltage. DC extraction always overestimates

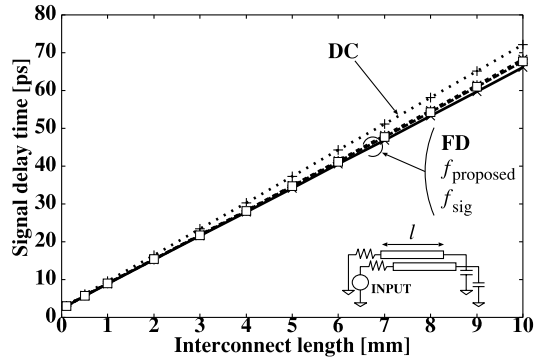

Fig. 22 Delay time when the interconnect length changed.

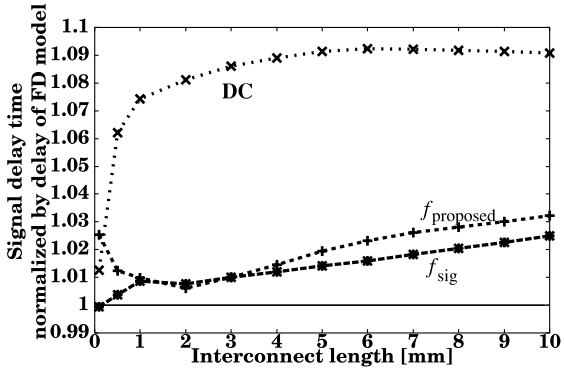

Fig. 23 Normalized delay time when the interconnect length changed.

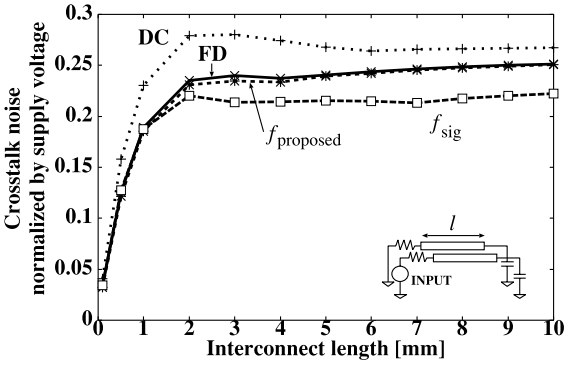

Fig. 24 Crosstalk noise peak-to-peak when the interconnect length changed.

the $V_{\rm pp}$, and $f_{\rm sig}$ extraction causes underestimation when the interconnect length becomes long. As shown in Fig. 22 and Fig. 23, DC extraction causes about 10% error when the interconnect length becomes long. The errors of $f_{\rm proposed}$ and $f_{\rm sig}$ extraction are almost same and below 4%. From Fig. 24, crosstalk noise becomes larger as the interconnect length becomes long in the region where the interconnect length is small. The noise amplitude is almost constant when the length is more than 2 mm. Figure 24 shows that DC extraction causes overestimation and $f_{\rm sig}$ causes underestimation of the crosstalk noise.

The maximum errors are listed in Table 4. As you see,

Table 4 Maximum errors when the interconnect length changed.

Extraction Freq.	DC	f_{proposed}	f_{sig}
Error in V_{pp}	$+10.2\%$	-2.4%	-15.7%
Error in Delay	$+9.1\%$	$+3.2\%$	$+2.5\%$
Error in V_{noise}	$+18.7\%$	-1.8%	-11.3%

Table 5 Maximum errors in overall experiments.

Extraction Freq.	DC	f_{proposed}	f_{sig}
Error in V_{pp}	$+22.5\%$	-4.6%	-28.0%
Error in Delay	$+27.0\%$	$+4.8\%$	$+23.0\%$
Error in V_{noise}	$+37.4\%$	$+7.9\%$	-18.2%

DC and f_{sig} may cause over 10% errors but the maximum error of f_{proposed} is about 3%. These results indicates the ladder extracted at f_{proposed} is robust against the change of the interconnect length.

4.5 Results of Overall Experiments

In the above sections, we show that the frequency calculated from time-of-flight f_{proposed} achieves the most accurate analysis. Table 5 shows the maximum errors in all of results we evaluate. We carefully choose the experimental conditions and hence the effectiveness of the proposed frequency is comprehensively confirmed. The amount of conditions is about 14,000. The ladder extracted DC or f_{sig} causes errors beyond 20%. When wide micro-strip interconnect is driven by strong driver, DC and f_{sig} tend to cause large error. As you see, the proposed frequency f_{proposed} achieves the error below 8%. The above discussions prove that the ladder extracted at the proposed frequency f_{proposed} provides the most accurate modeling of frequency-dependent interconnects.

5. Tolerance to Extraction Frequency Variation

We here discuss the effect of f_{proposed} estimation error on modeling accuracy. The proposed frequency is based on transmission-line resonator theory. As mentioned in Sect. 3.3, the proposed method assumes that transmission-lines have ideal open-end. However in real chips, interconnects are terminated by input capacitor of the receiver and, rigidly speaking, the sink is not ideal open-end. The resonance frequency is not equal to f_{proposed} exactly, but the difference is usually quite small because input capacitor of CMOS receiver is small.

Figure 25 shows the extraction frequency versus errors. X-axis is the extraction frequency and Y-axis is the error from frequency-dependent model. The experimental setup is the same as that of Fig. 15, 5 mm wire length and 10 ps transition time. The proposed frequency f_{proposed} is 7.5 GHz. As shown in Fig. 25, the errors in V_{pp} and in V_{noise} become minimum at the proposed frequency. The error in delay becomes minimum at about 20 GHz, but the error is almost constant above 10 GHz. From Fig. 25, the errors are below 2% in the region of $f_{\mathrm{proposed}} \pm 30\%$. This result indicates that the proposed method is accurate enough even

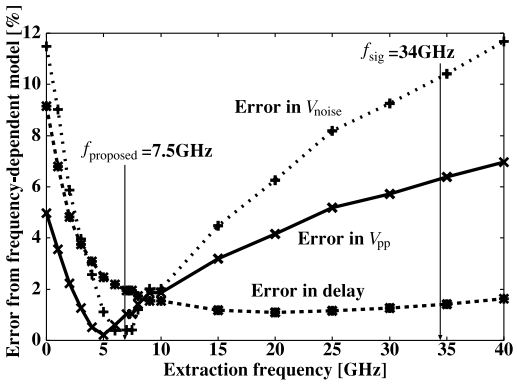

Fig. 25 Extraction frequency vs. errors.

if the proposed frequency has a certain error in comparison with the exact resonance frequency.

We can also see that extraction at DC and significant frequency $f_{\mathrm{sig}} = 34$ GHz is far from the frequency with the minimum error around f_{proposed}. The errors at DC and significant frequency are above 10% whereas that of the proposed method is below 2%.

6. Conclusion

The frequency that should be used to extract RLC values is discussed. When we use frequency-independent equivalent circuits for circuit design, the extraction frequency must be carefully determined to maximize the fidelity in interconnect characteristics. We propose an RLC extraction scheme that uses the frequency determined by interconnect length. We experimentally verify that the proposed frequency achieves the most accurate estimation in delay time and amplitude of overshoot or undershoot. The maximum error is within 5% in peak-to-peak voltage and delay, and the maximum error in crosstalk is within 8% in our experiments. With the proposed representative frequency, RLC extraction at a single frequency becomes accurate enough to model interconnect characteristics, and hence we can exploit many effective design and analysis techniques developed ignoring frequency-dependence.

Acknowledgement

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