PAPER Special Section on Analog Circuit Techniques and Related Topics

Signal-Dependent Analog-to-Digital Conversion Based on MINIMAX Sampling

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SUMMARY This paper presents an architecture of signal-dependent analog-to-digital converter (ADC) based on MINIMAX sampling scheme that allows achieving high data compression rate and power reduction. The proposed architecture consists of a conventional synchronous ADC, a timer and a peak detector. AD conversion is carried out only when input signal peaks are detected. To improve the accuracy of signal reconstruction, MINIMAX sampling is improved so that multiple points are captured for each peak, and its effectiveness is experimentally confirmed. In addition, power reduction, which is the primary advantage of the proposed signal-dependent ADC, is analytically discussed and then validated with circuit simulations.

key words: *signal-dependent sampling, MINIMAX, peak-detection*

1. Introduction

Conventional synchronous analog-to-digital conversion and digital signal processing algorithms have been widely used in various applications and thoroughly studied. Traditionally, converters sample amplitude of analog signals consecutively at constant time intervals. In this approach, the sampling rate is determined by the maximal frequency in the signal spectrum. Therefore, for signals with high frequency components yet low activity, the conventional sampling is not power-efficient due to high constant sampling rate.

For many applications with limited memory recourses and strict power consumption requirements, such as sensing applications, alternative signal-dependent sampling schemes have been explored [1]–[5]. Use of non-uniform sampling provides various advantages for data acquisition, e.g. reduced number of samples (data compression), absence of aliasing, etc. However, it often suffers from difficulty of accurate signal reconstruction due to its high computational complexity [7]. A well-known signal-dependent sampling is level-crossing scheme [1]. In level crossing ADC, sampling occurs when the signal crosses predefined threshold levels. As a result, non-uniformly spaced samples, whose local sampling density depends on the signal local properties, are obtained. This scheme requires at least two constantly operating comparators and a reference voltage circuit, which contributes to power consumption [2].

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Another signal-dependent sampling approach, MINIMAX sampling, which captures a sample every time an analog signal reaches its local maximum or minimum value, is proposed in [6]. The voltage amplitude of the sample is quantized and the time elapsed after the previous sample is measured by a local timer. MINIMAX sampling naturally adjusts sampling frequency depending on input signal activity. In fact, [6] reported that MINIMAX sampling scheme provides relatively high data compression rate and high reconstruction precision compared to level-crossing scheme. However, no physical implementation has been presented.

In this paper, we propose a power-efficient and signal reconstruction-friendly implementation of MINIMAX ADC consisting of a peak detector, a timer and an amplitude quantizer circuit. Power consumption is reduced by storing an analog signal at discrete time intervals and performing AD conversion for the stored signal only when a signal peak is detected. Such discretely sampled signal is highly compatible with traditional signal processing algorithms since peak samples are inherently located on a uniform grid and only missing samples on the grid need to be reconstructed. We further improve this architecture to enhance reconstruction accuracy by capturing multiple samples per peak, which reduces necessity of precise peak detection. In addition, we analytically evaluate the power reduction of the proposed implementation, and experimentally validate the derived relation through 180 nm circuit simulation.

The remainder of this paper is organized as follows: Sect. 2 presents the proposed architecture of MINIMAX ADC. Section 3 describes reduction of number of samples and an improved MINIMAX sampling to enhance the accuracy of signal reconstruction. In Sect. 4, an analytical discussion on reconstruction error for 1-point and 3-point MINIMAX samplings is given. Section 5 analytically discusses dependence of power dissipation on active ratio of analog input signal, and Sect. 6 experimentally confirms power reduction compared with conventional synchronous ADC. Section 7 concludes the discussion.

2. Basic ADC Architecture

Figure 1 shows the architecture of the proposed ADC for MINIMAX sampling composed of a peak detector, a discrete timer and an amplitude quantizer circuit. The peak detector finds peaks of a given analog input voltage V_{analog}, and gives triggers *trig* to amplitude quantizer circuit and

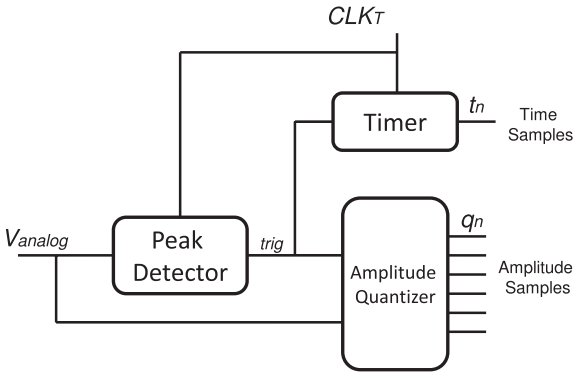

Fig. 1 Structure of MINIMAX ADC.

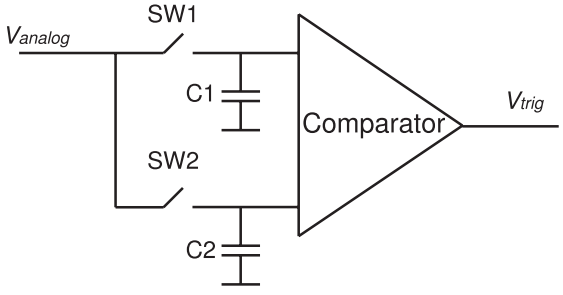

Fig. 2 Switched-capacitor peak detector.

timer. The key circuit of MINIMAX ADC is the peak detector, which enables signal-dependent sampling. The timer is driven by a timer clock CLK_T, which attains higher compatibility with traditional signal processing algorithms, since all samples are located on the grid of CLK_T. For the MINIMAX ADC, precision of peak detection is one of the important points that characterize the overall performance, which will be discussed in Sect. 4.

A possible implementation of peak detector is shown in Fig. 2. It consists of a comparator, two capacitors and two switches. These pairs of capacitor and switch work as sample-and-hold circuits for storing previous and current amplitude values of V_{analog} for comparison. In this configuration, when a peak occurs, the comparator generates a transition, which triggers the amplitude quantizer and makes the timer count the time between two adjacent peaks. In addition, to reduce DC power that is often dissipated by analog bias current, clocked comparator [2], [9], [10] is desirable and used in this work.

On the other hand, conventional synchronous ADC can be used as an amplitude quantizer. This ADC works only when peaks are detected, and hence an implementation with less static power consumption is desirable. For that purpose, Successive Approximation (SA) ADC [9] with clocked comparator [2] was selected in this work.

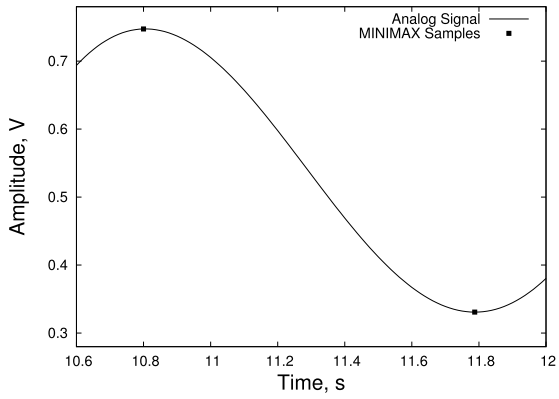

Fig. 3 1-point MINIMAX sampling.

3. MINIMAX Sampling

3.1 1-Point MINIMAX Sampling and Signal Reconstruction

Figure 3 illustrates an example of "1-point MINIMAX sampling", which was proposed and called "MINIMAX sampling" in [6]. The name "1-point" comes from the fact that one sample is captured for each peak. One of the advantages of MINIMAX sampling is the ability to reconstruct an analog signal from reduced number of samples. Reference [6] reported that it is theoretically possible to reconstruct an analog signal from MINIMAX samples with relatively high precision if the exact timings of the peaks are known. However, the signal reconstruction from non-uniform peak samples is computationally expensive, and [6] presented an iterative reconstruction algorithm. Furthermore, precise peak detection, assumed in [6], is a challenging task in terms of hardware implementation, since a continuous timer is practically infeasible and a digital timer driven by a high frequency consumes large power and area and requires large storage to store time information. On the other hand, with this implementation, signal reconstruction becomes more straightforward since samples generated by proposed MINIMAX ADC are located on uniform grid of CLK_T and no iterative reconstruction algorithms are necessary.

For MINIMAX sampling, there are two factors that degrade sampled signal quality — quantization error and reconstruction error. The quantization error comes from amplitude and time discretization, and the conventional synchronous ADC has the same error. The additional error is the reconstruction error introduced when missing non-peak samples are reconstructed from the peak samples. In this paper, piecewise cubic Hermite interpolation (PCHIP) [13] is used for signal reconstruction. This interpolation method does not include excessive variation between data points and provides good reconstruction results processing MINIMAX samples, compared to, such as, polynomial interpolation [13]. On the other hand, the reconstruction accuracy may change depending on the class of input signals, and in some

Table 1 Comparison in # samples and MSE.

Sampling	# of samples	ε (V^2)
Conventional (44 kHz)	1.6M	-
MINIMAX (δ = 0.01 V)	160k	0.0021
MINIMAX (δ = 0.06 V)	80k	0.0054
Conventional (4 kHz)	160k	0.0051

cases, other reconstruction methods could be necessary.

Table 1 lists a comparison of conventional synchronous and 1-point MINIMAX sampling schemes in processing an audio signal. The timer frequency for 1-point MINIMAX sampling was 44 kHz. Here, a short male speech signal was chosen, because it consists of active regions and pauses, which is the property that signal-dependent sampling scheme exploits. The peak-to-peak amplitude of the given signal is 1.6 V, and the bandwidth is up to 4 kHz. MSE (Mean Squared Error), ε, is defined as:

$$\varepsilon = \frac{1}{n_s}\sum_{i=1}^{n_s}(s_i - \widehat{s_i})^2, \tag{1}$$

where s_i and $\widehat{s_i}$ are original and reconstructed signals at the i-th timing and n_s is number of samples. Note that after signal reconstruction, n_s is the same for all the sampling schemes.

The sensitivity of peak detection is expressed as a parameter δ, which represents how large the difference in voltage amplitude is necessary between successive timer timings for peak detection. It is associated with the comparator performance in the peak detector. At low δ values even small variations of analog signal can be detected, but it will increase the number of acquired samples.

1-point MINIMAX approach with δ = 0.01V produces 160k samples, whereas conventional sampling scheme at 44 kHz sampling frequency produces 1.6M samples. After reconstructing this signal using PCHIP, the introduced MSE error is 0.0021 V^2, although the number of samples is reduced by 90%. The same number of samples could be achieved by down-sampling. However, the reconstruction of down-sampled signal would lead to 2.4 times higher error (0.0051 V^2). On the other hand, it would be possible to achieve similar error (0.0054 V^2) by using MINIMAX approach with δ = 0.06 V. In this case, the number of samples is reduced to 80k indeed.

The simplified implementation of SAR ADC used in 1-point MINIMAX ADC, based on charge-redistribution DAC [9], is shown in Fig. 4 (only 3-bit ADC is exemplified) and its timing diagram is presented in Fig. 5. Assuming that a sample of analog signal $S0$ was previously sampled, the next sample $S1$ will be sampled to capacitor C1 of the peak detector through switch SW1 (Fig. 2) and also to capacitor array C_{MSB1} of the SAR ADC through SW3 (Fig. 4). The following sample $S2$ will be sampled to C2 through SW2 and also to C_{MSB2} through SW4. When the difference between two adjacent samples changes its sign, the comparator will generate V_{trig} signal. After that, switch SW5 will be turned on, which will trigger the charge-redistributional

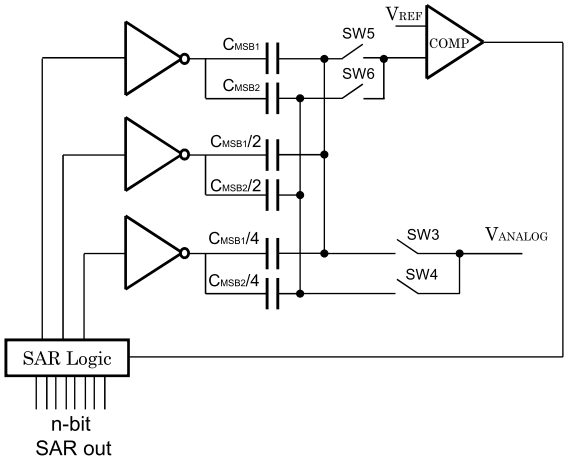

Fig. 4 Structure on 1-point MINIMAX SAR ADC.

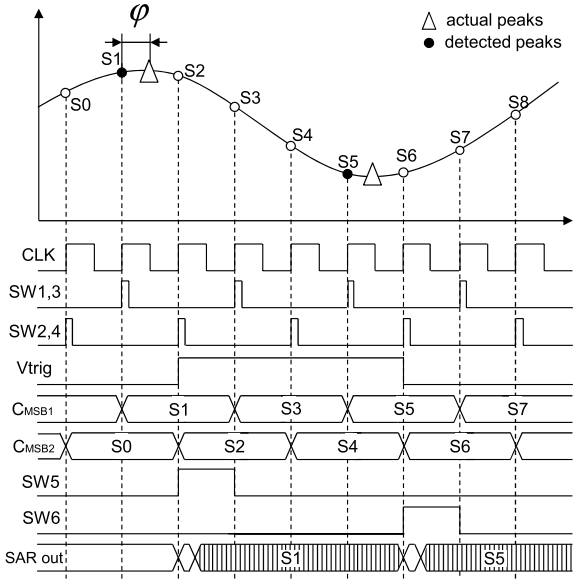

Fig. 5 Timing diagram of 1-point MINIMAX ADC.

conversion of the sample $S1$ using simple digital inverters. The digitally represented voltage of sample $S1$ will appear at the output of SAR logic after the conversion finishes.

Figure 5 also shows the phase shift φ that correspond to time difference between actual (Δ) and detected ($\bullet$) peaks. The impact of the phase shift on reconstruction precision will be discussed in Sect. 4.

3.2 3-Point MINIMAX Sampling

Processing signals in the real world, it is hard to guarantee that clock edges are aligned at the peaks of analog signal unless infinitely high clock frequency is used. Therefore, in 1-point MINIMAX sampling, errors always exist due to misalignment of actual and detected peaks. In order to reduce the reconstruction error even with presence of phase shift, we propose an alternative approach that samples multiple points around a peak, instead of one, to improve recon-

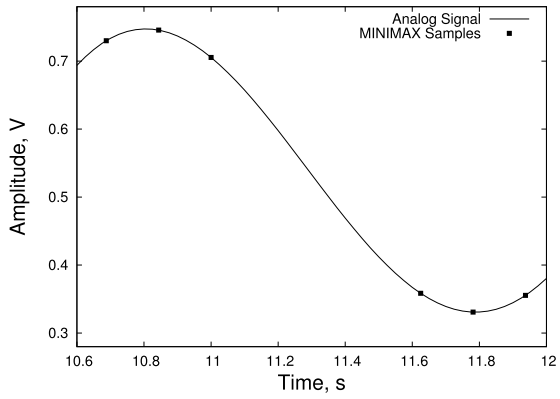

Fig. 6 3-point MINIMAX sampling.

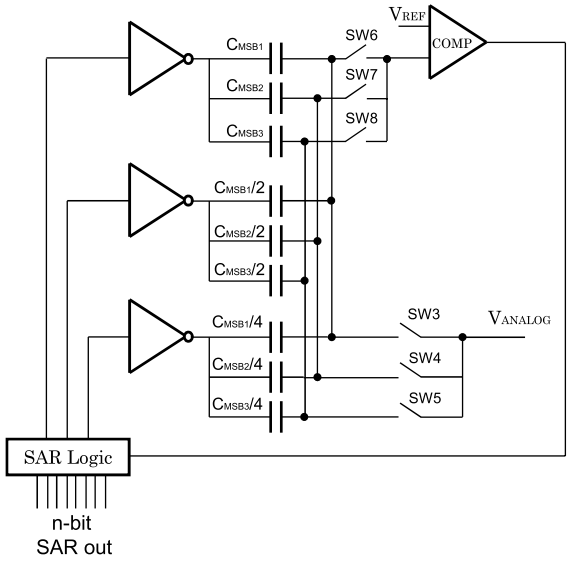

Fig. 7 Structure on 3-point MINIMAX SAR ADC.

struction accuracy by mitigating uncertainty of peak timings (Fig. 6). In the proposed sampling scheme, named 3-point MINIMAX, three points, which are ones before/at/after the peak detection, are stored in capacitors C_{MSB1}, C_{MSB2} and C_{MSB3} (Fig. 7). The peak detector works in the same way as in the case of 1-point MINIMAX sampling. The only difference is that SAR ADC used for 3-point sampling has one extra sample-and-hold circuit which consists of capacitors C_{MSB3}, SW5 and SW8 and three samples are converted instead of one after peak detection (Fig. 8).

Figure 9 shows an example that a chirp signal ($f_{high} = f_t/10$, $f_{low} = f_t/100$) with amplitude modulation ($f_c = f_t/100$) was sampled, where f_t is the timer frequency. Figure 9 also shows the signal reconstructed from the samples using PCHIP. The MSE for this signal is 0.22 mV. We can see that 3-point sampling and signal reconstruction work well. MINIMAX ADC is capable of sampling modulated signals if the timer frequency is at least 10 times higher than the frequency of the highest harmonic of analog signal. This timer frequency will be discussed in association with signal

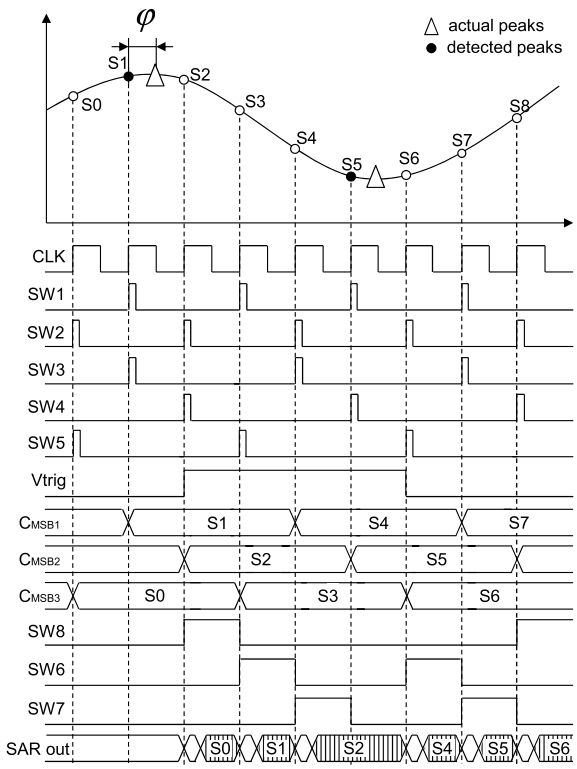

Fig. 8 Timing diagram of 3-point MINIMAX ADC.

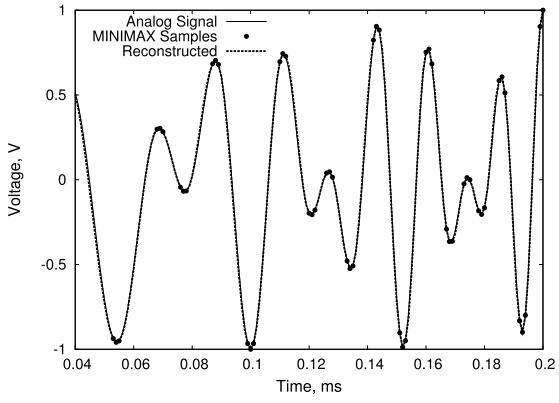

Fig. 9 Modulated signal sampled using 3-point MINIMAX ADC.

reconstruction error in the next section.

4. Discussion on Signal Reconstruction Error

If an analog signal is sampled at a certain non-infinite sampling frequency, any actual peaks of the signal occurred between clock edges will not be detected. Instead, the peak sample will be approximated to the nearest discreet sample with the highest/lowest amplitude.

This section discusses reconstruction error for 1-point and 3-point MINIMAX samplings to clarify the accuracy improvement thanks to 3-point sampling. For an illustration purpose, sampling for a sine signal is assumed in this section.

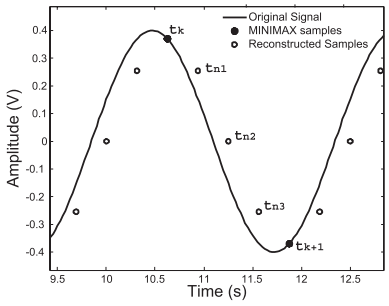

Fig. 10 Temporal misalignment of peaks due to a discrete timer for 1-point MINIMAX sampling (F=8).

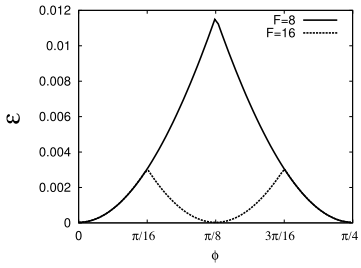

Fig. 11 Phase shift impact on reconstruction error using 1-point MINIMAX sampling.

4.1 1-Point MINIMAX Sampling

Figure 10 shows a sine signal sampled with 8 times higher sampling frequency and clock signal shifted by $\varphi = \frac{\pi}{8}$. Since both minimum and maximum peaks occurred between the clock edges, the peak samples were approximated to t_k and t_{k+1}. This contributes to increase in reconstruction error since the reconstructed points between the peaks, t_{n1}, t_{n2} and t_{n3} do not closely correlated with the original signal. The following analytically discusses this reconstruction error.

In order to understand the impact of clock phase shift on reconstruction precision, we firstly estimate the location of the maximum and minimum peaks analytically with phase shift as one of the parameters. Then, the original signal is reconstructed with various phase shift values to find the worst case scenario for 1-point MINIMAX sampling scheme.

Suppose 1-point MINIMAX sampling is applied to a signal $s(t) = A\sin(2\pi f_s t + \varphi)$. Then the samples are at the maximum and minimum peaks of the signal if:

$$MAX : \sin(2\pi f_s t+\varphi)=1 \Longrightarrow 2\pi f_s t+\varphi=\frac{\pi}{2}+2\pi n, \quad (2)$$

$$MIN : \sin(2\pi f_s t+\varphi)=-1 \Longrightarrow 2\pi f_s t+\varphi=\frac{3\pi}{2}+2\pi n, \quad (3)$$

where f_s is signal frequency and n is integer. Therefore, the locations of maximum and minimum peaks are expressed by:

$$t_{MAX} = \frac{\frac{\pi}{2} + 2n\pi - \varphi}{2\pi f_s}, \quad (4)$$

and

$$t_{MIN} = \frac{\frac{3\pi}{2} + 2n\pi - \varphi}{2\pi f_s}, \quad (5)$$

for $-\frac{\pi}{F} < \varphi < \frac{\pi}{F}$. Here F is defined as:

$$F = \frac{f_t}{f_s}, \quad (6)$$

where f_t is the timer frequency that determines the minimum time interval between samples. f_s is analog signal frequency.

Given sets of time and amplitude $[t_k, y_k]$ corresponding to peak samples, the signal waveform between adjacent peaks, i.e. $t_k < t < t_{k+1}$, $P(t)$ is reproduced by piecewise cubic Hermitian interpolation as follows [13]:

$$P(t) = y_k + (t - t_k)d_k + (t - t_k)^2 c_k + (t - t_k)^3 b_k, \quad (7)$$

where d_k denotes the slope of $P(t)$ at the peak:

$$d_k = P'(t_k), \quad (8)$$

and the coefficients of the quadratic and cubic terms are:

$$c_k = \frac{3\delta_k - 2d_k - d_{k+1}}{t_{k+1} - t_k}, \quad (9)$$

$$b_k = \frac{d_k - 2\delta_k + d_{k+1}}{(t_{k+1} - t_k)^2}, \quad (10)$$

where

$$\delta_k = \frac{y_{k+1} - y_k}{t_{k+1} - t_k}. \quad (11)$$

The derivative value d_k is approximately calculated as a weighted harmonic mean, where weights are determined by the lengths of the two intervals:

$$d_k = \frac{w_1 + w_2}{\frac{w_1}{\delta_{k-1}} + \frac{w_2}{\delta_k}}, \quad (12)$$

where $w_1 = 2h_k + h_{k-1}$, $w_2 = h_k + 2h_{k-1}$ and $h_k = t_{k+1} - t_k$.

In case of 1-point MINIMAX sampling, the calculation of the slopes is simple and $d_k = 0$ because the derivatives at peaks should be zero. Therefore, interpolant that reproduces the points between two peaks can be calculated as follows:

$$P(t)=y_k+(t-t_k)^2\frac{3\delta_k}{t_{k+1}-t_k}-(t-t_k)^3\frac{2\delta_k}{(t_{k+1}-t_k)^2}. \quad (13)$$

Figure 11 shows how phase shift affects the reconstruction error at two different sampling frequencies. It is obvious that at low timer frequencies, it will be difficult to detect the timings of peaks precisely. Use of higher timer frequency, in contrast, leads to more precise peak detection, but increases power consumption of the system.

4.2 3-Point MINIMAX Sampling

The location of maximum and minimum peaks for 3-point sampling can be calculated using Eq. (4) and Eq. (5). The

other two points, which are before and after the peaks, can be found using:

$$t_{MAX\pm1} = t_{MAX} \pm \frac{1}{f_t}, \tag{14}$$

$$t_{MIN\pm1} = t_{MIN} \pm \frac{1}{f_t}. \tag{15}$$

Similarly to 1-point sampling, the waveform reproduced from 3-point MINIMAX sampling is represented by Eq. (7). On the other hand, the slopes d_k need to be calculated using Eq. (12), since not all of them are equal to zero in contrast to 1-point sampling.

Figure 11 shows the reconstructed samples when $\varphi = \frac{\pi}{16}$. We can see that the reconstructed samples are close to the original signal. An important factor of 3-point MINIMAX sampling is that when reproducing missing samples t_{n1} to t_{n5} in Fig. 11, the signal between t_{k+2} and t_{k+3} is monotonically changing and is easy to interpolate. In other words, an actual peak must exist between t_k and t_{k+2} and its position between t_k and t_{k+2} becomes less important. On the other hand, in the case of 1-point sampling, the signal between t_k and t_{k+1} in Fig. 9 is not monotonically changing and then difficult to reproduce such non-monotonicity from samples.

Figure 12 shows the reconstruction error of missing samples in case of 3-point sampling. Compared to Fig. 10 of 1-point sampling, the error is two orders of magnitude smaller. The error is still dependent on φ, but the impact is much suppressed. On the other hand, opposite to 1-points sampling, increasing sampling frequency f_t would increase reconstruction error (Fig. 13), since higher f_t makes three samples t_k, t_{k+1} and t_{k+2} in Fig. 11 closer to each other. In this case, 3-point sampling gradually loses the advantage over 1-point sampling and approaches to 1-point sampling.

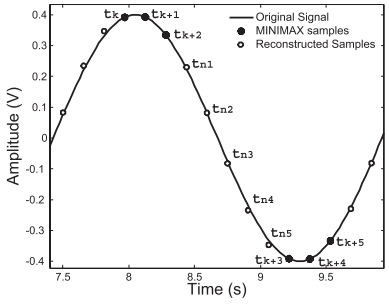

Fig. 12 Temporal misalignment of peaks due to a discrete timer for 3-point MINIMAX sampling.

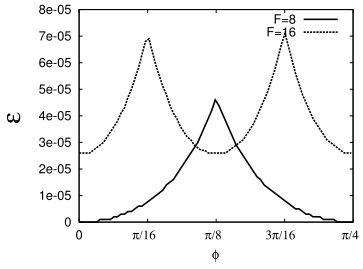

Fig. 13 Phase shift impact on reconstruction error using 3-point MINIMAX sampling.

4.3 Discussion

Figure 14 shows how MSE of the reconstructed signal depends on the ratio F (Eq. (6)) at the maximal phase shift. Quantization error due to sampling is not included here.

It can be seen that, for 1-point sampling, the MSE decreases as the timer frequency increases. As for 3-point sampling, the error is lower compared to 1-point case and it is relatively stable for all F values, which indicates that high timer frequency is not necessary. This contributes to power-efficient implementation, because power dissipation associated with clocking can be suppressed.

We further investigate MSE of 3-point MINIMAX sampling comparing to conventional synchronous sampling. For synchronous sampling f_t in Eq. (6) is the sampling frequency. Besides, it is well known that Nyquist−Shannon sampling theorem guarantees a perfect signal reconstruction if $F \geq 2$. On the other hand, the theorem requires samples for infinite time for the perfect reconstruction, and obviously this requirement cannot be satisfied in real applications. We, therefore, adopted a popular signal reconstruction that interpolates finite samples with sinc function [14], which means the reconstruction error is not zero even while Nyquist−Shannon sampling theorem is satisfied. Then, the signals reconstructed from both conventional synchronous sampling and 3-point MINIMAX sampling were resampled at 20x higher frequency than the signal frequency, and their MSEs were evaluated.

Figure 15 shows the comparison between MSEs of synchronous sampling and 3-point MINIMAX sampling. MSE of synchronous sampling decreases significantly, as F increases. On the other hand, in energy or memory constrained applications, the value $F \approx 2$ is often used. For small F values, MSE of MINIMAX sampling is very close to the one of synchronous sampling because few samples are eliminated during MINIMAX sampling. For higher F values ($F > 6$), more samples between peaks have to be restored which may cause increase in reconstruction error.

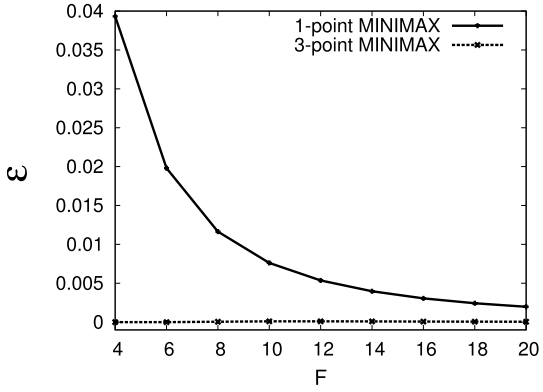

Fig. 14 MSE error dependence on ratio of sampling frequency to signal frequency.

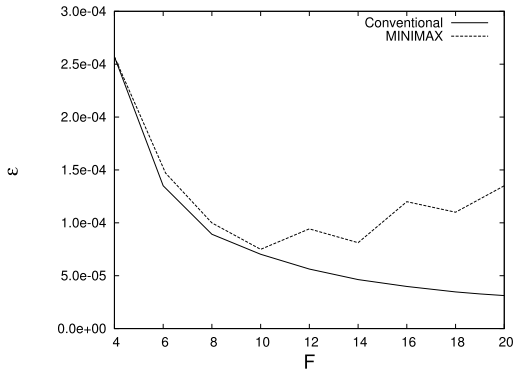

Fig. 15 Comparison of reconstruction errors.

However, MSE remains almost unchanged. In fact, for $F = 10$, the error of signal sampled using 3-point MINIMAX sampling is only 6% higher compared to the signal sampled traditionally. This means that although MINIMAX sampling requires signal reconstruction between peaks, the error originating from such signal reconstruction is on the same order of conventional synchronous sampling. Therefore, it can be concluded that MINIMAX sampling allows achieving data compression with relatively precise reconstruction precision.

Lastly, the complexity of PCHIP for signal reconstruction is discussed below. PCHIP method uses cubic interpolants, which are relatively easy to compute (Eq. (7)), and does not require iterations nor calculation of window functions, e.g. SINC interpolation. It estimates the individual slopes using only three neighboring points. In fact, to obtain b_k, c_k and d_k in Eq. (7), 5 summation, 5 subtraction, 6 multiplication and 6 division operations are necessary for 3-point sampling, and substituting a value of t for Eq. (7) requires 3 summation, 1 subtraction and 5 multiplication operations. On the other hand, since the proposed ADC is targeted for low power applications, e.g. battery-powered sensors, the signal reconstruction is not expected to be executed at each sensor, but it is often performed at a server after the sensor data transmission. At the server, derivation of coefficients of b_k, c_k and d_k and calculation of the interpolant is much more affordable. For example, the interpolation of 1 kHz analog signal, sampled using MINIMAX ADC, with f_t=10 kHz requires 0.095 second of CPU time to process 1 second long signal. The evaluation was done using MATLAB on a machine with 2.66 GHz CPU.

5. Power Consumption Analysis

We derive and compare analytic expressions of power consumption for conventional synchronous SA-ADC and MINIMAX sampling ADC. In n-bit SA-ADC, comparison is repeated n times for one AD conversion. Then, power consumption of conventional synchronous SA-ADC, P_{conv}, is expressed by

$$P_{conv} = (E_{ADC} + E_{SAR})\cdot f_t \cdot n, \tag{16}$$

where E_{ADC} is the energy per one bit conversion in SA-ADC, E_{SAR} is the energy of Successive Approximation Register (SAR) and f_t is the sampling frequency. In the proposed MINIMAX ADC, the peak detector works at every timer timing. On the other hand, SA-ADC works only when peaks are detected. Therefore, the power dissipation of the proposed MINIMAX ADC, P_{prop}, is expressed by

$$P_{prop} = E_{PD}\cdot f_t + (E_{ADC}+E_{SAR})\cdot m\cdot f_t \cdot n\cdot \alpha + E_t \cdot f_t, \tag{17}$$

where E_{PD} is the energy of peak detector per timer cycle, E_t energy of the timer, α is the ratio of peak detection related to timer frequency and m is number of points per peak. For 3-point MINIMAX sampling, m equals 3 since three samples have to be captured for each peak. At $\alpha = 0\%$, analog input signal is constant, while at $\alpha = 100\%$ the AD conversion is done at every timer period. Using these two expressions, we can estimate the power ratio of the proposed ADC to the conventional ADC:

$$\begin{aligned}\frac{P_{prop}}{P_{conv}} &= \frac{E_{PD}\cdot f_t + (E_{ADC}+E_{SAR})\cdot m\cdot f_t\cdot n\cdot\alpha}{(E_{ADC}+E_{SAR})\cdot f_t\cdot n} \\ &\quad + \frac{E_t\cdot f_t}{(E_{ADC}+E_{SAR})\cdot f_t\cdot n} \\ &= \frac{E_{PD}+E_t}{(E_{ADC}+E_{SAR})\cdot n} + m\cdot\alpha.\end{aligned} \tag{18}$$

From Eq. (18), it is possible to derive the value of α at which the P_{prop} will start to be less that P_{conv}:

$$\alpha <= \frac{1}{m} - \frac{E_{PD}+E_t}{(E_{ADC}+E_{SAR})\cdot n\cdot m}. \tag{19}$$

This expression means that as α becomes small and n becomes large, the advantage of the proposed ADC increases. It can be seen that, theoretically, the value of α cannot be more that 33% for 3-point MINIMAX ADC to be more power-efficient than conventional ADC if $F \geq 6$. When $F < 6$, m becomes smaller than 3, since some samples are shared by two peaks. In addition, the energies of peak detector and timer are the key parameters that affect the efficiency.

6. Simulation Results

This section describes the basic ADC performance and validates the power reduction in Eq. (18) with circuit simulation.

6.1 Experimental Setup and ADC Performance

We implemented the proposed 3-point MINIMAX ADC in 180 nm CMOS technology. The resolution of ADC is 8 bits and supply voltage is 1.8 V. Comparator similar to [2] was adopted for the peak detector circuit and SA-ADC (Fig. 16). With this structure, the comparator consumes power only when CLK signal is high. For a constant duration of CLK being high, the energy needed for a single comparison is constant independent of CLK frequency.

The peak detector was designed assuming 1 Vpp input voltage. The smallest voltage that the peak detector can detect is 100 mV and its offset is 1.8 mV. The maximal delay

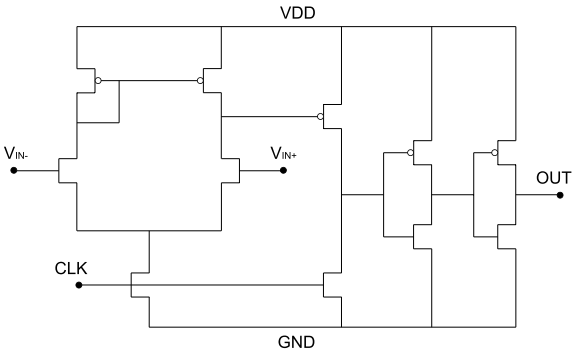

Fig. 16 Schematic of the comparator.

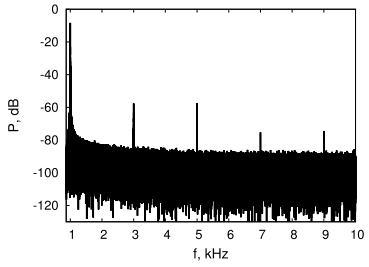

Fig. 17 FFT result of 3-point MINIMAX ADC.

caused by the offset and other non-linearities of the peak detector is 30 ns. Note that this implementation is an example, and if more sensitive peak detector is necessary for the accuracy despite the increased number of samples as discussed in Sect. 3.1, more sophisticated comparator should be used. In contract, to reduce the number of samples for small variation of analog input, the comparator in the peak detector should be less sensitive. This can be achieved by following approaches. A) When a cross coupled latch is added to the decision stage [16], the comparator has a certain amount of hysteresis to reject small and frequent noise-like input signals. In our design experiment, 100 mV hysteresis was obtained with additional 3% power overhead. B) Small signals require longer decision time of comparator. If the width of CLK signal is shorter than the time necessary for the comparator to make a decision, small variations of signal are not detected by the peak detector. Additionally, the power consumption of the peak detector is reduced, since the enabled duration of the comparator becomes shorter. The problem of this approach is that the time needed for the decision depends on the common-voltage level V_{CM}. However, if the swing of the input signal is relatively small and V_{CM} level is carefully selected to guarantee the constant decision time, the peak detector will operate properly. C) When the noise frequency is higher than the signal frequency of the interest, such high-frequency noise could be filtered using low-pass filter.

Fast Fourier transform (FFT) output spectrum for 1 kHz input signal with sampling rate of 10 kHz and 1.8 supply voltage is shown in Fig. 17. This FFT was performed after missing samples were reconstructed by PCHIP.

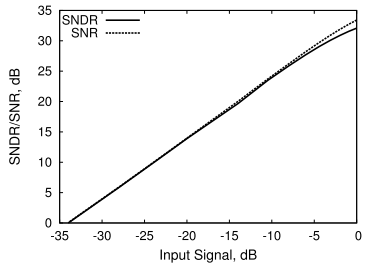

Fig. 18 Signal to noise and distortion ratio versus input level (3-point MINIMAX ADC).

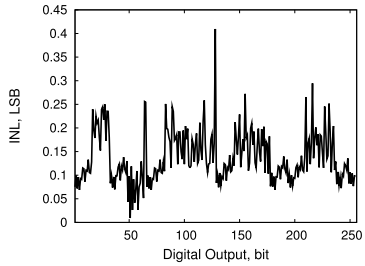

Fig. 19 Integral nonlinearity (INL) of 3-point MINIMAX ADC.

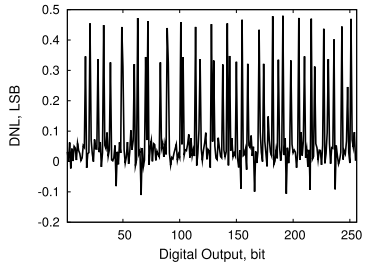

Fig. 20 Differential nonlinearity (DNL) of 3-point MINIMAX ADC.

The spurious free dynamic range (SFDR) of 3-point MINIMAX ADC is approximately 49 dB and the total signal-to-noise-and-distortion ratio (SNDR) is 34 dB (ENOB = 5.4) for this input frequency. Figure 18 shows the dependency of SNDR/SNR on input signal level. The integral nonlinearity (INL) and differential nonlinearity (DNL) are presented in Figs. 19 and 20, respectively. SNDR of 1-point MINIMAX ADC drops to 32 dB and SFDR to 38 dB due to higher reconstruction error. On the other hand, when the same ADC, which is used in MINIMAX ADC as an amplitude quantizer, samples 1 kHz input signal synchronously with 10 times higher sampling frequency, its SNDR is 35 dB and SFDR is 54 dB. These differences originate from the reconstruction. Conversely, it is expected that the performance of MINIMAX ADC can be improved if a better ADC is used for amplitude quantization.

6.2 Evaluation of Power Consumption

For evaluating power consumption, 2 kHz sine signal with 20 kHz timer frequency was used. To emulate intermittent input signals, we changed the ratio of sine signal and DC

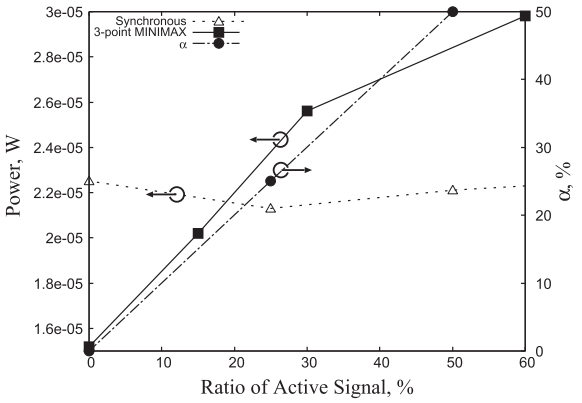

Fig. 21 Simulated power consumption.

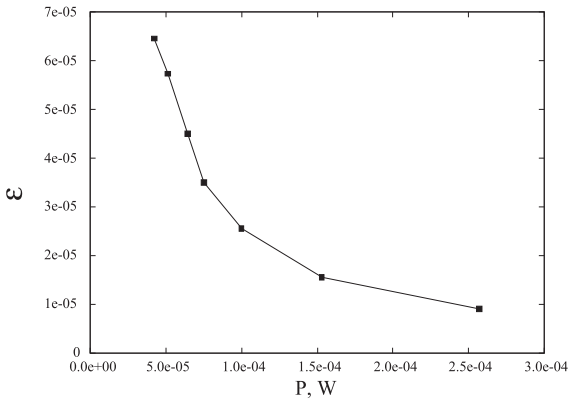

Fig. 22 Power consumption versus MSE.

signal. The power dissipation was estimated by circuit simulation.

Figure 21 shows simulation results of MINIMAX ADC with a peak detector, and demonstrates that its power consumption depends on the activity of input signal. The power dissipation of the synchronous SA-ADC is also shown in Fig. 21. The power dissipation of the synchronous SA-ADC is roughly constant, because AD conversion is carried out every time. When the ratio of active signal is high, conventional synchronous ADC is power-efficient. However, when the ratio of sine waveform is lower than 20%, i.e. α is smaller than 20%, the proposed ADC attains lower power operation. In fact, α of the speech signal used in Table 1 is 10% and the proposed ADC is more efficient than conventional synchronous ADC.

Let us compare the simulation result with the analytical discussion of Eq. (18). In the implemented circuit, the power is consumed only when driven by clock signal, and no DC current flows when clock signal is not given. Note that, strictly speaking, leakage current flows, but its amount is not significant in 180 nm technology. We therefore evaluated E_{PD}, E_{ADC}, E_{SAR} and E_t by measuring power dissipation during a clock cycle in circuit simulation. The obtained values are E_{PD}=15.84 μW/Hz, E_{ADC}=22 μW/Hz, E_{SAR}=0.5 μW/Hz.

The tie-break point is estimated to be 28% by Eq. (18), and close to 20% from the simulation result. It means that the proposed architecture can attain lower power ADC for input signals whose peak ratio is lower than 20∼28% Thus, the discussion in Sect. 5 is validated. The higher tie-break values of α can be achieved by reducing energies of peak detector and timer. In the current implementation, when the ratio is lower than 20%, the proposed ADC attains lower power operation. In speech and also various biomedical signals, e.g. neural spikes with low occurrence rate, the ratio of peaks is often much smaller than 20% [15].

Figure 22 shows the trade-off between power consumption and MSE derived from Fig. 15 and Eq. (17). In this trade-off, timer frequency was swept. We can see that MSE first decreases with small increase in power dissipation. This trade-off is helpful to design a power-efficient system that includes MINIMAX ADC, since the specification of each component needs to be determined for maximizing power-efficiency while the system-level specification, such as signal processing accuracy, is satisfied.

Finally, let us compare power dissipations of MINIMAX ADC and level-crossing ADC. In MINIMAX ADC, when the input signal is constant, only peak detector, which consists of a comparator and two sample-and-hold circuits, is operating. On the other hand, at least 2 comparators will be constantly operating in level-crossing ADC. Therefore, the power consumption of level-crossing ADC is at least twice higher than that of MINIMAX ADC for constant signal. MINIMAX ADC is more power efficient than level-crossing ADC for low-active signals.

7. Conclusion

This paper demonstrated that 3-point MINIMAX sampling approach can be effective for processing signals with low or changing activity while keeping the reconstruction accuracy. This sampling naturally adjusts to input signal activity and allows saving power dissipation during inactive periods of input. The structure of 3-point MINIMAX ADC was proposed with switched-capacitor peak detector circuit. The simulation results confirmed the validity of theoretical power reduction. In our 0.18 μm implementation, when the ratio of peak samples in the given signals is lower than 20∼28%, power reduction can be obtained.

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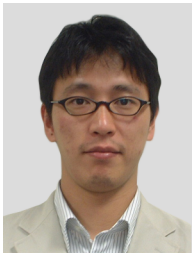

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