Angular Dependency of Neutron-Induced Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM

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Abstract—This paper reports neutron-induced MCU (Multiple Cell Upset) measured in 0.4-V 65-nm 10T SRAM at two incident angles of 0° and 60°. The measurement results show that the ratio of the number of measured MCUs at the angles of 60° to that at 0° is 1.13 in 0.4-V operation, while the ratio of neutrons radiated to the test chip was 50% at 60°. The spatial MCU patterns measured at 60° indicate that forward emission of secondary ions plays an important role to cause the angular dependency in 0.4-V operation. Furthermore, a Monte-Carlo simulation using PHITS (Particle and Heavy Ion Transport code System) was performed to confirm the measured angular dependency of neutron-induced MCUs. The simulation results show that the ratio of the number of MCUs at the angles of 60° to that at 0° is 1.20 and the same tendency of MCU patterns is observed. The measured angular dependency of neutron-induced MCUs is mostly reproduced by the simulated generation and transport of secondary ions.

Index Terms—Angular dependency, multiple cell upset, neutroninduced soft error, PHITS (particle and heavy ion transport code system), subthreshold circuit.

I. INTRODUCTION

CUs (MULTIPLE CELL UPSETs) in SRAMs are a serious concern since MCU-tolerant design techniques at the architecture, logic and device levels necessarily involve area, power, and/or performance overheads depending on the required immunity levels to MCU. Especially in ultra-low-voltage operation as in subthreshold circuits, increased MCU occurrence rate and MCU multiplicity [1], which means the number of cells flip at once, may cause errors even when conventional redundant techniques for SRAMs are employed at nominal voltages. We need to account for the occurrence probabilities of MCU and MCU multiplicity to ensure that SRAMs have necessary and sufficient immunity to MCU with the minimum overhead.

A lot of real-time and accelerated neutron radiation tests and device-level simulations have been performed with the goal being to characterize neutron-induced MCUs [1]–[10]. In such radiation tests, a single angular setup of the DUT (Device

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Digital Object Identifier 10.1109/TNS.2012.2224373

Under Test) is often adopted. For example, in the accelerated neutron radiation test, DUTs are irradiated by the neutron beam at only right angles to the DUT surface because of the limited radiation time. On the other hand, [11] reported that the probability of MCU and MCU multiplicity for a 1.2-V 6T SRAM in a 90-nm bulk CMOS process depend on the incident angle, in other words, the tilt angle of the neutron beam. [11] explained the angular dependency by using a simulation such that, in case of radiation at a large incident angle, forward emission of secondary ions leads to secondary ions hitting multiple sensitive nodes. Besides, the angular dependency of proton-induced SEU is reported in [12]–[14]. On the other hand, although it is known that in bulk CMOS technology MCUs are often provoked by bipolar effects [1]–[3], the bipolar effect was not considered in the simulation of [11]. Therefore, it is not clear how consistent the explanation is with the measurement result in [11].

Here, we focus on neutron-induced MCUs in ultra-lowvoltage operation and investigate the correlation between the measured angular dependency and the simulation of the generation and transport of secondary ions. As the supply voltage becomes lower, especially below 0.5 V, bipolar-induced MCUs are less likely to happen because the gain of bipolar transistor becomes smaller and the bipolar effects are less likely to be triggered, which is related to a fact that latch up does not occur below 0.5-V even when forward body biasing is given [15], [16]. Therefore, in lower-voltage operation, it is expected that MCU occurrences and their angular dependency are explained by the forward emission of secondary ions.

This paper presents the results of neutron-induced MCU measurements of a 10T subthreshold SRAM fabricated in a 65-nm bulk CMOS process, which has differential read ports and can operate even at 0.3-V [1], at two incident angles, i.e., 0° (right angle to the surface of DUT) and 60°. We confirm that the number of measured MCU at 60° is 1.13 times larger than that at 0° in 0.4-V operation, although the amount of radiated neutrons is half at 60°. On the other hand, we also observe that in 1.0-V operation the bipolar effect could make the angular dependency different. Applying RBB (Reverse Body Bias) that makes MCUs due to the bipolar effect less likely to happen [3], the ratio of MCU in RBB to ZBB (Zero Body Bias) is 0.58 in 1.0-V operation.

Furthermore, we execute a Monte-Carlo simulation using PHITS (Particle and Heavy Ion Transport code System), which can calculate the energy distribution deposited by neutron collisions [17]–[19]. The simulated SEU (Single Event Upset) probability shows that He and heavier ions are the dominant secondary ions which cause SEUs at the critical charge of 0.4-V operation. We then estimate the probability that secondary ions deposit sufficient charges on two or more sensitive volumes by

Manuscript received July 13, 2012; accepted October 04, 2012. Date of current version December 11, 2012.

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Fig. 1. Structure of 10T memory cell unit [1].



Fig. 2. Layout of memory cell array. The size of a memory unit is $4.4 \,\mu\text{m} \times 0.8 \,\mu\text{m}$.

simulating the generation and transport of secondary ions at 0° and 60° . The number of calculated MCUs at the angle of 60° is 1.20 times more than that at 0° , which is consistent with the measurement results. In addition, the simulated distribution of MCU multiplicity is correlated with the measured one.

The observed MCU patterns at the incident angle of 60° suggest that the forward emission of secondary ions induces the angular dependency. In our radiation-test setup, DUTs are irradiated by the neutron beam diagonally between the BL (Bit Line) and the WL (Word Line) on the x-y plane. The number of MCUs with checkerboard patterns along the beam path is larger than that with the checkerboard patterns orthogonal to the beam path in both the measurement and simulation.

The remainder of this paper is organized as follows. Section II explains the test setup of the 10T subthreshold SRAM and presents the measured angular dependency of neutron-induced MCUs. Section III verifies the angular dependency of neutron-induced MCUs with the Monte-Carlo simulation using PHITS. Section IV concludes with a brief summary.

II. MCU MEASUREMENT

A. Test Setup

A test chip including a 256 kb 10T SRAM was fabricated in a 65-nm CMOS process with triple well structure. Fig. 1 shows the cell structure of the 10T SRAM. This SRAM can operate even at 0.3 V, because the cross-coupled inverters are large enough to mitigate threshold voltage variability. Fig. 2 illustrates the physical layout of memory cell array. The size of a memory unit is 4.4 μ m × 0.8 μ m. Ellipses indicate sensitive areas to the radiation. The two cells along the BL are designed as symmetry. Well ties are placed every 8 BL memory cells.



Fig. 3. Test board configuration.

Fig. 3 shows the configuration of a test board used for the radiation test. Four test chips were placed on the test board at the roll angle of 45° to the board side. The incident angle of the neutron beam to the test structure, θ , was either 0° or 60° . Note that the diameter of the neutron beam is larger than the size of test board. The total amount of neutrons radiated to each test chip at the angle of 60° is half as much as that at 0° , because the cross-section of the test chip against the neutron beam decreases by $\cos 60^{\circ}$.

The neutron radiation tests were performed at RCNP (Research Center for Nuclear Physics, Osaka University) using an accelerated spallation neutron beam. The average flux density of the neutron beam was 2.36×10^9 cm⁻²h⁻¹. In this test, the eight test boards, one of which is shown in Fig. 3, were placed in series on the beam track, so that we tested 32 chips simultaneously. We first wrote zero to all bits, and then read all bits with a 3.54 s time interval. As we read with sufficiently short time interval, the occurrence probability of multiple neutron collisions during the time interval is sufficiently lower than that of MCU and it is negligible.

B. Experimental Result

Fig. 4 shows the measured angular dependency of the MCUs in 0.4-V operation. The horizontal axis is the MCU multiplicity. The vertical axis is the number of MCUs normalized by the total cells and the measurement time. Note that most of the MCUs occurred along the BL because the distance between two cells along the BL is one fifth of that with the WL. In this measurement, we observed 2 to 8 simultaneous upsets. The number of MCUs decreases as MCU multiplicity increases. The ratio of the total number of MCUs at the angle of 60° to those at 0° is 1.13 in 0.4-V operation. This result clearly indicates that the angular dependence of secondary ions raises the MCU probability at the angle of 60° comparable to, or rather larger than that of 0° even while the total amount of radiated neutrons decreases according to the incident angle.

Now let us compare the spatial MCU patterns at both incident angles. As shown in Fig. 3, neutrons at the incident angle of 60° were injected diagonally between the BL and the WL at the roll angle of 45° . Therefore, checkerboard MCUs, which are defined as the MCUs including upsets at a pair of two diagonal corners, can be classified into CHB_{along} (checkerboard pattern along the neutron beam) and CHB_{orth} (checkerboard pattern orthogonal to the neutron beam). Examples of CHB_{along}, CHB_{orth}, and other MCU patterns are illustrated in Fig. 5. We here classify the measured MCU patterns at the angles of 0° and 60° into them for comparison. Note that CHB_{along} and CHB_{orth} at the incident angle of 0° do not have any meaningful difference because neutrons are perpendicularly radiated to the test chip. Fig. 6 shows the angular dependency of CHB_{along} and CHB_{orth}



Fig. 4. Measured angular dependency of MCUs in 0.4-V operation. Each error bar indicates $\pm \sigma$, where σ is defined as the square root of the number of the observed upsets.



Fig. 5. Example of MCU patterns at the incident angle of 60° : (a) CHB_{along}, (b) CHB_{orth}, and (c) the others.



Fig. 6. Measured angular dependency of $\rm CHB_{along}\,$ and $\rm CHB_{orth}\,$ MCUs in 0.4-V operation. Each error bar indicates $\pm\sigma.$

MCUs. The number of CHB_{along} MCUs is similar to that of the CHB_{orth} MCUs at the incident angle of 0°, which is consistent with our expectation. On the other hand, at the angle of 60°, the number of CHB_{along} MCUs is roughly twice larger than that of CHB_{orth} MCUs. This result suggests that secondary ions contributing to MCU tend to emit forward and upset the memory cells along the neutron beam.

Next, Fig. 7 compares the body bias dependencies of SBU (Single Bit Upset) and MCUs in 0.5-V and 1.0-V operation. Here, RBB means 1.0-V body biased to N-well and -1.0-V body biased to P-well. In 1.0-V operation, RBB significantly reduces the MCU rate while maintains the SBU rate, which means a considerable portion of MCUs in 1.0-V ZBB operation are caused by the bipolar effect. This tendency is consistent with the results of [1], [3]. On the other hand, the difference between RBB and ZBB in 0.5-V operation is limited, or rather the MCU rate of RBB is higher, which indicates that MCUs due to the bipolar effect are not dominant in 0.5-V operation.



Fig. 7. Measured body bias dependency of SBU and MCUs in 0.5 and 1.0-V operations. Each error bar indicates $\pm \sigma$.

III. SIMULATION

A. Simulation Setup

To further investigate the MCU angular dependency, a Monte-Carlo simulation was performed using PHITS (Particle and Heavy Ion Transport code System) [17]. PHITS was employed to simulate neutron-induced soft errors together with a 3-D TCAD (Technology Computer Aided Design) simulator [18]. In the present work, on the other hand, the collected charge is calculated by a sensitive volume model [20] because the TCAD simulation is time consuming even for the SER analysis of SBU and is unrealistic for the MCU analysis.

The MCU simulation with the sensitive volume model in this work is outlined as follows:

- Simulation setup: The sensitive volume of an SRAM memory cell is defined by the off-state NMOS drain area and the funneling length. Incident neutrons are radiated on the area of a memory cell placed in the center of the memory cell array. Sufficient reaction volumes are also located on the top and bottom of the memory cell layer.
- 2) Particle transport simulation: Nuclear reactions and the subsequent transport of secondary ions are simulated by PHITS. The reaction models validated in the previous work [18] are used, namely, the e-mode option with a JENDL-3.3 (Japanese Evaluated Nuclear Data Library Version 3 Revision-3) for neutron energies less than 20 MeV, and the MQMD (Modified Quantum Molecular Dynamics) model option for those above 20 MeV. For calculations of the LET (Linear Energy Transfer) of secondary ions, the ATIMA (Atomic Interaction with Matter) option [21] implemented in PHITS is applied.
- 3) Judgment of MCUs: In the sensitive volume model, it is assumed that an SEU occurs when the total charge deposited in the sensitive volume exceeds the critical charge which is estimated by circuit simulation. For each neutron incidence, we examine the memory cells in which the charge deposited by secondary ions exceeds critical charge, and accumulate the MCU events.

Fig. 8 illustrates the configuration of the test device used in PHITS simulation. An SRAM memory cell with the size of 4.4 μ m × 0.8 μ m is placed in the bottom of a 4.4 mm × 1.6 mm × 0.5 mm silicon substrate as two-dimensional grid. A silicon dioxide insulation layer with 0.35 μ m thickness is placed under the silicon substrate. A 3.0 μ m metal layer consisting of copper and silicon dioxide is located under the insulation layer and a 0.5 mm silicon dioxide package layer is placed under



Fig. 8. Test device configuration in PHITS simulation.



Fig. 9. RCNP neutron energy spectrum used in PHITS simulation.

a metal layer. The size of the defined sensitive volume is 0.5 μ m × 0.25 μ m × 0.6 μ m, where the depth of 0.6 μ m was determined referring to [22]. The sensitive volume is located in each memory cell. Neutrons with the same energy spectrum as RCNP neutron beam [23] shown in Fig. 9 are radiated at the incident angles of 0° and 60°.

Fig. 10 shows the simulated SEU probability including both SBU and MCU per neutron flux as a function of critical charge at the incident angles of 60° and 0°. Individual contributions from secondary H, He, and heavier ions to the SEU are separated for the result of 0° in Fig. 10. There is little difference between the SEU probabilities at the angles of 60° and 0°. On the other hand, the critical charge of our 10T SRAM in 0.4-V operation with ZBB is estimated by circuit simulation to be 1.4 fC (Fig. 11). The circuit simulation setup for critical charge evaluation is found in [1]. We used a simple current pulse model similarly to [24]. Therefore, He and heavier ions are the dominant secondary ions causing SEUs in 0.4-V operation because these ions occupy 89% of the SEU probability at 1.4 fC of critical charge.

B. Simulation Results and Discussion

Fig. 12 shows the simulated angular dependency of MCUs. The horizontal axis denotes the MCU multiplicity. The vertical axis represents the number of events normalized by the incident neutron flux. The ratio of the total number of MCUs at the angles of 60° to those at 0° is 1.20. This is compatible with the measurement results. Compared with Fig. 4, this simulation result explains that the decrease in the number of neutrons radiated to the test chip is overwhelmed by the angular dependency of the secondary ions.



Fig. 10. Simulated SEU probability of each ion as a function of critical charge.



Fig. 11. Simulated critical charge of 10T memory cell when node A is "1" and node B is "0" [1].



Fig. 12. Simulated angular dependency of MCUs. Each error bar indicates $\pm \sigma$.

Next, Fig. 13 shows the simulated angular dependency of $\rm CHB_{along}$ and $\rm CHB_{orth}$ MCUs. We can see that, similarly to Fig. 6, the number of $\rm CHB_{along}$ MCUs is larger than that of $\rm CHB_{orth}$ MCUs at the incident angle of 60°. Forward emission of secondary ions, which is considered in this simulation, reproduces the measured tendency.

MCU is also caused by charge-sharing [12], though it was not considered in the simulation. Reference [1], in which the test chips were irradiated only at the incident angle of 0° , describes that not bipolar but another effect, such as the charge-sharing, becomes a dominant mechanism of MCUs in the subthreshold region. As the incident angle of the neutron beam increases, the influence of charge-sharing may increase, but it could not be evaluated in the simulation. On the other hand, the simulation in this work, which considers the generation and transport of



Fig. 13. Simulated angular dependency of CHB_{along} and CHB_{orth} MCUs in 0.4-V operation. Each error bar indicates $\pm \sigma$.

secondary ions, mostly reproduced the measured tendency. This indicates that the forward emission of the secondary ions plays an important role to cause the MCU angular dependency.

IV. CONCLUSION

We measured the neutron-induced MCUs in a 10T subthreshold SRAM that was fabricated in a 65-nm bulk CMOS process in 0.4-V operation at neutron incident angles of 0° and 60° . Our measurement results showed that the number of measured MCU at the angles of 60° to that at 0° was 1.13 even though the total amount of neutrons decreased by half. Moreover, the simulation results using PHITS presented that the number of MCU at the angles of 60° to 0° was 1.20, which is consistent with the measurement. Furthermore, the measurements and simulation showed that the number of CHB_{along} MCUs was larger than that of CHB_{orth} MCUs at the angle of 60°. Thus, the measured angular dependency is explained by the generation and transport of secondary ions in the device simulated with PHITS. These results indicate that, in ultra-low-voltage operation, the forward emission of secondary ions plays an important role to cause the angular dependency of MCU.

ACKNOWLEDGMENT

The VLSI chip in this study was fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with STARC, e-Shuttle, Inc., and Fujitsu Ltd. The authors appreciate the support of Prof. K. Hatanaka and Assistant Prof. K. Takahisa of Osaka University with the neutron radiation test at RCNP.

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