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Power Gating Implementation for Supply Noise Mitigation with Body-Tied Triple-Well Structure

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SUMMARY This paper investigates power gating implementations that mitigate power supply noise. We focus on the body connection of power-gated circuits, and examine the amount of power supply noise induced by power-on rush current and the contribution of a power-gated circuit as a decoupling capacitance during the sleep mode. To figure out the best implementation, we designed and fabricated a test chip in 65 nm process. Experimental results with measurement and simulation reveal that the power-gated circuit with body-tied structure in triple-well is the best implementation from the following three points; power supply noise due to rush current, the contribution of decoupling capacitance during the sleep mode and the leakage reduction thanks to power gating.

key words: *power gating, on-chip power supply noise, rush current, well structure*

1. Introduction

With strong demands for low power VLSIs ranging from portable devices to high-end processors, power gating technique has become of a common practice for reducing leakage current of inactive circuits, and is intensively investigated for reducing wake-up time and maximizing leakage reduction. On the other hand, shorter wake-up time from sleep (power-gated) mode necessarily induces larger rush current to recharge gate and PN-junction capacitances in the power-gated circuit, which results in a large voltage drop in the power supply network. To mitigate the drop induced by the rush current, a smart wake-up procedure [1], [2] and a sophisticated power gating structure [3], [4] are presented.

Power gating involves another undesirable feature that intrinsic decoupling capacitances in the power-gated circuit becomes isolated from the power distribution network and their contribution as a decoupling capacitance cannot be expected. Consequently, the power supply noise in neighboring active circuits increases. Besides, the intrinsic decoupling capacitance consists of gate and PN-junction capacitances, and the PN-junction capacitance depends on the well structure. In [5], power supply noises in twin-well and triple-well structures are measured and compared. Compared to the twin-well structure, the ground bounce in the triple-well structure is larger due to the absence of the P-substrate resistive network, and the power voltage drop is smaller thanks to the increase in the PN-junction capacitance.

This paper clarifies how power gating should be implemented for mitigating power supply noise without degradation in leakage reduction effect. For this purpose, we focus on the well structure and the body connection and designed and fabricated a 65 nm test chip. Using the fabricated chip, two measurement results of the power supply noise and one measurement result of the leakage current are presented, where the first noise measurement shows the difference of power supply noise due to the rush current during the wake-up and the second result exemplifies how the power-gated circuit behaves as an intrinsic decoupling capacitance. On the basis of these measurement results, we demonstrate the best gating implementation.

The remaining of this paper is organized as follows. Section 2 explains power gating structures and qualitatively discusses their influence on power supply noise. Section 3 shows the test chip structure. Section 4 presents measurement and simulation results, and reveals the best implementation for power gating. Finally, Sect. 5 concludes this discussion.

2. Power Gating Structure

When we implement power gating, there are two options; bodies of PMOSs and NMOSs are also gated or not. We hereafter call the option that only VDD and VSS are gated "body-tied", and the option that the bodies as well as VDD and VSS are gated "body-gated". The aim of this paper is to quantitatively demonstrate how these options in twin- and triple-well structures affect power supply noise. In the following, both VDD and VSS are gated, whereas either of the two is often gated in practical implementations.

2.1 Power Gating with Body-Gated Option

Figures 1 and 2 illustrate power gating with body-gated option. Figure 2 shows a cross-section of twin-well structure and its equivalent circuit when body-gated option is adopted. VDD and VSS are power and ground lines, and VNW and VPW represent backgate voltage lines connected to N-well and P-substrate respectively. PN-junction between N-well and P-substrate is modeled as a diode (D_{nw}). This diode is reversely biased, and hence it behaves as PN-junction capacitance. An important point here is that this capacitance is connected between virtual VDD and virtual VSS and the charge is gradually discharged during the sleep

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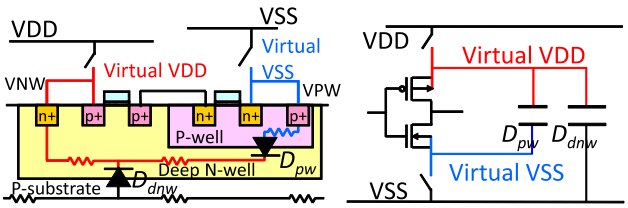


Fig. 1 Cross-section and circuit representation of triple-well structure with body-gated option.

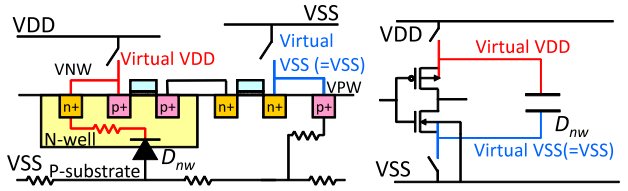


Fig. 2 Cross-section and circuit representation of twin-well structure with body-gated option.

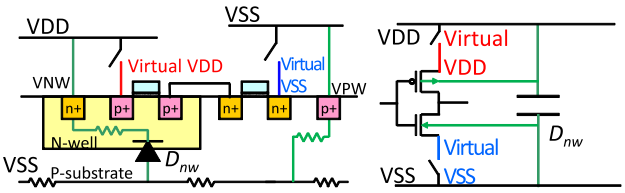


Fig. 3 Cross-section and circuit representation of twin-well structure with body-tied option.

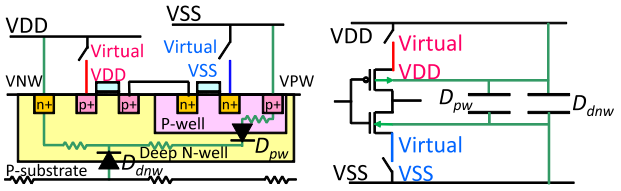


Fig. 4 Cross-section and circuit representation of triple-well structure with body-tied option.

mode, where virtual VSS is connected to VSS through P-substrate in twin-well structure.

A cross-section of triple-well structure and its equivalent circuit for body-gated option is illustrated in Fig. 1. VNW and VPW are connected to deep N-well and P-well, respectively. In the case of the triple-well structure, there are two types of well junction capacitance, which originate from the diode between P-well and deep N-well (D_{pw}) and the diode between deep N-well and P-substrate (D_{dnw}). D_{pw} is connected between virtual VDD and virtual VSS, and D_{dnw} is between virtual VDD and VSS. This means that the charges stored in D_{pw} and D_{dnw} are discharged during the sleep mode.

Thus, with body-gated option, well capacitance must be recharged when the power is turned on. In bulk CMOS technology, the well capacitance occupies a significant portion of intrinsic circuit capacitance [6], and hence large rush current flows. This large rush current causes large IR drop and Ldi/dt noise. On the other hand, it is well known that well capacitance behaves as a decoupling capacitance [6]. During the sleep mode, the noise reduction effect thanks to the well junction capacitance in power-gated circuits cannot be expected.

2.2 Power Gating with Body-Tied Option

On the other hand, when body-tied option is adopted, these well capacitances are always connected between VDD and VSS. This is illustrated in Figs. 3 and 4. Both in twin- and triple-well structures, well capacitances are not discharged during the sleep mode, which means it is not necessary to recharge the well capacitances. When power is turned on, only the gate and source/drain-body diffusion capacitances are recharged. Therefore, smaller rush current is expected. In addition, the well capacitances are always connected to the power distribution network, and hence the contribution as decoupling capacitance is expected even in the sleep mode. Here, it should be noted that "body-tied" option requires a tap-less standard cell library, in which well taps are not included inside each standard cell and special cells for body connection are provided, is necessary.

3. Test Chip Structure and Simulation Setup

3.1 Test Chip Structure

A test chip for evaluating noises and leakage current was fabricated in a 65 nm CMOS process. Figure 5 shows a micrograph of the test chip. The test chip consists of four test elementary groups (TEGs) and shift registers. The shift registers store configurations of the TEGs. The counter used in the waveform sampling macros [7] is also included in the shift resistors. These macros called "gated oscillator" and "latch oscillator" are ring-oscillator-based circuits but they capture dynamic noise waveforms thanks to intermittent operation at the timing of interest.

Each TEG consists of noise sources, the measurement macros, control logic and source followers. Figure 6 depicts the basic TEG structure including the measurement macros, switches for power gating and source followers. The source followers are used to observe the voltage variations of virtual VDD and VSS during the sleep mode. A noise source is composed of 512 (= 8×64) 12-stage NAND chains. Two noise sources are placed in a TEG, and these are connected through transmission gates (switches). A noise source occupies $115\,\mu\text{m} \times 150\,\mu\text{m}$ and the area of a TEG is $490\,\mu\text{m} \times 300\,\mu\text{m}$. The right noise source, which can be gated, is named "gated_NS", and the other, which is always connected to power and ground lines, is called "powered_NS". In the following measurements, VDD and VSS are set to be 1.2 V and 0.0 V.

Figures 7–10 illustrate four TEGs (TEG1–TEG4) on the test chip. These TEGs are different in terms of well structure (twin- and triple-well for powered_NS and gated_NS) and power gating structure (body-tied and body-

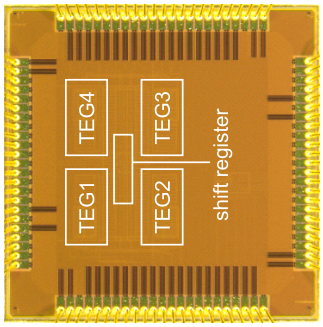


Fig. 5 Chip micrograph (2.1 mm × 2.1 mm).

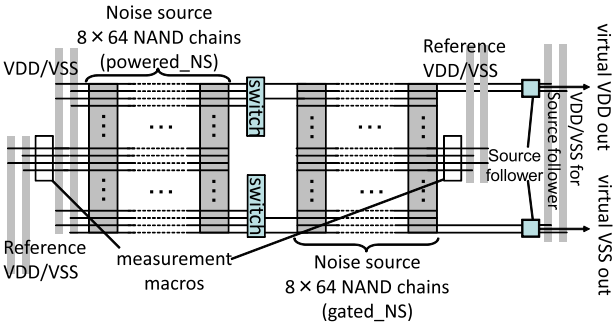


Fig. 6 Basic TEG structure with noise sources and measurement macros.

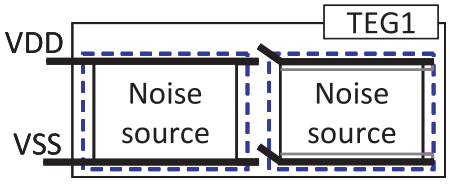


Fig. 7 TEG1: triple-well to triple-well, body-gated. Dotted line represents deep N-well, bold lines are VDD and VSS lines, and gray lines show body connection.

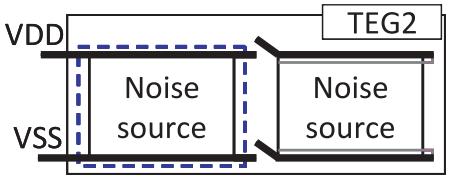


Fig. 8 TEG2: triple-well to twin-well, body-gated. Dotted line represents deep N-well, bold lines are VDD and VSS lines, and gray lines show body connection.

gated). With these four TEGs, we first evaluate the power supply noise due to rush current that flows when the switch gets turned on. In the body-tied structures (TEG 3 and 4), the wells under gated_NS are always connected to VDD or VSS. Then, the well capacitance is not discharged even while gated_NS is gated, which is expected to result in smaller rush current. Therefore, smaller power supply noises are expected in the body-tied structures (TEG 3 and 4) compared to the body-gated structures (TEG 1 and 2). In addition, the well capacitance under the gated_NS is supposed to behave as a decoupling capacitance and help reduce power supply noise. The second evaluation aims to examine whether the well capacitance inside the power-gated circuits can contribute to noise suppression as a decoupling capacitance.

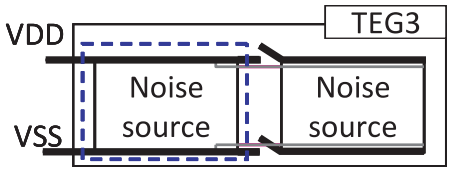


Fig. 9 TEG3: triple-well to twin-well, body-tied. Dotted line represents deep N-well, bold lines are VDD and VSS lines, and gray lines show body connection.

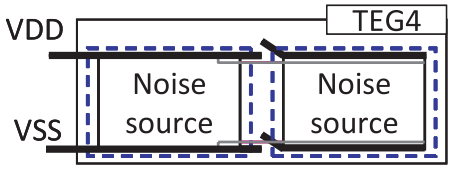


Fig. 10 TEG4: triple-well to triple-well, body-tied. Dotted line represents deep N-well, bold lines are VDD and VSS lines, and gray lines show body connection.

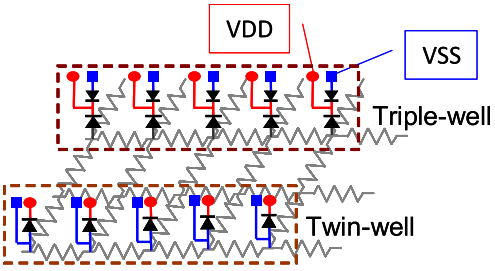


Fig. 11 Well modeling for simulation.

3.2 Simulation Model

A circuit model used for simulation includes package and bonding wires, on-chip power and ground networks, noise sources, P-substrate resistive mesh and well junction diodes (Fig. 11) associated with four TEGs and peripheral IO cells. Figure 12 shows the layout outline of the modeled N-well and deep N-well on the chip. Then, the network of on-chip wire resistance, which is connected to an ideal voltage source through package inductances, is attached to the chip-level substrate and well models. N-well, deep N-well and P-well diode models and substrate resistivity are given from a foundry. We simulate power supply and ground noises with SPICE.

4. Measurement Results

4.1 Power Supply Noise Due to Rush Current

We first measured the waveforms in voltage between vir-

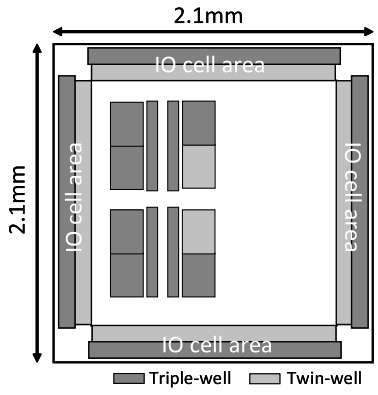
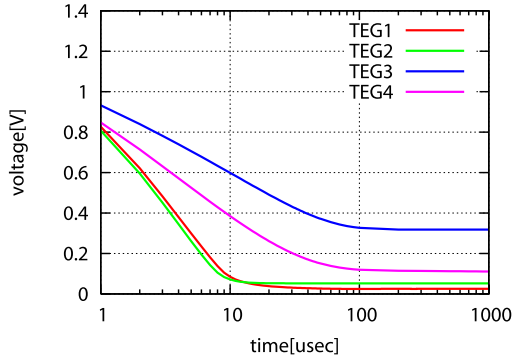
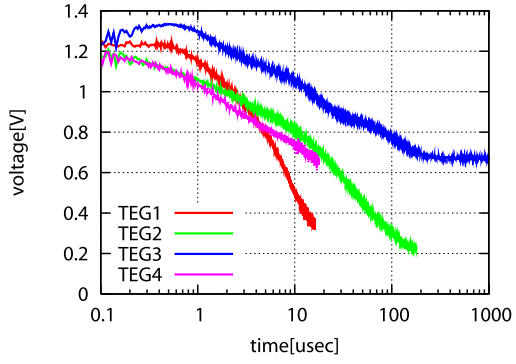


Fig. 12 Well layout of test chip.



(a) Simulation results



(b) Measurement results

Fig. 13 Virtual VDD — virtual VSS waveforms after power gating.

tual VDD and virtual VSS after power gating using calibrated source followers. Figure 13 shows simulation and measurement results. In the measurement, the regions in which the gains of the source followers for sensing virtual VDD and VSS have are larger than 0.25 are plotted. As the time elapses, the voltage difference between virtual VDD and virtual VSS becomes smaller, but the decreasing speed is different among TEGs. In the simulations, the speed is fast in the body-gated structures of TEG1 and TEG2. On the other hand, the speed is slow in the body-tied structures of TEG3 and TEG4. This slow speed is desirable for short-term power gating, because the amount of leaked charge is small and the energy to recharge the capacitance is small. This behavior can be explained as follows. In the body-tied structures, virtual VDD is lower than VNW and virtual VSS is higher than VPW, which means transistors in the power-gated circuit are in reverse body bias. In this case, the threshold voltage is higher compared to zero body bias, and then the discharging speed becomes slower. Thus, the body-tied structure has a desirable property on the discharging speed. The measurement results are correlated with the simulations, while the speed of TEG2 was slower than expected. When the right noise source circuit in TEG2 is power-gated, the p-substrate rather than the NMOS power switch is included in the leakage path. A possible reason is that the resistance of p-substrate was different from the value used in the simulation and the virtual VDD in the steady state could be different between simulation and measurement.

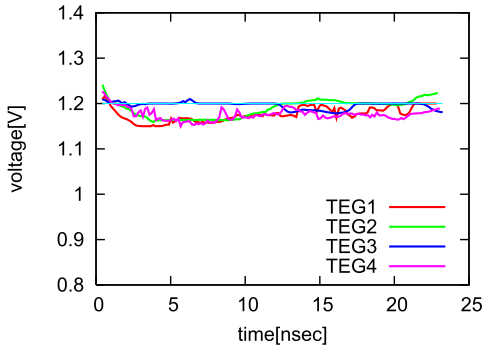
We next evaluate noise waveforms due to rush current. We varied the time of the sleep mode and measured the noise waveforms using a latch-oscillator which is suitable for long-term measurement. The voltage resolution was below 20 mV at most voltages and the worst resolution was 50 mV with 400 ps time resolution. Figures 14(a) to 14(d) show the measured noise waveforms. We can see that the noise magnitude becomes larger as the sleep time becomes longer. When the sleep times are 500 ns, 5 μs and 50 μs, it can be clearly seen that the noises in the body-tied structures (TEG2 and TEG3) are smaller than those of TEG1 and TEG4, which is consistent with our expectation. In the case of 50 μs, the noise reduction effect is over 0.1 V. Especially, focusing on the power-gated circuits in triple-well structure (TEG1 and TEG4), the difference is significant. The triple-well structure has larger well capacitance and hence it tends to induce larger rush current. However, this disadvantage can be completely solved in the body-tied structure (TEG4).

4.2 Effect of Leakage Current Reduction

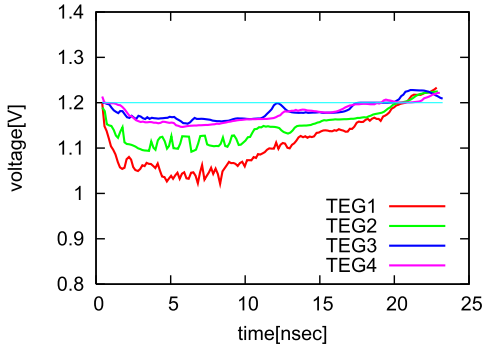
We next evaluate the leakage reduction effects in different well and body connection implementations. The leakage current of each TEG was measured with the power gating switch ON and OFF keeping the noise sources inactive. Note that the leakages of both powered_NS and gated_NS are included, whereas that of gated_NS is reducible by power gating.

The measurement result in Fig. 15 shows that TEG1 and TEG4 achieved the lowest leakage current. In the case that the power gated circuit is in twin-well (TEG2 and TEG3), larger leakage current flows. Also, it pointed out that the body-tied structure in twin-well is not a good idea from a viewpoint of leakage current.

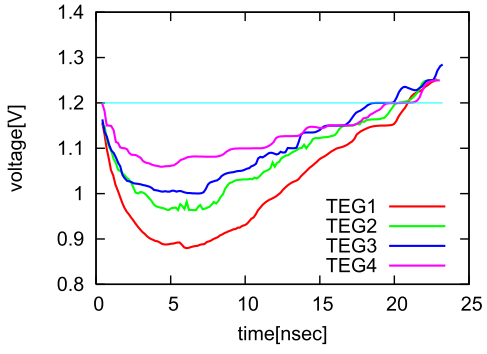
We next compare TEG1 and TEG4 having the power-gated circuit in triple-well, where the difference is the body connection. We can see that the leakage currents of TEG1 and TEG4 are almost the same in both cases that the gating switch is ON and OFF, which means that the well junction leakage in the triple-well structure is negligible. We thus conclude that the body-tied structure in triple-well is reasonable and usable.



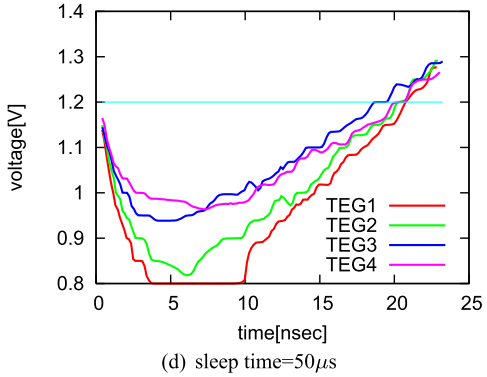
(a) sleep time=50 ns



(b) sleep time=500 ns



(c) sleep time=5μs



(d) sleep time=50μs

Fig. 14 Noise waveforms due to rush current w/different sleep times.

4.3 Decoupling Effect of Power-Gated Circuits

We lastly evaluate the performance of the power-gated circuit (gated_NS) as a decoupling capacitance. In this measurement, all the chains in powered_NS were active (switching), while all the chains in gated_NS were inactive. A 50 MHz clock signal was given to powered_NS, and the power supply noise was measured with a gated oscillator which can attain higher time and voltage resolutions. The voltage resolution was below 10 mV at most voltages and the worst resolution was 30 mV with 400 ps time resolution. The transmission gates for power gating were off, and the difference of the power supply noise was evaluated.

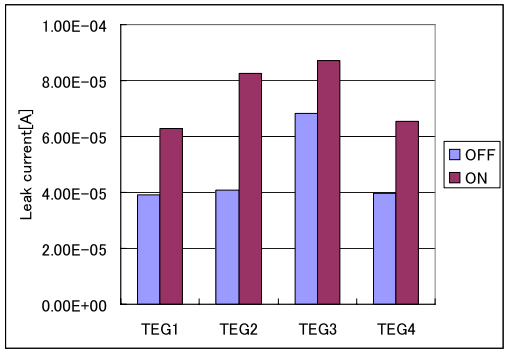
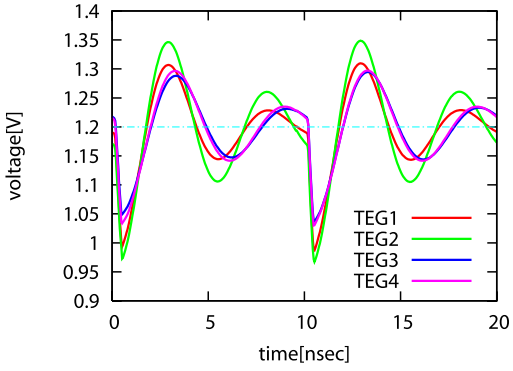
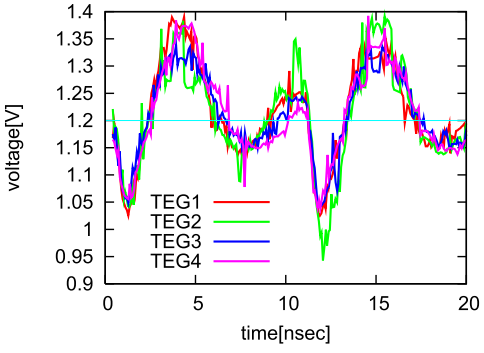


Fig. 15 Measured leakage currents when gating switch is ON or OFF.



(a) Simulation results



(b) Measurement results

Fig. 16 Noise waveforms when the switch for power gating is OFF.

Figure 16 shows VDD-VSS noise waveforms of simulation and measurement. Let us compare the maximum drops comparing the body-tied groups of TEG3 and TEG4 with the body-gated groups of TEG1 and TEG2. The volt-

age drops of the body-gated groups are clearly larger those of the body-tied groups in simulation, and this tendency is consistently with the measurement, expecially of TEG2. This result validates our expectation that the well capacitance in body-tied circuits contributes as decoupling capacitance even in the sleep mode.

5. Conclusion

We investigated the power gating implementations focusing on the well structure and body connection. The measurement results of the 65 nm test chip clearly revealed that the circuit for power gating should be placed in triple-well whose bodies are always connected to VDD/VSS. With this configuration, we can expect (1) smaller noise due to rush current, (2) good leakage reduction effect, and (3) decoupling effect for other circuits even during the sleep mode.

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