Supply Noise Suppression by Triple-Well Structure

Yasuhiro Ogasahara, Masanori Hashimoto, Toshiki Kanamoto, and Takao Onoye

***Abstract*— This brief discusses the impact of twin- and triple-well structures on power supply noise, and a substrate model for simulating the power supply noise. We observed V_{ss} noise reduction by the resistive network of the p-substrate and V_{dd} noise reduction by the junction capacitance of a triple-well structure on a 90-nm test chip. Measurement results also showed that the total noise reduction of a triple-well structure is superior to that of a twin-well structure. The measurement results correlate well with the results obtained from the power supply noise simulation using a hierarchical resistive mesh model. Our simulation-based verification indicates that in common CMOS design, a triple-well structure can reduce the power supply drop by 10%–40% or the decoupling capacitance area by 5%–10%. We also verified that supply drop sensitivity to variation of the well junction capacitance is sufficiently small and that supply noise reduction using a triple-well structure is robust to process variation.**

***Index Terms*— Circuit noise, noise measurement, substrate.**

I. Introduction

Power supply noise is becoming a serious issue in recent processes. A stable power supply network design is essential, and hence accurate estimation and mitigation of power supply noise are crucial for successful physical design. Power distribution networks are often analyzed with current consumption of the circuit, resistance and inductance of wire and package, and capacitance [1], [2]. Optimization of the power distribution network, pad allocation, and decoupling capacitance (decap) placement is discussed for power integrity.

In a conventional design with a twin-well structure, V_{ss} is connected to a p-substrate to supply backgate voltage. The p-substrate makes V_{ss} voltage stable because the V_{ss} current is widely diffused and drained to the system ground through the resistive network of the p-substrate in addition to supply wires. In previous published works, [3], [4] referred to the relation between the p-substrate and supply noise, [5] measured smaller V_{ss} noise than V_{dd} noise in a twin-well structure, and our preliminary work [6] measured noise reduction by a p-substrate.

In recent processes, a triple-well structure, which involves additional fabrication cost, is often used for body biasing in high-performance and low-power designs [7] and for substrate noise reduction in mixed systems-on-chip designs [8]. In addition, the PN junction capacitance associated with triple-well structures works as a decoupling capacitance (decap) and contributes to mitigation of the power supply noise.

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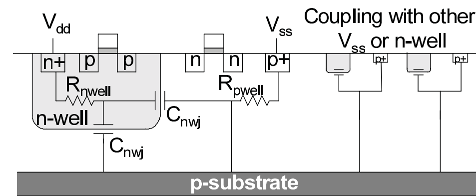

Fig. 1. Cross section and parasitic elements in twin-well structure.

Although substrate noise reduction in the triple-well structure has been actively discussed [8], solid measurements of supply noise reduction by the triple-well structure have not been reported as far as the authors know. In addition, isolation from the p-substrate by a triple-well structure immunizes the p-substrate effect on the power supply. There is a tradeoff between reductions by the p-substrate in a twin-well structure and the large PN junction capacitance of a triple-well structure.

In this brief, we measured V_{dd} and V_{ss} noise waveforms on a test chip fabricated with a 90-nm CMOS process. The contributions of this brief are as follows:

1) clarifying the impact of twin- and triple-well structures on power supply noise;
2) validating a simulation model for power supply noise considering substrate structure;
3) evaluating the effectiveness of a triple-well structure for achieving power integrity.

Measurement results of twin- and triple-well structures suggest that consideration of the well structure is highly required for power integrity analysis. A substrate model with a hierarchical mesh [9] well reproduces the impact of the substrate structure. Our simulation-based discussion clearly shows that a triple-well structure can effectively reduce the supply fluctuation. Effective use of a triple-well structure can cut down on the area required for decap.

II. Substrate/Well Structures and Supply Noise

A. Well Structures

Fig. 1 depicts a cross section of a twin-well structure with intrinsic parasitic elements. Usually V_{dd} and V_{ss} are, respectively, connected to the n-well and the p-substrate in cell-based designs to provide backgate voltage to the transistors. The p-substrate is modeled as a resistive network, which is described in Section II-B. The PN junction between the n-well and the p-substrate is modeled as capacitance (C_{nwj}), and works as decap. Due to the resistive substrate network, the impedance of the V_{ss} network becomes smaller, which helps to reduce V_{ss} noise. Simulated and measured results for this V_{ss} noise suppression were reported in [5].

A triple-well structure is modeled as shown in Fig. 2. V_{dd} and V_{ss} are, respectively, connected to the deep n-well and p-well. There is a substrate resistance network under the wells. For a triple-well structure, there are junction capacitance between the p-well and the deep n-well (C_{pwj}) and that

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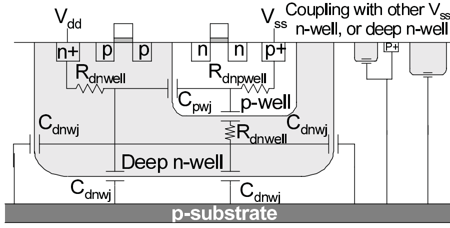

Fig. 2. Parasitic capacitance of deep n-well structure.

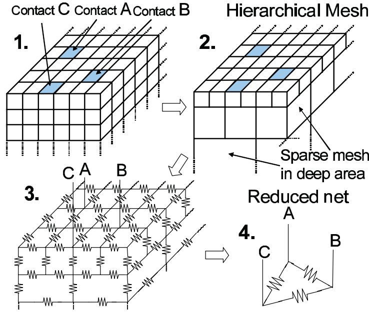

Fig. 3. Resistive mesh model of substrate. (a) Uniform mesh. (b) Hierarchical mesh. (c) Converting resistance. (d) Reduced net.

between the deep n-well and the p-substrate (C_{dnwj}). Both C_{pwj} and C_{dnwj} help to stabilize V_{dd}. V_{ss} benefits only from C_{pwj}, and is isolated from the resistive network of the p-substrate.

In the triple-well structure, there are two aspects in terms of power supply and ground noises.

1) P-substrate: V_{ss} noise becomes worse due to isolation from the p-substrate in comparison with a twin-well structure.
2) Junction capacitance: Larger PN junction capacitance (C_{pwj}, C_{dnwj}) reduces V_{dd} noise.

It is not clear whether a decrease in the V_{dd} noise or an increase in the V_{ss} noise is dominant, or whether the power supply noise increases, decreases, or is unchanged. Clarifying this point is the primary objective of this brief, and the measurement and simulation data in Section V explain our results.

B. Substrate Modeling

A substrate can be modeled as a 3-D resistive mesh as shown in Fig. 3 [10]. This model represents a numerical approximation of Maxwell's equation. A uniform mesh model requires substantial computational cost for reducing the number of networks because increasing the grid density is required for accurate analysis. Hierarchical mesh model [9] can simplify the uniform model. The resistive mesh of the hierarchical model (the third network) can be reduced as the fourth network in this example. The resistance network among three points of interest is composed of dc resistances between two points.

III. Measurement Circuit Structure

A. Overview of Test Chip

A test chip for evaluating substrate and deep n-well effects on power supply noise was fabricated with a 90-nm CMOS process. 1.0 V V_{dd} is supplied for the chip. Fig. 4(a) shows a micrograph of the test chip. The measurement circuit on test chip consists of three test element group (TEGs), shift registers, and a phase lock loop (PLL). The power supply noise is intentionally induced, and V_{dd} and V_{ss} waveforms are observed on the TEGs. The PLL supplies a clock signal to TEGs. The shift registers store configurations of TEGs and the PLL, and include a counter for waveform measurement.

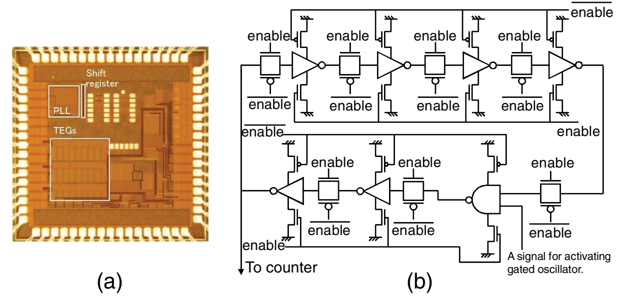

Fig. 4. (a) Test chip micrograph. Chip size is 2.5 × 2.5 mm^2. (b) Measurement macro for waveform sampling.

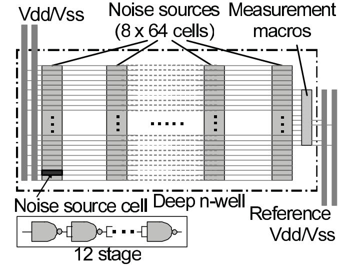

Fig. 5. Layout of a DUT with noise sources and measurement macros.

B. TEG Structure

Each TEG consists of a device under test (DUT) with noise sources, measurement macros, and a control logic circuit. The measurement macro shown in Fig. 4(b) [11] is adopted. The test chip fabrication technology is the same as that reported in [11], and the time and voltage resolutions of this macro are, respectively, about 180 ps and 10 mV. Fig. 5 shows the layout of the DUT. Each cell of the noise source consists of serially connected 12-stage NAND gates, and 512 cells are located in the whole noise source. The 620 × 160 μm DUT area includes eight columns of 64 cells with 76.72 μm pitch, and the noise sources occupy 22% of the DUT area. Dedicated power and ground pins are allocated for each DUT. Each supply line to a DUT includes a wide on-chip M6 wire (0.1 Ω) and package and bonding wires (3.5 nH). Power and ground lines in a DUT use M1 lines. To observe the V_{dd} waveform, the V_{ss} waveform, and the voltage difference between the two (V_{dd}-V_{ss}), three measurement macros are embedded. Reference V_{dd} and V_{ss} lines are prepared to measure V_{dd} and V_{ss} waveforms separately.

We implemented three TEGs named TEG_2WELL, TEG_2WELL_5X, and TEG_3WELL. The DUT is isolated by the deep n-well in TEG_3WELL as shown in Fig. 5. In TEG_2WELL and TEG_2WELL_5X, the DUTs are implemented on the p-substrate. The n-well

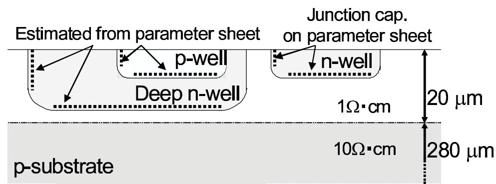

Fig. 6. Simulation setup for the substrate.

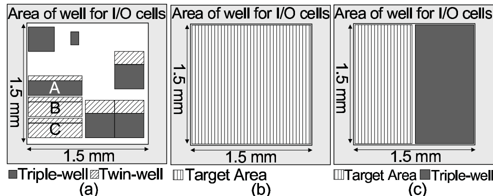

Fig. 7. Layout of n-well, deep n-well, and well of I/O cells. (a) Layout of test chip = TEST-CHIP configuration. (b) ASIC configuration. (c) MIXED configuration.

area in TEG_2WELL_5X is five times larger than that in TEG_2WELL. The V_{dd} and V_{ss} of each TEG are directly connected to package Pins, and are not shared with other TEGs.

IV. Simulation Setup

We simulate supply and ground noise with a circuit simulator [12]. The simulated circuit includes a full-chip power distribution network, noise sources, package and bonding wires, a full-chip substrate, and wells on the chip.

The power supply network is modeled with package inductance and on-chip resistance. The noise source circuit in a TEG of interest is modeled with the variable switch model proposed in [13] to make simulation time practical.

The substrate is modeled with the hierarchical model in Fig. 3, (explained in Section II-B). We assume the substrate structure in Fig. 6. The depth and doping profile of the p-substrate are confidential. The resistivity was first extracted from the actual profile, and its simplified resistivity was used for experiments. The junction capacitance value of the n-well follows the process parameter sheet. On the other hand, the doping information on the deep n-well was not disclosed, and hence we adopted a simple estimation that the junction capacitance of the deep n-well and the p-well in the deep n-well is twice as large as the n-well junction capacitance.

The PN junction capacitances of the n-well and the deep n-well in the core area are connected to the V_{dd}/V_{ss} supply network as well as to the substrate node. We here omitted the R_{well} for simplicity because the RC time constant of the PN junction capacitance is estimated to be smaller than one-tenth of the FO1 inverter delay.

We evaluate the impact of the substrate effect with the three chip layout configurations shown in Fig. 7. The first configuration [Fig. 7(a)] is the test chip layout (TEST-CHIP configuration). In the second configuration [Fig. 7(b)] it is assumed that there is only a digital circuit on the chip (ASIC configuration). In the third configuration in Fig. 7(c) (MIXED configuration), the digital circuit area occupies half of the chip and remaining half is occupied by an analog and/or memory in triple-well structure.

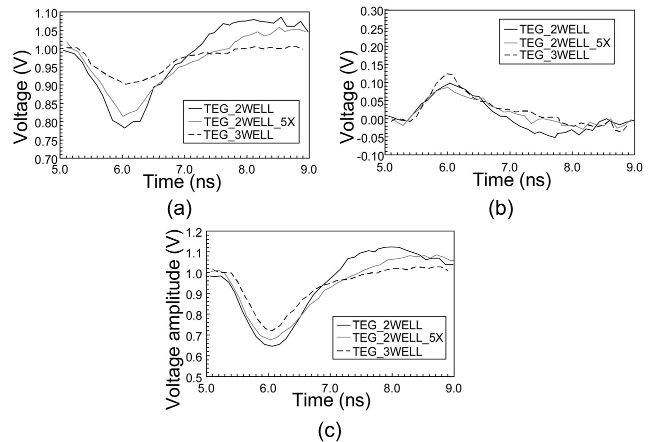

Fig. 8. (a) Measured V_{dd} waveforms. V_{dd} noise in TEG_3WELL is smaller than that of TEG_2WELL. (b) Measured V_{ss} waveforms. Increase of V_{ss} noise in TEG_3WELL is relatively small in comparison with reduction of V_{dd} noise. (c) Measured waveforms of voltage amplitude (V_{dd}-V_{ss}). Power supply noise is reduced in TEG_3WELL.

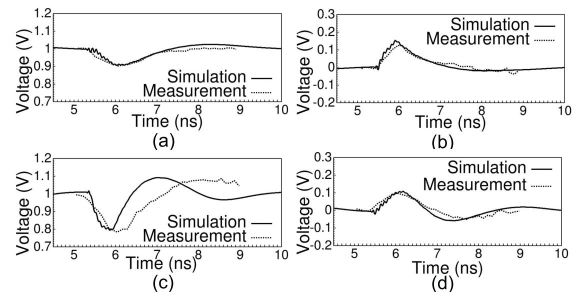

Fig. 9. Measured and simulated waveforms. (a) TEG_3WELL, V_{dd}. (b) TEG_3WELL, V_{ss}. (c) TEG_2WELL, V_{dd}. (d) TEG_2WELL, V_{ss}.

The analog (memory) areas in MIXED configurations, the TEGs except the TEG of interest in the TEST-CHIP configuration, and the I/O areas are modeled with only the PN junction capacitance and power supply's package inductance. The test chip's noise source cell (a serially-connected 12-stage NAND cell) was adopted as the digital area circuits for simulation of the ASIC and MIXED configurations, and the active cell occupies 22% of the whole circuit. The digital area layout structures are the same as those of the DUT of the test chip through the areas are different.

V. Experimental Results Using Test Chip

Fig. 8 shows measured V_{dd}, V_{ss}, and V_{dd}-V_{ss} waveforms of TEG_2WELL, TEG_2WELL_5X and TEG_3WELL, with all noise sources operating with a 100 MHz clock signal (effectively 200 MHz because negative edge also activate the noise sources). The time resolution of the sampling macros is 200 ps and the sampling period for capturing waveforms is 100 ps. The voltage resolution is 10 mV in this configuration. Fig. 9 compares the simulation and measurement results of TEG_2WELL and TEG_3WELL.

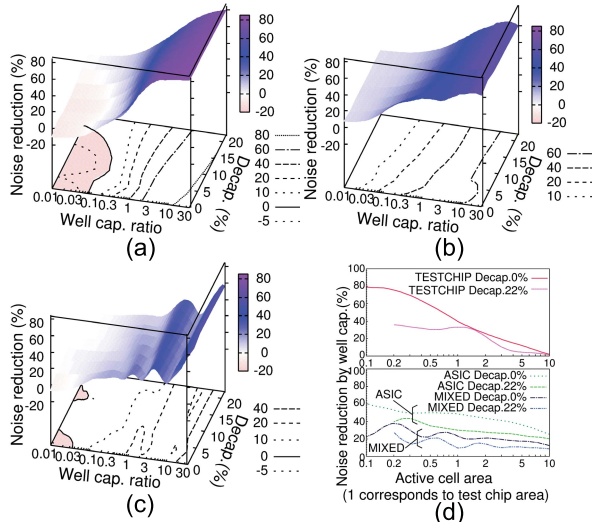

Fig. 10. 3-D plots and contour maps of supply fluctuation improvements by triple-well. (a) TEST-CHIP configuration. (b) ASIC configuration. (c) MIXED configuration. (d) Supply fluctuation improvement by triple-well structure versus transistor density.

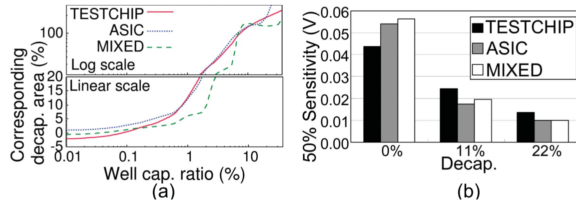

Fig. 11. (a) Triple-well effect represented in corresponding decap. (b) Maximum sensitivity (V/50%-variation) of triple-well structure to well capacitance variation.

1) *Impact of well junction capacitance:* TEG_2WELL_5X has a larger well junction area than TEG_2WELL, and the measured voltage drop in TEG_2WELL_5X is smaller than that in TEG_2WELL in Fig. 8(a) and (b). We confirmed that the impact of well junction capacitance is comparable to that of ordinary decap insertion for supply noise suppression.
2) *Reduction of V_{ss} noise by p-substrate:* The V_{ss} noise of TEG_2WELL is smaller than that of TEG_3WELL in Fig. 8(b), and reduction of V_{ss} noise by the p-substrate is observed.
3) *Reduction of V_{dd} noise by deep n-well:* The V_{dd} noise of TEG_3WELL is reduced by 120 mV in comparison with TEG_2WELL in Fig. 8(a), and noise reduction effect of the deep n-well is observed. This reduction is due to the well junction capacitances C_{pwj} and C_{dnwj}.
4) *Supply noise reduction by triple-well:* Fig. 8(c) shows that the V_{dd}-V_{ss} drop of TEG_3WELL is smaller than that of TEG_2WELL. This confirmed that the deep n-well shows effective decoupling effect in this case.
5) *Adequacy of substrate model:* Fig. 9 shows fine correlation between measurement and simulation results. Our modeling of the power distribution network, which includes the hierarchical substrate model, is thus experimentally validated.

VI. Verification of Triple-Well Structure Utility

The effectiveness of the triple-well structure in voltage drop improvement, which was demonstrated in previous sections, is thought to be design- and technology-dependent. This section clarifies the conditions under which a triple-well structure should be used for noise suppression. We also assess the impact of well capacitance uncertainty on power integrity.

A. Discussion on Effectiveness

1) Evaluation Setup: We evaluate the effectiveness of a triple-well structure under various circuit and well conditions. In this evaluation, we focus on the amount of decap, well junction capacitance per unit length and area, and density of active cells in the digital circuit area. The decap density is set to 0%–22% of the DUT area, and active cell density of is set to 22%. The ratio of switching load capacitance, well junction capacitance, and decap (22%) is 1:2.47:2.54 in the TEST-CHIP configuration. Well capacitance is swept from 0.01 to 40× the test chip value to investigate the effect of well capacitance in various technologies and designs. The supply voltage is set to 1.0 V.

2) Noise Reduction Versus Well Capacitance: Fig. 10(a)–(c) shows, respectively, the simulation results in TEST-CHIP, ASIC, and MIXED configuration. The x-axis is well capacitance ratio and the y-axis is the decap density. The 3-D-plot of z-axis and its contour map at the bottom represent noise reduction, i.e., how much the fluctuation of the V_{dd}-V_{ss} amplitude in a triple-well structure is reduced in comparison with that in a twin-well structure. A positive value corresponds to a reduction of V_{dd}-V_{ss} amplitude fluctuation by a triple-well structure. Here, the amplitude fluctuation is defined as the difference between the maximum and minimum values of the V_{dd}-V_{ss} amplitude. The fluctuation values are normalized by corresponding absolute fluctuation values of a twin-well structure. The colored areas of the contour maps depict negative values, which are degradations of fluctuation. Our major findings were as follows:

a) a triple-well structure reduces supply fluctuation when the well capacitance ratio is over 0.1×;
b) a 20%–40% reduction of supply fluctuation is observed around 0.3–1.0× well capacitance;
c) if the digital area is sufficiently large, such as in the ASIC configuration, supply fluctuation reduction by the triple-well structure is achieved even when the well junction capacitance and the decap density are substantially changed.

3) Noise Reduction Versus Transistor Density: We next evaluate the utility of a triple-well structure for the case when transistor density is changed, i.e., total circuit capacitance, including active cell capacitance and decap, is varied. Fig. 10(d) shows transistor density versus fluctuation improvement by triple-well structure, where the transistor density ratio of the x-axis is normalized by that of the test chip. In the ASIC and MIXED configurations, the triple-well structure reduces supply noise by 30% and 10%, respectively, even when the transistor density ratio is over 5×. In the TEST-CHIP configuration, the supply noise improvement strongly depends

on the transistor density, but 10% supply noise reduction can be expected when the transistor density is smaller than 2.5×.

4) Translating Noise Reduction Into Decap Area: The noise reduction achieved thanks to the triple-well structure can contribute to reduction of the required decap. Fig. 11(a) shows the decap area corresponding to the noise reduction attained by a triple-well structure, where a 100% decap area means the entire chip area is occupied by decap. When the well capacitance is 0.3-1.0×, using a triple-well structure reduces the decap area by 5%–10%. When the well capacitance ratio is over 1.0x, a triple-well structure is equivalent to 10% of the chip area in terms of noise suppression.

5) Summary: Our experimental results indicate that a triple-well structure is effective in most CMOS designs. Under a 1× well capacitance ratio and a transistor density ratio of over 1×, the triple-well option corresponds to 5%–10% area decap insertion in the ASIC and MIXED configurations. It should be noted that the triple-well advantage is obtainable even if well capacitance decreases to 0.1× or transistor density is increased to 5×.

B. Discussion of Variation Immunity

Well capacitance variation may unexpectedly degrade the efficiency of a triple-well structure, since it is not carefully controlled by a foundry unlike MOS and metal-insulator-metal capacitance. Acceptable sensitivity of noise to well capacitance variation is an important issue for practical use.

We verify the robustness of the triple-well effect through an evaluation of peak drop sensitivity to well capacitance variation. Fig. 11(b) shows the maximum sensitivities when well capacitance is changed by 50% (1.5 or 1/1.5 times). Well junction capacitance is changed from 0.01 to 40× of the test chip well capacitance.

In an extreme case of 0% decap, the maximum sensitivity is about 50 mV. On the other hand, when decap occupies 11% or 22% of the circuit area, the sensitivity is, respectively, 20 or 10 mV, which corresponds to 2% or 1% delay variation at 1.0-V operation. Furthermore, empty space after placement and routing is often filled up with decap, and nonswitching transistors can be regarded as decap. In addition, high-performance design usually includes decap planning at the floorplanning step [14], [15]. Consequently, in most designs 11%–22% decap can be expected, and in those designs the impact of well capacitance variation is limited. We thus conclude that in common digital circuit designs, variations of well junction capacitance do not appreciably impact the noise reduction provided by a triple-well structure.

VII. Conclusion

In the work reported in this brief, we observed substantial effects of the substrate and the deep n-well on the power supply for a 90-nm test chip, and demonstrated that their effects can be explained by simulations with a simple 3-D hierarchical mesh model of the substrate and well capacitances. The V_{ss} noise was mitigated by a resistive p-substrate network. The PN junction capacitance involved in a triple-well structure also alleviated power supply noise. A triple-well structure slightly increases V_{ss} noise yet reduces V_{dd} noise more, thus it can improve the power integrity overall.

We also verified that using a triple-well structure was an effective option for reduction of supply fluctuation, and was robust to variation of well junction capacitance. We verified the effectiveness of a triple-well structure by focusing on the chip configuration, the well capacitance configuration, and the transistor density. The use of triple-well structure in experiments attained over 10%–40% reduction of supply fluctuation (corresponding to 5%–10% reduction of circuit area) and good robustness to process variation (10–20 mV even for 50% well capacitance variation). The triple-well structure was a good candidate for noise suppression without the increase in gate leakage and area overhead that accompanies decap insertion.

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