IEICE TRANS. FUNDAMENTALS, VOL.E94–A, NO.10 OCTOBER 2011

PAPER

Setup Time, Hold Time and Clock-to-Q Delay Computation under Dynamic Supply Noise*

Takaaki OKUMURA[†,††a)] ***and*** **Masanori HASHIMOTO**[†††]**,** ***Members***

SUMMARY This paper discusses how to cope with dynamic power supply noise in FF timing estimation. We first review the dependence of setup and hold times on supply voltage, and point out that setup time is more sensitive to supply voltage than hold time, and hold time at nominal voltage is reasonably pessimistic. We thus propose a procedure to estimate setup time and clock-to-Q delay taking into account given voltage drop waveforms using an equivalent DC voltage approach. Experimental results show that the proposed procedure estimates setup time and clock-to-Q delay fluctuations well with 5% and 3% errors on average.

key words: *power supply noise, Flip-Flop, setup time, hold time, timing analysis*

1. Introduction

Recently, Power/Ground voltage level fluctuation (PG noise) is becoming a primary concern in designing LSI products with the progress of technology scaling. Current density in a chip has been increasing due to increase in operating frequency and power consumption. Moreover, lowering supply voltage with technology scaling, over-drive voltage ($V_{dd} - V_{th}$) is decreasing, which results in higher sensitivity of gate delay to power supply voltage [1]. On the other hand, the authors in [2] predict that PG noise level is nearly constant despite lowering power supply voltage. These tendencies make circuit timing more susceptible to supply noise, and hence timing verification taking PG noise into account is essential for successful chip design.

Several gate delay estimation methods considering a given noise waveform have been proposed to capture the impact of dynamic noise behavior on timing [1], [3], [4]. These methods assign equivalent DC voltage to each instance by averaging the noise within a time interval of interest to eliminate dynamic behavior. Reference [3] classified the delay variation due to power noise into two categories and carefully calculates the equivalent DC voltage for rise/fall transition to reproduce the stage delay decrease as well as the stage delay increase. Then, Ref. [1] improved [3] to overcome inaccuracy originating from higher nonlinearity and sensitivity unique to advanced technology, and shows that the stage delay fluctuations can be estimated well within a few percent errors. Also, Ref. [1] shows that the method computes stage delay fluctuations of 112,000 instances by 13.3 seconds of CPU time, whereas SPICE simulation consumes 8.6 hours of CPU time.

On the other hand, under dynamic voltage drop, capturing the delay fluctuations arisen only in combinational circuits is not obviously enough for accurate timing verification, since setup and hold times of Flip-Flop (FF) also play important roles in timing verification. However, the variations of setup and hold times under dynamic voltage drop and their estimation have not been clarified.

Besides, focusing on FF setup and hold times, there are several studies on interdependence between setup and hold times [5], [6]. Conventionally, though the setup and hold times are characterized independently, Refs. [5] and [6] pointed out that the setup and hold times of an FF are interchangeable, that is, the hold time can be relaxed when the setup timing is critical, and vice versa. Furthermore, the authors in [7] experimentally compared the variations between combinational circuit delay and setup/hold times under static voltage drop, and pointed out a cancellation behavior. However, to the best of our knowledge, the variation of setup and hold times and clock-to-Q delay under dynamic voltage drop has not been discussed so far.

In this paper, we discuss how to estimate setup and hold times and clock-to-Q delay under given dynamic voltage drop. We first investigate their tendencies under static and dynamic voltage drop and show that the setup time becomes optimistic while the hold time constraint becomes pessimistic under the noise. We then propose an estimation procedure of the setup time and clock-to-Q delay under the dynamic noise on the basis of [1], and evaluate the estimation accuracy. Note that although the given noise may change according to the resultant timing fluctuations of the FFs, this paper does not cover the re-examination of the waveforms.

The rest of paper is organized as follows. In Sect. 2, we review the setup and hold times and examine the necessity/un-necessity to consider the dynamic voltage drop. In Sect. 3, we propose an estimation procedure of setup time and clock-to-Q delay under dynamic noise. Section 4 experimentally evaluates the proposed procedure and

Manuscript received October 12, 2010.
Manuscript revised May 17, 2011.

[†]The author was with Semiconductor Technology Academic Research Center, Yokohama-shi, 222-0033 Japan.
[††]The author is now with Fujitsu Semiconductor Ltd., Akiruno-shi, 197-0833 Japan.
[†††]The author is with Osaka University, Suita-shi, 565-0871 Japan.

*This paper is based on "Setup Time, Hold Time and Clock-to-Q Delay Computation under Dynamic Supply Noise," by T. Okumura and M. Hashimoto which appeared in proceeding of Custom Integrated Circuits Conference (CICC), September 2010. ©2010 IEEE.

a) E-mail: takaaki.okumura@jp.fujitsu.com

DOI: 10.1587/transfun.E94.A.1948

Sect. 5 concludes the paper.

2. Review of Setup and Hold Times

2.1 Characterization Procedure

Figure 1 shows the circuit diagram of a popular positive edge triggered FF cell [8], and this structure is evaluated throughout this paper. Similar discussion can be done for negative edge triggered flip-flops. The cell has clock signal input terminal CK, data input terminal D, and output terminal Q. When CK signal is low, the signal path consisting of instances X2 and X3 is enabled to update the value of internal node M1 to the given input signal of D, while the slave latch consisting of instances X5 and X6 outputs the internally stored value to Q. When CK signal is high, clocked inverter X2 is disabled and then the stored value in the master latch consisting of X3 and X4 is outputted to Q through X5 and X7.

Figure 2 illustrates the timing definition of setup and hold skews. The setup skew is defined as the arrival time difference between D and CK, and the hold skew is defined as the arrival time difference between CK and D. The setup time and hold time are defined in textbooks as the amount of time that a given data must be stable before the capturing clock edge and the data must remain stable after the capturing clock edge, respectively. Setup and hold times are often characterized independently as the setup and hold skews so that the increase in CK-to-Q delay remains within a certain amount of percentage (e.g. 10%) [9]. Hereafter, this allowable delay increase is called "CK-to-Q degradation criterion". As shown in Fig. 3, the CK-to-Q delay increases drastically as the skews become small. Without allowing the delay degradation, the setup and hold times would be very large. Note that the CK-to-Q delay needs to be increased simultaneously according to the degradation criterion to keep the consistencies. To explore the boundaries of allowable CK-to-Q delay, heuristic approaches, such as binary search method, are employed, which makes the FF characterization time-consuming.

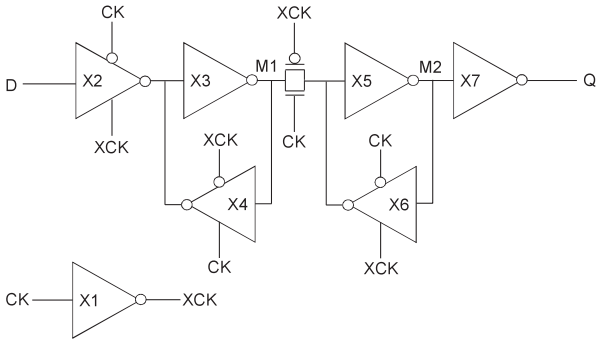

Fig. 1 Circuit diagram of positive edge triggered Flip-Flop.

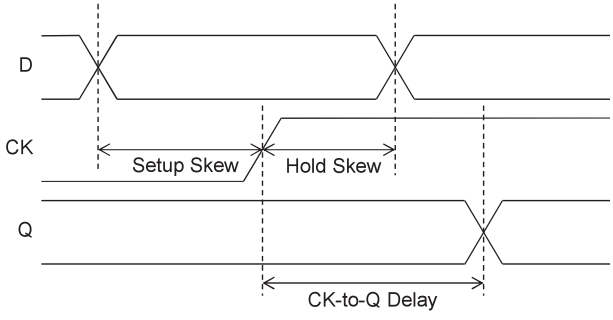

Fig. 2 Timing definitions of setup/hold skews.

2.2 Setup Time and Its Dependence on Supply Voltage

In FF of Fig. 1, the setup time is correlated with D-to-M1 delay and CK-to-XCK delay, since internal node M1 should be stable to capture the data signal safely while CK signal is low. Therefore, the setup time becomes large under the conditions when the stage delays of X2, X3, and/or X1 become large, such as large input transition time of CK or D. This is also valid for supply voltage drop.

Figure 4 plots the setup time dependence on supply voltage with several CK-to-Q degradation criteria given to the characterization. The figure shows that the setup time is

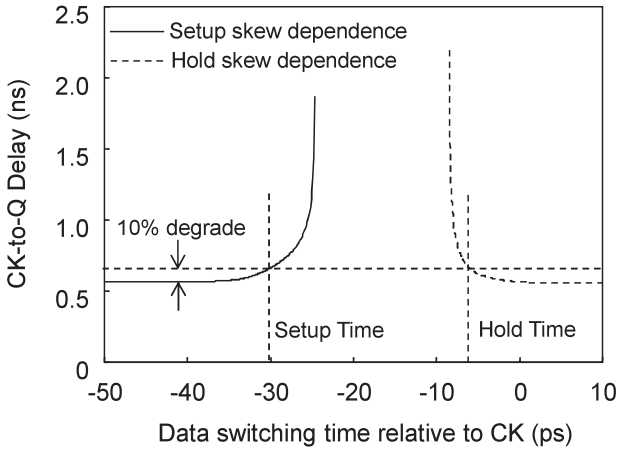

Fig. 3 Relation between CK-to-Q delay and setup/hold skews.

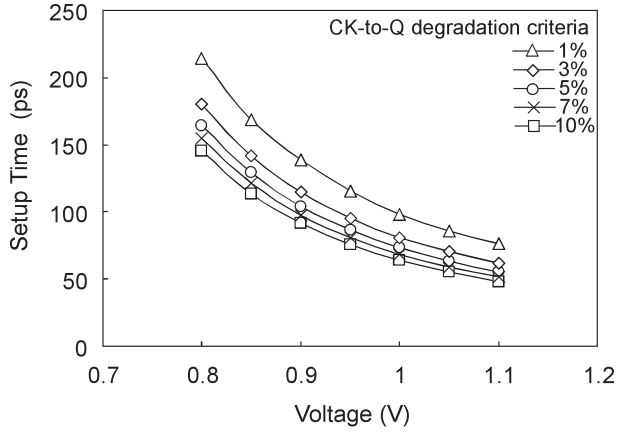

Fig. 4 Setup time dependence on supply voltage.

sensitive to supply voltage and becomes 2 to 3 times longer when the supply voltage is dropped from 1.0 to 0.8 (V). The observed tendency is independent of the CK-to-Q degradation criteria. Thus, the setup time at the nominal supply voltage is the loosest setup constraint. Hence the dependence of setup time on supply voltage should be re-examined, and an appropriate setup time must be given to STA.

2.3 Hold Time and Its Dependence on Supply Voltage

An intuitive understanding of hold time is that D should be stable before XCK is given to X2, X4 and the switch. This means that the hold time is tightly related to CK-to-XCK (X1) delay and is expected to become larger as X1 delay increases.

Figure 5 shows the hold time dependence on supply voltage with several CK-to-Q degradation criteria. Given the strict CK-to-Q degradation criterion of 1%, the hold time is positive and becomes larger as X1 delay increases according to lowering supply voltage, which is consistent with above understanding. However, with CK-to-Q degradation criterion of 5%, the hold time is insensitive to supply voltage, and above 5% the tendency becomes opposite, which means the hold time is relaxed according to supply voltage drop. Let us explain the reason.

In the cases of 7% and 10%, incomplete storing in the master latch at CK capturing edges is acceptable, as long as additional time needed to stabilize the stored value is within CK-to-Q degradation criterion. Suppose the stage delay of X1 is not large enough to dominate CK-to-Q delay with CK-to-Q typical (5–10%) criteria. In this case, the hold time could be interpreted as the time required to make the master latch stable prior to the capturing clock edge and takes negative value in this situation.

The important point here is that the amount of allowing delay degradation can be consumed in the required time to make the master latch stable and which results in the relaxation of the hold time constraint. When supply voltage becomes lower, CK-to-Q delay increase, which means the absolute value of CK-to-Q degradation criterion increases. Thus more additional time to stabilize the master latch becomes acceptable. This is why the hold time is relaxed as supply voltage decrease.

Looking at Fig. 5, revising the hold time under the dynamic voltage drop seems to be dispensable at glance, since the hold time at nominal supply voltage (here, 1.0 (V)) is not necessarily pessimistic. On the other hand, FF characterization is often carried out with CK-to-Q degradation criteria of 5 to 10% range in industry, as far as the authors know. In this range, the hold time at nominal voltage is the upper bound with reasonable pessimism, since the variation of hold time due to supply voltage is small. We thus conclude that the hold time at nominal voltage is given to STA.

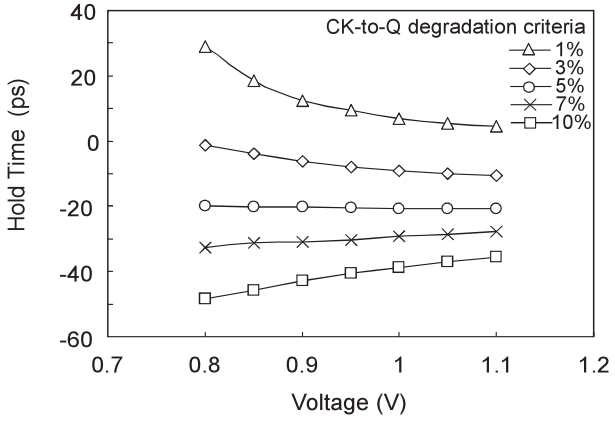

Fig. 5 Hold time dependence on supply voltage.

3. Setup Time and CK-to-Q Delay Estimation under Dynamic Voltage Drop

3.1 Setup and Hold Time Dependencies on Dynamic Voltage Drop

Figure 6 shows the setup and hold time variations when a dynamic voltage drop waveform is given. The waveform was obtained from analysis results of a commercial tool [10] and we applied it to each cell as a supply voltage. The timing of clock edge injection was alternated, and the setup and hold times for each injection timing were characterized with 10% CK-to-Q degradation criterion. In the figure, the vari-

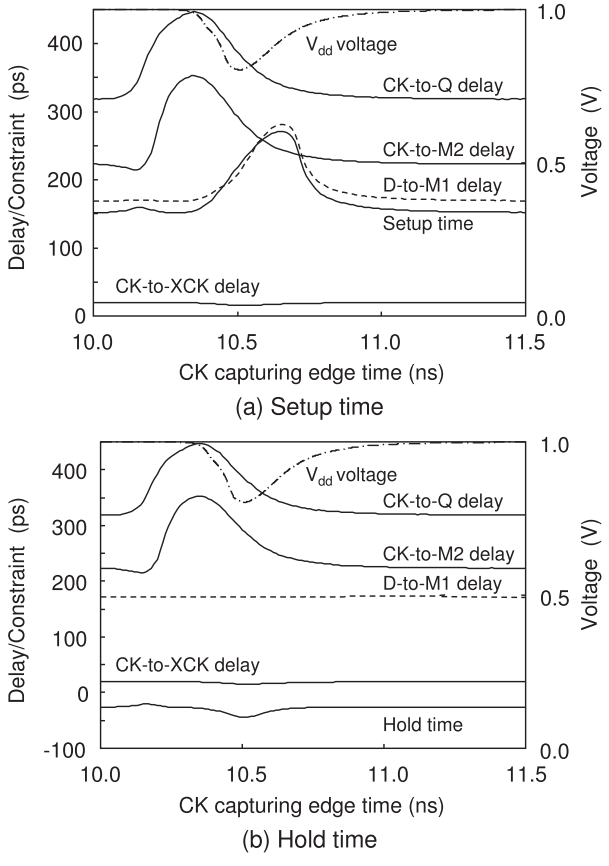

Fig. 6 Setup and hold time dependencies on dynamic voltage drop.

ation of CK-to-Q delay, CK-to-M2 delay, D-to-M1 delay, and CK-to-XCK delay are also shown.

Figure 6(a) plots the setup time variation. The figure shows that, as we discussed in Sect. 2, the setup time can be associated with CK-to-XCK delay and D-to-M1 delay (dashed line) and increases in the timing range of 10.4 to 10.9 (ns). The figure also indicates that the setup time variation is well correlated with that of D-to-M1 delay.

The hold time variation is plotted in Fig. 6(b). In the figure, hold time is less sensitive to the dynamic voltage drop than that of the setup time in Fig. 6(a). The figure also shows that the hold time is slightly relaxed due to the noise, which is consistent with the discussions in Sect. 2.

3.2 Setup Time and CK-to-Q Delay Estimation Considering Dynamic Voltage Drop

Reference [1] presents a gate delay estimation method taking into account given dynamic noise waveforms. The method derives an equivalent DC voltage V_{dd_eq} that makes the gate delay at V_{dd_eq} equal to the actual gate delay under the dynamic noise, and then computes the gate delay using V_{dd_eq}. The method computes V_{dd_eq} by integrating noise w.r.t. time.

$$V_{dd\_eq} = \frac{1}{t2 - t1} \int_{t1}^{t2} V_{dd\_actual}\, dt, \tag{1}$$

where V_{dd_actual} is the supply voltage with noise, $t1$ and $t2$ are the time when the input and output voltage swing become 50% of V_{dd}, respectively. The difficulty here is how to estimate $t2$, since $t2$ is required to compute V_{dd_eq}, and V_{dd_eq} is necessary for $t2$ computation. To deal with this problem, Ref. [1] adopts an iterative computation as shown in Fig. 7. In the figure, j is an iteration counter. T_i and D_i are an arrival time and the nominal stage delay of i_{th} stage gate. $T_{i,j}$, $\Delta v_{i,j}$, and $\Delta D_{i,j}$ are the arrival time, equivalent DC voltage drop from nominal supply voltage, and stage delay increase in the j_{th} iteration of i_{th} stage gate, respectively. Δt is the time step to increase $T_{i,j}$ during the iterations. f represents the dependence of the stage delay on supply voltage drop, and it gives the stage delay increase.

The goal of the computation is to find $t2$ satisfying that $(t2 - t1)$ equals to the stage delay $D_i + \Delta D_i$, where ΔD_i is delay variation due to noise and estimated using Eq. (1) and $t2$. Initially, $T_{i,0}(= t2)$ is set to $T_{i-1}(= t1) + D_i$. Then, in the j_{th} iteration, $T_{i,j}$ is increased by a small step Δt, and estimate $\Delta D_{i,j}$ from the function f of voltage-delay characteristics using Eq. (1). The iteration will finish if the difference between $T_{i,j} - T_{i,0}$ and $\Delta D_{i,j}$ becomes smaller than Δt.

Reference [1] also discusses the necessities of the separate treatment for rise and fall transitions to estimate the gate delay fluctuations accurately, since V_{dd} drop affects rise and fall delays with different mechanisms. On the other hand, looking at D flip-flop structure of Fig. 1, rise and fall transitions occur in pairs, i.e. X2–X3 and X5–X7. Reference [1] pointed out that path delays can be estimated well using the average supply voltage during the path operation as long as the voltage-delay sensitivity difference between the stages is insignificant. This was also experimentally validated on silicon [11]. We thus expect that the estimation procedure in Fig. 7 gives a reasonable estimate of CK-to-Q delay using the dependence on ΔV described in Ref. [1] as the function f. Here, ΔV is a static drop of input and supply voltages, and this dependence can be obtained by referring the conventional library [12].

The setup time corresponds to the stage delays of internal instances as we discussed in Sect. 2, and hence the above expectation is also applicable to the setup time estimation. However, the setup time is the time interval between data switching time and capturing clock edge, and then the procedure should be revised slightly as follows.

Initially, $T_{i,0}$ is set to $T_{ck} - T_{setup}$ where T_{ck} and T_{setup} are capturing clock edge time and setup time at nominal supply voltage, respectively. Then, in the j_{th} iteration, $T_{i,j}$ is decreased by a small step Δt and estimate $\Delta D_{i,j}$ using Eq. (1) from the setup time dependence on voltage as shown in Fig. 4. The iteration will finish if the difference between $T_{i,0} - T_{i,j}$ and $\Delta D_{i,j}$ becomes smaller than Δt.

Figure 8 shows an estimation example of the CK-to-Q delay and setup time under the dynamic voltage drop. The solid and dashed lines are the estimation results and the SPICE reference, respectively. The figure shows that the estimates are consistent with the references. This result

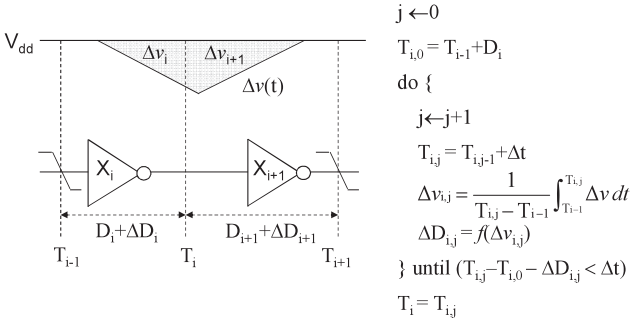

Fig. 7 An iterative procedure to obtain stage delay increase from voltage-delay characteristics.

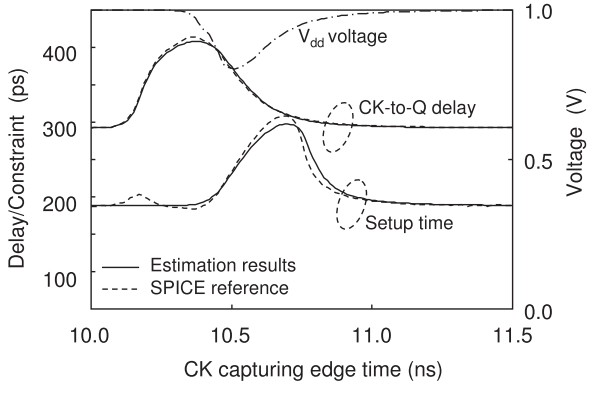

Fig. 8 Comparison between reference and estimation results of CK-to-Q delay and setup time.

suggests that the presented estimation would be applicable to cells including transfer gates, more precisely to FFs of Fig. 1 in which the delay of transfer gates is insignificant, although Ref. [1] does not discuss transfer gates. This applicability will be experimentally verified in the next section.

4. Experimental Results

We confirmed the accuracy of the estimation procedure discussed in Sect. 3 with an experimental circuit. Figure 9 depicts the experimental setup and parameter definitions, and Table 1 details the experimental conditions.

We used a 45 nm industrial design which consists of 300 K instances. The operating frequency is 100 MHz. We picked up two hundreds capture FFs on setup critical paths and extract each output load (C_L) and input transition times of CK and D ($T_{in,CK}$ and $T_{in,D}$, respectively) from commercial STA tool results [13]. We then obtained the dynamic voltage drop waveforms from analysis results of a commercial tool, and applied them as the supply voltage of each FF. In the experiments, we altered the capturing clock edge time (T_{CK}) within the first 10% of the cycle time (1ns) by 20 ps, and evaluated with 10% CK-to-Q degradation criterion at each clock edge time. The time step in the iterative computation (Δt) was set to 1 ps.

The accuracy was evaluated as the relative error which is defined as

$$Err(\%) = \frac{|Est - Ref|}{Ref} \times 100, \quad (2)$$

where *Est* and *Ref* are the results of the estimate and SPICE reference, respectively. The relative error was computed for each FF at every clock edge timing, and then for each FF the average error and standard deviations were calculated. For comparison, we also estimated setup time and CK-to-Q delay using static IR-drop which is an average voltage within a cycle time. This approach is widely used in industrial design flow.

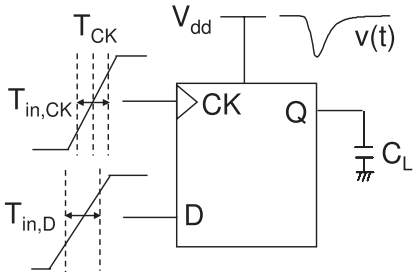

Fig. 9 Experimental setup and parameter definitions.

Table 1 Details of experimental conditions.

Parameters	Values
Technology	45nm
#Instances	300K
V_{dd}	1.0 (V)
Operating Freq.	100M (Hz)
FF	200 capture FFs on setup critical paths.
v(t)	Obtained from analysis results of a commercial tool [10].
$T_{in,CK}$, $T_{in,D}$, C_L	Extracted from the commercial STA tool results [13].
T_{CK}	First 10% cycle time (1 ns) by 20 (ps).
Δt	1 (ps)

Figure 10 plots the average of the relative errors of each FF as the function of the setup time at nominal supply voltage. As shown in the figure, the proposed method achieves smaller errors compared to "static IR-drop" method. The average errors of the proposed and "static IR-drop" methods are 5.33% and 11.4%, and the standard deviations are 0.69% and 3.0%, respectively.

Figure 11 plots the evaluation results of the CK-to-Q delay in the similar manner of Fig. 10. The figure also shows the improvement of the estimation errors by the proposed method compared to the results of "static IR-drop" method. The average errors of the proposed and "static IR-drop" methods are 3.02% and 11.1%, and the standard deviations are 0.89% and 1.89%, respectively.

The evaluation results are summarized in Table 2. As shown in the table, the proposed method can reduce the

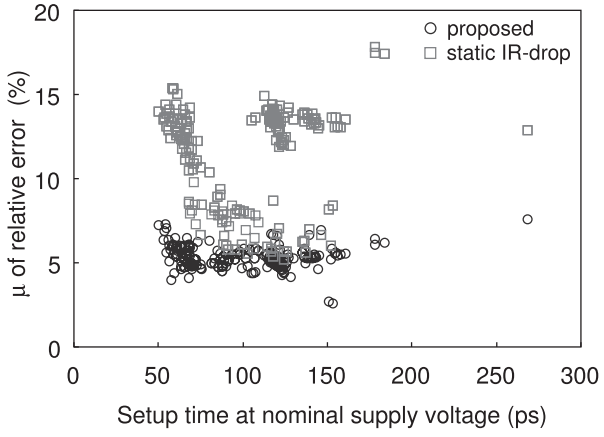

Fig. 10 Accuracy evaluation results of setup time estimation.

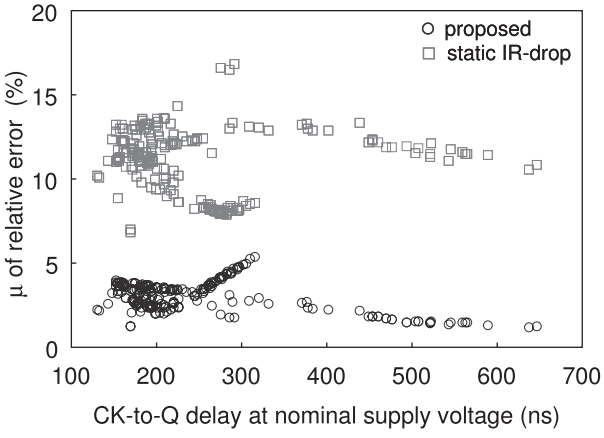

Fig. 11 Accuracy evaluation results of CK-to-Q delay estimation.

Table 2 Summary of accuracy evaluation results.

Estimation Method	Average error			
	Setup time		CK-to-Q delay	
	μ	σ	μ	σ
Proposed	5.33%	0.69%	3.02%	0.89%
static IR-drop	11.4%	3.00%	11.1%	1.89%
Improvement	53.2%	76.9%	72.8%	52.9%

estimation error of the setup time and CK-to-Q delay by more than 50% for both of averages and standard deviations, which contributes to avoid optimism in static timing analysis.

5. Conclusion

In this paper, we discussed variations of setup time, hold time and CK-to-Q delay due to dynamic voltage drop. Through experimental reviews, hold time is less sensitive to supply voltage, and with ordinary 5–10% CK-to-Q degradation criteria hold time at nominal voltage maintains reasonably conservativeness. We thus proposed a method to estimate setup time and CK-to-Q delay under dynamic voltage drop. The experimental results show that the proposed method estimates the setup time fluctuation well with 5% error on average. The proposed method can eliminate the optimism of timing estimate caused by dynamic voltage drop.

Acknowledgments

This work is supported by NEDO (New Energy and Industrial Technology Development Organization) in Japan as part of the project for the Development of Next-generation Process-friendly Design Technologies.

References

[1] T. Okumura, F. Minami, K, Shimazaki, K. Kuwada, and M. Hashimoto, "Gate delay estimation in STA under dynamic power supply noise," IEICE Trans. Fundamentals, vol.E93-A, no.12, pp.2447–2455, Dec. 2010.
[2] A. Mezhiba and E. Friedman, "Scaling trends of on-chip power distribution noise," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol.12, no.4, pp.386–394, April 2004.
[3] M. Hashimoto, J. Yamaguchi, T. Sato, and H. Onodera, "Timing analysis considering temporal supply voltage fluctuation," Proc. ASP-DAC, pp.1098–1101, 2005.
[4] K. Shimazaki, M. Fukazawa, M. Miyahara, M. Hirata, K. Sato, and H. Tsujikawa, "An integrated timing and dynamic supply noise verification for nano-meter CMOS SoC designs," Proc. CICC, pp.31–34, 2005.
[5] A.M. Jain and D. Blaauw, "Modelling flip-flop delay dependences in timing analysis," Proc. TAU, pp.67–73, 2004.
[6] E. Salman, A. Dasdan, F. Taraporevala, K. Kucukcakar, and E.G. Friedman, "Exploiting setup-hold-time interdependence in static timing analysis," IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol.26, no.6, pp.1114–1125, June 2007.
[7] E. Salman and E.G. Friedman, "Methodology to achieve higher tolerance to delay variations in synchronous circuits," Proc. GLSVLSI, pp.447–452, 2010.
[8] M.J. S. Smith, Application-specific integrated circuits, Addison-Wesley Longman Publishing, 1998.
[9] Altos Design Automation Inc., "Liberate user guide," Ver. 2.4, Aug. 2009.
[10] Apache Design Solutions Inc, "RedHawk users' manual," 2007.1B ed., Feb. 2008.
[11] Y. Ogasawara, T. Enami, M. Hashimoto, T. Sato, and T. Onoye, "Validation of a full-chip simulation model for supply noise and delay dependence on average voltage drop with on-chip delay measurement," IEEE Trans. Circuit Syst. II, vol.54, no.10, pp.868–872, Oct. 2007.
[12] Synopsys Inc., "Liberty user guide," 2009.06 ed., 2009.
[13] Synopsys Inc., "Primetime user guide," A-2007.12 ed., Dec. 2007.

Takaaki Okumura received the B.S. and M.S. degrees in information engineering from Shinshu University, Nagano, Japan, in 1986 and 1988, respectively. He is with Fujitsu VLSI Ltd., Kasugai, Japan, from 1988. From 2008 to 2011, he was on loan to Semiconductor Technology Academic Research Center (STARC). He is now on loan to Fujitsu Semiconductor Ltd.

Masanori Hashimoto received the B.E., M.E. and Ph.D. degrees in Communications and Computer Engineering from Kyoto University, Kyoto, Japan, in 1997, 1999, and 2001, respectively. Since 2004, he has been an Associate Professor in Department of Information Systems Engineering, Graduate School of Information Science and Technology, Osaka University. His research interest includes computer-aided-design for digital integrated circuits, and high-speed circuit design. He is a member of IEEE and IPSJ.