Neutron-Induced Soft Errors and Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM

Hiroshi Fuketa, *Member, IEEE*, Masanori Hashimoto, *Member, IEEE*, Yukio Mitsuyama, *Member, IEEE*, and Takao Onoye, *Senior Member, IEEE*

***Abstract*—In this paper, the soft error rate (SER) induced by neutrons in 65-nm 10T static random access memory (SRAM) is measured over a wide range of supply voltages from 1.0 to 0.3 V. The results show that the neutron-induced SER at 0.3 V is around eight times that at 1.0 V. The dependence of multiple cell upsets (MCUs) on the supply voltage and on the distance between well ties is also investigated. The dependence of the MCU rate on the supply voltage between 1.0 and 0.5 V is small and increases as the voltage is reduced below 0.5 V. This is because the effect of another mechanism, such as charge-sharing, becomes larger in the subthreshold region, rather than the parasitic bipolar effect, which is considered the dominant mechanism causing MCUs in SRAM at the nominal supply voltage in our design.**

***Index Terms*—Multiple cell upset, neutron-induced soft error, soft error rate, subthreshold circuit.**

I. Introduction

An aggressive voltage scaling down to the threshold voltage of MOSFETs can significantly reduce power dissipation [1]. Therefore, subthreshold circuits that operate at a lower supply voltage than the threshold voltage are promising for ultra-low power applications, such as processors for sensor networks [2], [3] and medical applications [4]. However, subthreshold circuits are extremely sensitive to manufacturing variability and environmental fluctuation, such as temperature, due to the exponential dependence of the subthreshold characteristics of MOSFETs on the threshold voltage. This sensitivity has been a major concern, and many researchers have investigated ways to cope with it [5], [6]. However, little attention has been paid to the vulnerability of subthreshold circuits to radiation particles.

Studies have shown that the neutron-induced soft error rate (SER) in static random access memory (SRAM) increases as the supply voltage is lowered [7], [8]. This is because reducing the supply voltage reduces the energy required to cause upsets. These studies, however, were done using a voltage between the nominal supply voltage and 0.8 V. If the SER in the subthreshold region was much larger than that in the super-threshold (nominal supply voltage) region, it would not be appropriate to use subthreshold circuits in actual applications. Therefore, subthreshold circuits need to be made immune to soft errors. Casey *et al.* analyzed single event transients (SETs) in the subthreshold region using ring oscillators [9], and Mostafa *et al.* analytically examined the vulnerability to radiation particles of SRAM operating in the subthreshold region [10]. Although alpha-particle-induced SER in subthreshold SRAM has been measured [11], neutron-induced SER has not been measured.

This paper presents the first work to measure neutron-induced soft errors in SRAM over a wide range of supply voltages between 1.0 and 0.3 V. Since conventional 6T SRAM, which is used in commercial off-the-shelf SRAMs, can barely function in the subthreshold region due to weak writability and read instability [12], [13], we use 10T SRAM [11], which can operate even at 0.3 V. Accelerated SER measurements using a neutron beam showed that the neutron-induced SER at 0.3 V is 7.8 times higher than at 1.0 V.

In addition, many researchers have pointed out that the occurrence of multiple cell upsets (MCUs) induced by a single neutron is a serious concern [8], [14], [15]. Although the dependence of MCUs induced by alpha particles on the supply voltage in the subthreshold region has been measured [11], neutron-induced MCUs in the subthreshold region have not been investigated.

We examine the neutron-induced MCUs at supply voltages between 1.0 and 0.3 V. While previous investigations [15]–[18] found that the major mechanism of MCUs in SRAM is the parasitic bipolar effect at the nominal supply voltage, the importance of the parasitic bipolar effect depends on technology, well structure (twin well or triple well), and cell layout style [19]. We, in this paper, investigate the dependence of MCUs on the distance between well ties to clarify the contribution of the parasitic bipolar effect in our design. The measurement results indicate that the parastic bipolar effect strongly contributes the occurrence of MCUs in the super-threshold region.

Furthermore, previous researches on the parasitic bipolar effect [15]–[18] were peformed in the super-threshold region. Therfore, it is not clear whether the parasitic bipolar effect contributes the occurrence of MCUs even in the subthreshold region or not. We examine the dependence of MCUs on the supply voltage, and reveal that while the dependence of MCUs on the supply voltage between 1.0 and 0.5 V is small, the MCU rate slightly increases below 0.5 V. We conclude that this is because the effect of another mechanism, such as charge-sharing

Manuscript received March 28, 2011; revised May 24, 2011; accepted June 09, 2011. Date of publication July 29, 2011; date of current version August 17, 2011. This work was supported in part by the New Energy and Industrial Technology Development Organization (NEDO) of Japan.

H. Fuketa is with the Institute of Industrial Science, University of Tokyo, Tokyo 153-8505, Japan (e-mail: fuketa@iis.u-tokyo.ac.jp).

M. Hashimoto, Y. Mitsuyama, and T. Onoye are with the Department of Information Systems Engineering, Osaka University, Osaka 565-0871, Japan and also with JST, CREST, Tokyo 102-0075, Japan (e-mail: hasimoto@ist.osaka-u.ac.jp; mituyama@ist.osaka-u.ac.jp; onoye@ist.osaka-u.ac.jp).

Digital Object Identifier 10.1109/TNS.2011.2159993

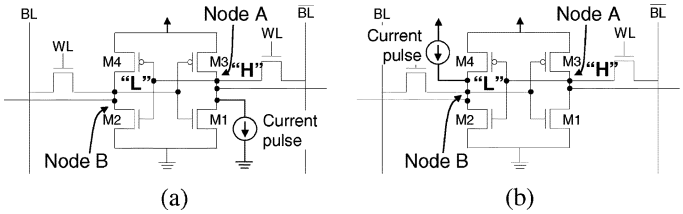

Fig. 1. Setup for simulations used to obtain critical charge of memory cell with current pulse induced by radiation particles. (a) strike on "Node A", (b) strike on "Node B".

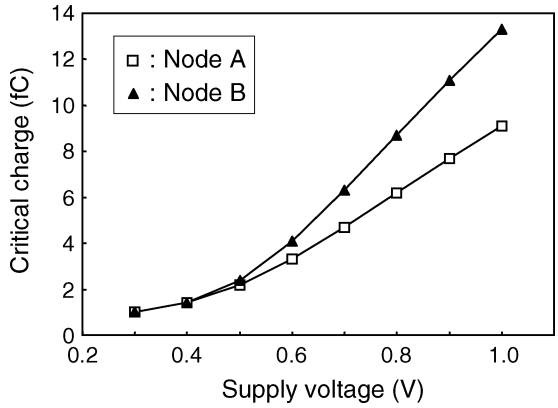

Fig. 2. Simulated critical charge of 10T memory cell as a function of supply voltage in 65 nm CMOS process.

[20] rather than the parasitic bipolar effect, is larger in the subthreshold region. In this paper, charge-sharing means the charge induced by a single neutron hit diffuses to multiple nodes.

The remainder of this paper is organized as follows. In Section II, the dependence of the critical charge on the supply voltage as revealed by simulation is described. Section III describes the structure of the subthreshold SRAM used to measure SERs over a wide range of supply voltages. The measurement results are presented in Section IV. Section V concludes with a summary of the key points.

II. Critical Charge Dependence on Supply Voltage

When radiation particles such as neutrons strike a transistor, a current pulse is generated. Conventionally, the current pulse is expressed as [21],

$$i(t) = \frac{Q}{\tau_f - \tau_r}(e^{-t/\tau_f} - e^{-t/\tau_r}), \tag{1}$$

where Q is the total collected charge and τ_r (τ_f) is the rising (falling) time constant.

The vulnerability of a memory cell to radiation particles is often evaluated using the critical charge, which is defined as the minimum charge required to flip the data stored in a memory cell. We obtained the critical charge by simulation of the current pulse (1) as depicted in Fig. 1. Two cases were considered; 1) particles strike "Node A," which is pulled up to $V_{\rm DD}$ (Fig. 1(a)), 2) particles strike "Node B," which is pulled down to the ground (Fig. 1(b)). Although a radiation-induced current can differ from (1) [23], we simply focused on the relative dependence of the critical charge on the supply voltage as the absolute values were not important for our investigation. Hence, an investigation using (1) is still expected to be reasonable.

Fig. 2 shows the critical charge of the 10T memory cell used to evaluate SER (see Section III) as a function of the supply voltage, when τ_r and τ_f in (1) were set to 1 and 50 ps, respectively, in accordance with the model of Jahinuzzaman *et al.* [21]. In our design, PMOSs (M3 and M4 in Fig. 1) of the cross-coupled inverters in the memory cell is weaker than NMOSs (M1 and M2 in Fig. 1) from 0.3 to 1.0 V. Thus, the critical charge in Node B, which is pulled down to the ground by NMOS (M2), is larger than that in Node A, which is pulled up to VDD by PMOS (M3). Fig. 2 shows that the critical charge decreases as the supply voltage is reduced. This means that a reduction in the supply voltage degrades immunity to radiation particles, such as neutrons.

III. Structure of Test Chip

A 256 kb 10T SRAM was fabricated in a 65-nm CMOS process with tripple well structure to measure neutron-induced soft errors. The circuit structure of the SRAM is shown in Fig. 3. The circuit consists of an I/O circuit, a control logic, and 16 memory blocks. Each memory block consists of two 8-kb memory cell arrays. A bit-interleaving technique is not used in the memory cell arrays.

The supply voltage of the I/O circuit was set to the nominal supply voltage ("VDDH" in Fig. 3). The control logic, which connects signals between the memory cell arrays and the I/O circuit, operates at the intermediate supply voltage ("VDDM" in Fig. 3). The memory cell arrays operate over a wide range of supply voltages, from 0.3 to 1.0 V ("VDDL" in Fig. 3). For example, when VDDL was 0.3 V, VDDM and VDDH were set to 0.6 and 1.2 V, respectively.

To measure the SER over a wide range of supply voltages, we used the 10T memory cell described in [11]. Fig. 4 shows the structure of the memory cell. The size of the unit cell is 0.8 μm $\times$ 4.4 μm, and the 6T area (M1–M6) occupies 80% of the total (10T) area because the cross-coupled inverters (M1–M4) were made large enough to mitigate threshold voltage variability. Furthermore, the word lines (WLs) are driven at a higher voltage ("VWRITE" in Fig. 3) than the supply voltage of the memory cell arrays in order to attain strong writability, which is similar to the so-called "boosted word line" technique [24], [25]. In this paper, VWRITE was consistently set to VDDL + 0.1 V. VFOOT (Fig. 4) is used to ensure correct read operation in the subthreshold region [24]. The VFOOT of the accessed word is set to low and those of the unaccessed words remain high.

In addition, in order to investigate the contribution of the parasitic bipolar effect to the occurrence of MCUs, we implemented two types of memory cell arrays, as shown in Fig. 3. The distance between the well ties of the left memory cell arrays is wide (25.6 μm), while that of the right memory cell arrays is narrow (6.4 μm). Fig. 5 illustrates the bipolar effect. Holes generated by a neutron-induced nuclear reaction increase the voltage of

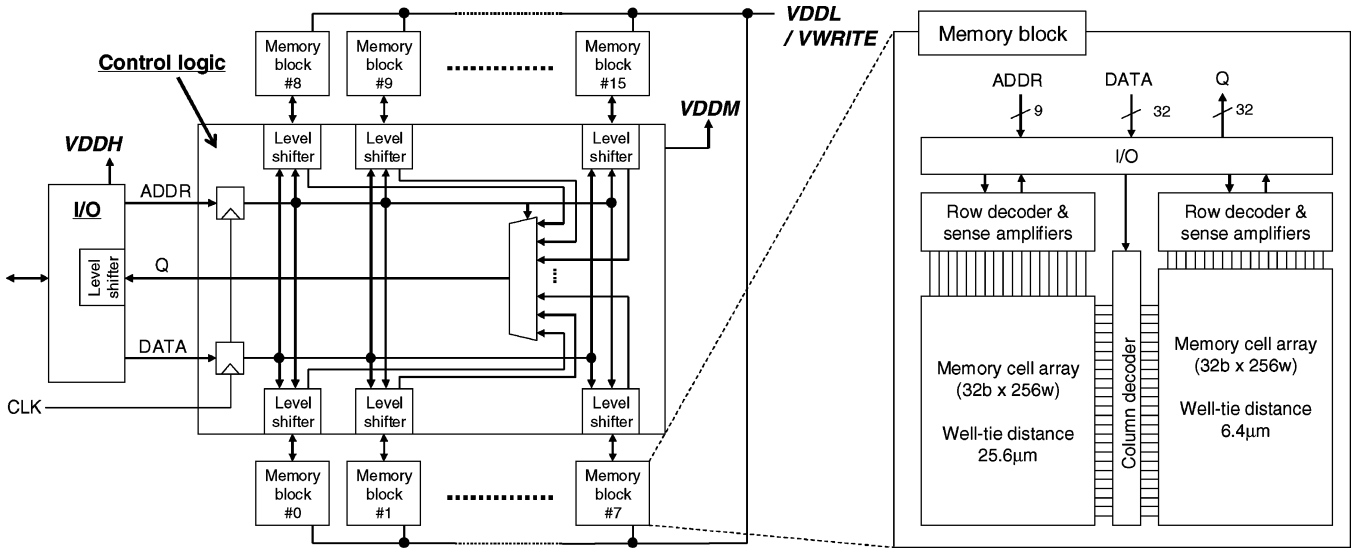

Fig. 3. Circuit structure of test chip consisting of I/O circuit, control logic, and memory blocks. Two types of memory cell arrays are implemented; the distance between the well ties of the left memory cell arrays is wide (25.6 μm) and that of the right memory cell arrays is narrow (6.4 μm).

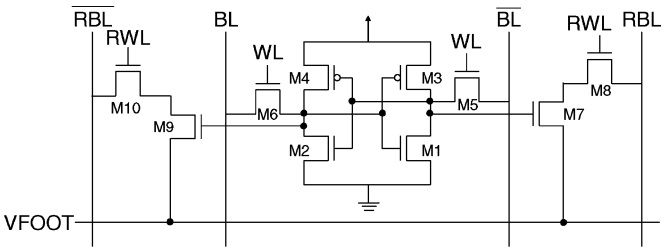

Fig. 4. Structure of 10T memory cell [11].

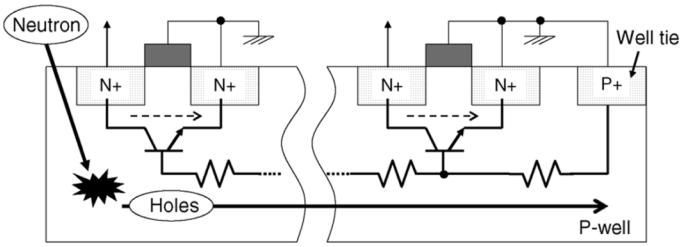

Fig. 5. Cross section of NMOSs in memory cells. Parasitic bipolar transistors cause multiple upsets due to increase in potential of p-well.

the p-well, which is equivalent to the base-emitter voltages of the parasitic bipolar transistors, due to well resistance. Consequently, the collector-emitter currents of the parasitic bipolar transistors increase, which causes MCUs. This means that the occurrence of MCUs depends on the distance between well ties [16] since the well resistance inducing the base-emitter voltage increases with the distance between well ties.

A micrograph of the test chip is shown in Fig. 6.

IV. Experimental Results

A. Experimental Setup

Accelerated high-energy-neutron SER measurements were performed at the Research Center for Nuclear Physics (RCNP)

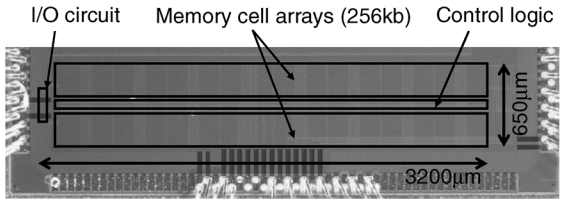

Fig. 6. Micrograph of test chip.

at Osaka University, Japan [8]. The energy spectrum of the RCNP neutron source is similar to the terrestrial neutron energy spectrum [8], [15]. The flux was estimated to be 2.3×10^9 $\mathrm{cm^{-2}h^{-1}}$, which is 1.6×10^8 times larger than that of terrestrial cosmic neutrons. The minimum neutron energy used in the calculation of this acceleration factor is 10 MeV [15].

Using the neutron beam, we tested 31 chips with a total of 7.75 Mb of memory cells. All the memory cells were functional between 0.5 and 1.0 V. When the supply voltage was reduced to 0.3 V, 924 memory cells (0.01% of the total cells) did not work correctly and hence were excluded from the measurements.

We first wrote zero to all bits ("ALL0" data pattern). Then, all the stored data were read every 60 seconds, and each bit was checked to see if it had flipped. Performance of these two steps for each supply voltage enabled us to obtain the dependence of SER on the supply voltage.

The occurrence of MCUs in adjacent bits depends on the written data pattern [11]. Fig. 7 shows the physical layout of adjacent cells when the data pattern written was "ALL0." Adjacent sensitive nodes along the WLs are on different well potentials. With this configuration, multiple upsets belonging to the same word rarely occur since neutron-induced MCUs are mainly caused by the bipolar effect (discussed in Section IV.B), and the distance between the sensitive nodes in adjacent rows is 1/5 less than those in the adjacent columns, as shown in Fig. 7. Therefore, we focus on MCUs occurring in adjacent bits along bit lines (BLs). The definition of single bit upset (SBU) and MCU is illustrated in Fig. 8.

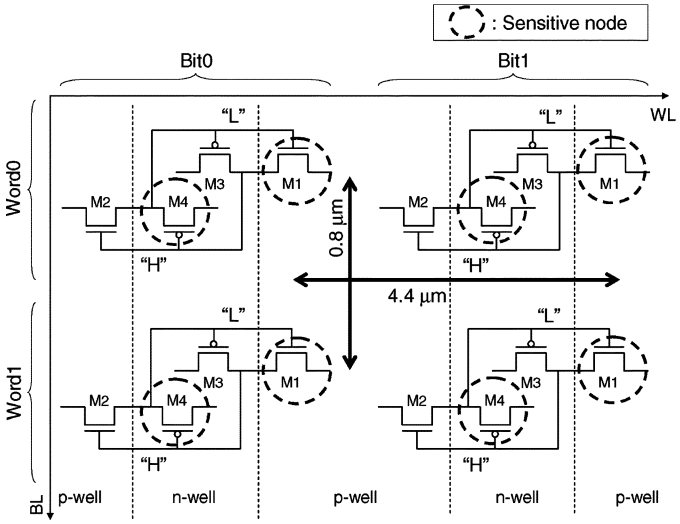

Fig. 7. Physical layout of adjacent memory cells. Value stored in each cell was zero. Note that only cross-coupled inverters (M1–4 in Fig. 4) are shown in this figure.

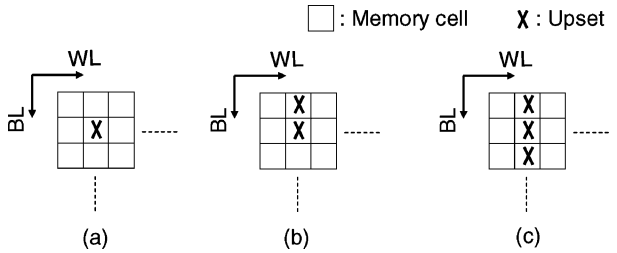

Fig. 8. Definition of single bit upset (SBU) and multiple cell upset (MCU).

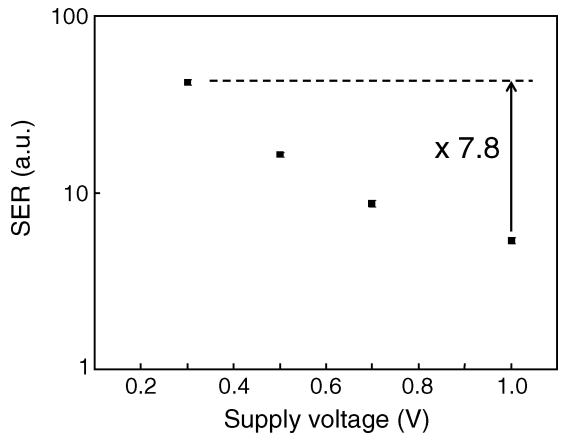

Fig. 9. SER as a function of supply voltage of memory cell array. Each error bar indicates $\pm 3\sigma$, where σ is defined as the square root of the number of the observed upsets.

B. Measurement Results

Fig. 9 shows the neutron-induced SER as a function of the supply voltage. The SER increases as the supply voltage is reduced. The SER at 0.3 V is 7.8 times higher than at 1.0 V. The ratio of this increase is almost the same as that due to alpha particles, as reported in [11]. Note that the slope of the SER with respect to the supply voltage is steeper when the supply voltage is less than 0.7 V, as depicted in Fig. 9, whereas the slope is almost constant for alpha-particle-induced SER.

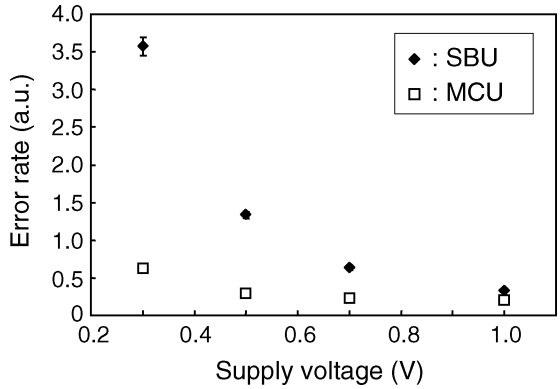

Fig. 10. SBU and MCU rates as a function of supply voltage of memory cell array. SBU and MCU rates are plotted with error bars, where each error bar indicates $\pm 3\sigma$.

Fig. 10 illustrates the dependence of the SBU and MCU rates on the supply voltage. The MCU rate was derived by dividing the number of failing bits (for example, a "2b MCU" was considered to be two errors) by the measurement period. The SBU rate dramatically increases as the supply voltage is reduced. As described in Section II (Fig. 2), the decrease in the supply voltage reduces the critical charge. Ibe *et al.* [22] reported that SBU is dominated more significantly as scaling proceeds due to lighter particles such as protons, which are secondary particles produced by the nuclear reaction between neutrons and Si. Although rigidly speaking the reduction in the supply voltage and the device miniaturization are different in terms of the sensitive volume and the charge collection efficiency, the supply voltage reduction corresponds to the device miniaturization in terms of the critical charge. Therefore, the drastic increase in SBU shown in Fig. 10 is attributed to secondary particles such as protons.

On the other hand, the dependence of the MCU rate on the supply voltage is smaller than that of the SBU rate. Contributions of lighter particles such as protons to MCUs are less than those to SBUs [22]. Previous work [15] has shown that the MCU rate is less sensitive to the supply voltage between 1.2 and 0.7 V and concluded that this is because most neutron-induced MCUs are caused by the parasitic bipolar effect. Interestingly, however, the MCU rate shown in Fig. 10 slightly increases when the supply voltage is below 0.5 V.

To examine this phenomenon, we focus on the distance between well ties. Figs. 11 and 12 illustrate the dependence of the SBU and MCU rates on the well-tie distance. There is no significant difference between the SBU rates for the memory cells with a narrow well-tie distance and those for ones with a wide well-tie distance. In contrast, the MCU rates depend on the well-tie distance. Fig. 12 also shows the ratio of the MCU rate for the memory cells with a narrow well-tie distance to that for those with a wide well-tie distance. Notably, the MCU rate for the memory cells with a wide well-tie distance is always higher than that for ones with a narrow well tie distance, yet the dependence of the MCU rate on the well-tie distance decreases with the supply voltage.

This indicates that the parastic bipolar effect strongly contributes the occurrence of MCUs in our design when the supply

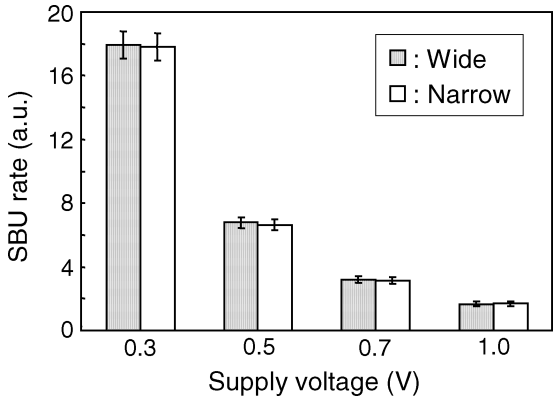

Fig. 11. Dependence of SBU rates on distance between well ties. Each error bar indicates $\pm 3\sigma$.

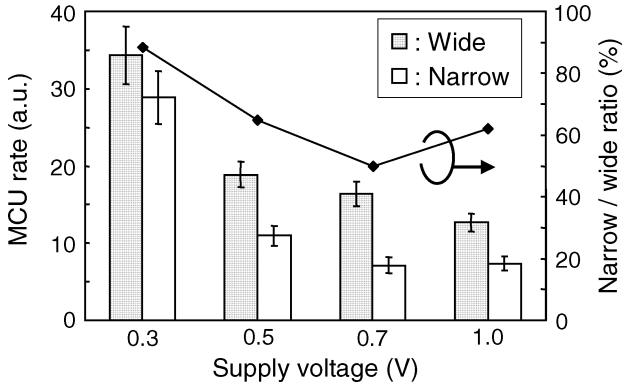

Fig. 12. Dependence of MCU rates on distance between well ties. Line plot represents ratio of MCU rate for memory cells with narrow well-tie distance to that for ones with wide well-tie distance. Each error bar indicates $\pm 3\sigma$.

voltage is more than 0.5 V, and the contribution becomes relatively small in the subthreshold region. Instead, another mechanism has a larger effect on the MCU rate for the following reasons:

- When the supply voltage is below 0.5 V, MCUs induced by the parasitic bipolar effect decrease because the collector-emitter current of the bipolar transistor falls due to the reduction in the collector-emitter voltage.
- [11] reported that alpha-particle-induced MCUs sharply increase when the supply voltage falls below 0.6 V. This increase is mainly caused by "charge-sharing" [20] due to a decrease in the critical charge, as shown in Fig. 2. Therefore, it is possible that the effect of neutron-induced MCUs due to charge-sharing also increases as the supply voltage is reduced.

We conclude that, while the parasitic bipolar effect is the dominant mechanism of MCUs in the super-threshold region in our design, the effect of charge-sharing becomes larger in the subthreshold region, which results in the increase in the MCU rate between 0.3 and 0.5 V, as depicted in Fig. 10.

Fig. 13 shows the ratio of MCUs to total upsets as a function of the supply voltage. For alpha-particle-induced MCUs, a reduction in the supply voltage increases the ratio [11]. However, as shown in Fig. 13, the ratio of neutron-induced MCUs decreases as the supply voltage is reduced. This is because the

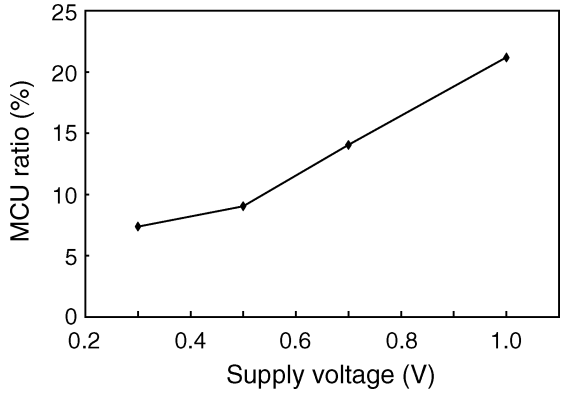

Fig. 13. Ratio of MCUs to total upsets as a function of supply voltage.

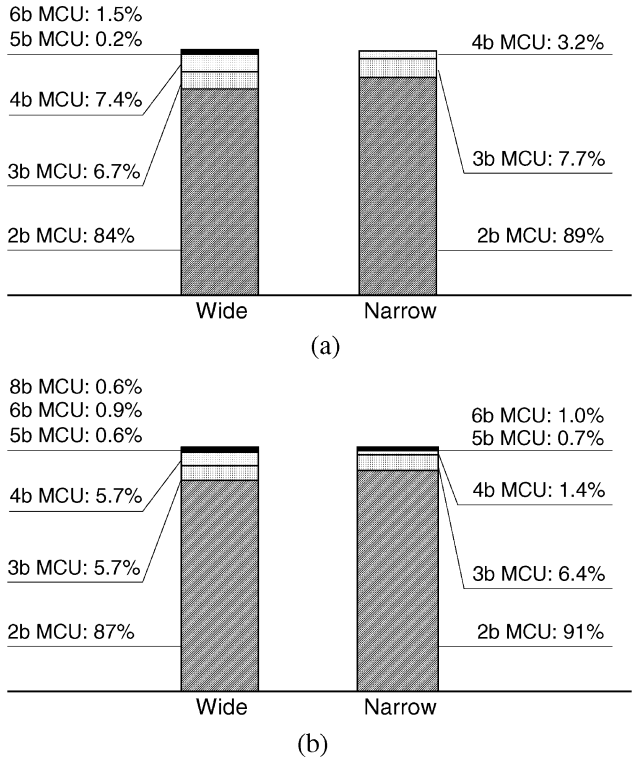

Fig. 14. Comparison of MCU distributions. (a) $V_{\rm DD} = 1.0$ V, (b) $V_{\rm DD} = 0.3$ V.

SBU rate dramatically increases as the supply voltage is reduced, whereas the increase in the MBU rate is relatively small.

Finally, the MCU distributions in the memory cells with wide and narrow well-tie distances are shown in Fig. 14. Large-bit MCUs are likely to occur in memory cells with a wide well-tie distance compared to ones with a narrow well-tie distance. A decrease in the supply voltage also increases the probability of large-bit MCUs due to the decrease in the critical charge.

V. Conclusion

Our measurements of the neutron-induced soft error rate (SER) in 65-nm 10T SRAM between 1.0 and 0.3 V revealed that the neutron-induced SER at 0.3 V is 7.8 times higher than at 1.0 V and that the single bit upset (SBU) rate dramatically increases as the supply voltage is lowered. Our investigation of

the dependence of multiple cell upsets (MCUs) on the supply voltage and on the distance between well ties showed that the dependence of the MCU rate on the supply voltage between 1.0 and 0.5 V is small and that the MCU rate slightly increases when the supply voltage is below 0.5 V. This is because the parasitic bipolar effect is the dominant mechanism of MCUs in the super-threshold region in our design, whereas the effect of another mechanism, such as the charge-sharing, becomes larger in the subthreshold region.

ACKNOWLEDGMENT

This research was performed by the authors for STARC as part of the Japanese Ministry of Economy, Trade and Industry sponsored "Next-Generation Circuit Architecture Technical Development" program. The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with STARC, e-Shuttle, Inc., and Fujitsu Ltd.

The authors would like to thank Prof. K. Takahisa and Prof. K. Hatanaka of RCNP, Osaka University, for their assistance, and Dr. Ibe of Hitachi Ltd. for making our discussions with him very fruitful.

REFERENCES

[1] A. W. Wang, B. H. Calhoun, and A. P. Chandrakasan, *Sub-Threshold Design For Ultra Low-Power Systems*. New York: Springer, 2006.

[2] G. Chen, M. Fojtik, D. Kim, D. Fick, J. Park, M. Seok, M. Chen, Z. Foo, D. Sylvester, and D. Blaauw, "Millimeter-scale nearly perpetual sensor system with stacked battery and solar cells," in *Proc. Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2010, pp. 288–289.

[3] N. Ickes, D. Finchelstein, and A. P. Chandrakasan, "A 10-pJ/instruction, 4-MIPS micropower DSP for sensor applications," in *Proc. Asian Solid-State Circuits Conf.* , Fukuoka, Japan, 2008, pp. 289–292.

[4] S. Sridhara, M. DiRenzo, S. Lingam, S. J. Lee, R. Blazquez, J. Maxey, S. Ghanem, Y. H. Lee, R. Abdallah, P. Singh, and M. Goel, "Microwatt embedded processor platform for medical system-on-chip applications," in *Proc. Int. Symp. VLSI Circuits Dig. Tech. Papers*, 2010, pp. 15–16.

[5] H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "Adaptive performance compensation with in-situ timing error prediction for subthreshold circuits," in *Proc. Custom Integrated Circuits Conf.*, San Jose, CA, 2009, pp. 215–218.

[6] I. J. Chang, S. P. Park, and K. Roy, "Exploring asynchronous design techniques for process-tolerant and energy-efficient subthreshold operation," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 401–410, Feb. 2010.

[7] P. Hazucha, T. Karnik, J. Maiz, S. Walstra, B. Bloechel, J. Tschanz, G. Dermer, S. Hareland, P. Armstrong, and S. Borkar, "Neutron soft error rate measurements in a 90-nm CMOS process and scaling trends in SRAM from 0.25-mm to 90-nm generation," in *Proc. Int. Electron Device Meeting Tech. Dig.*, 2003, pp. 21.5.1–21.5.4.

[8] Y. Tosaka, H. Ehara, M. Igeta, T. Uemura, H. Oka, N. Matsuoka, and K. Hatanaka, "Comprehensive study of soft errors in advanced CMOS circuits with 90/130 nm technology," in *Proc. Int. Electron Device Meeting Tech. Dig.*, 2004, pp. 38.3.1–38.3.4.

[9] M. C. Casey, B. L. Bhuva, S. A. Nation, O. A. Amusan, T. D. Loveless, L. W. Massengill, D. McMorrow, and J. S. Melinger, "Single-event effects on ultra-low power CMOS circuits," in *Proc. Int. Reliability Phys. Symp.*, Montreal, QU, Canada, 2009, pp. 194–198.

[10] H. Mostafa, M. H. Anis, and M. Elmasry, "Analytical soft error models accounting for die-to-die and within-die variations in sub-threshold SRAM cells," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, pp. 182–195, Feb. 2011.

[11] H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "Alpha-particle-induced soft errors and multiple cell upsets in 65-nm 10T subthreshold SRAM," in *Proc. Int. Reliability Physics Symp.*, Anaheim, CA, 2010, pp. 213–217.

[12] M. Yamaoka, N. Maeda, Y. Shinozaki, Y. Shimazaki, K. Nii, S. Shimada, K. Yanagisawa, and T. Kawahara, "Low-power embedded SRAM modules with expanded margins for writing," in *Proc. Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2005, pp. 480–481.

[13] B. H. Calhoun and A. Chandrakasan, "A 256-kb 65-nm sub-threshold SRAM design for ultra-low-voltage operation," *IEEE J. Solid-State Circuits*, vol. 42, pp. 680–688, Mar. 2007.

[14] E. Ibe, S. S. Chung, S. Wen, H. Yamaguchi, Y. Yahagi, H. Kameyama, S. Yamamoto, and T. Akioka, "Spreading diversity in multi-cell neutron-induced upsets with device scaling," in *Proc. Custom Integrated Circuits Conf.*, San Jose, CA, 2006, pp. 437–444.

[15] T. Nakauchi, N. Mikami, A. Oyama, H. Kobayashi, H. Usui, and J. Kase, "A novel technique for mitigating neutron-induced multi-cell upset by means of back bias," in *Proc. Int. Reliability Physics Symp.*, Phoenix, AZ, 2008, pp. 187–191.

[16] G. Gasiot, S. Uznanski, and P. Roche, "SEE test and modeling results on 45 nm SRAMs with different well strategies," in *Proc. Int. Reliability Phys. Symp.*, Anaheim, CA, 2010, pp. 407–410.

[17] K. Osada, K. Yamaguchi, Y. Saitoh, and T. Kawahara, "Cosmic-ray multi-error immunity for SRAM, based on analysis of the parasitic bipolar effect," in *Proc. Int. Symp. VLSI Circuits Dig. Tech. Papers*, 2003, pp. 255–258.

[18] G. Gasiot, P. Roche, and P. Flatresse, "Comparison of multiple cell upset response of bulk and SOI 130 nm technologies in the terrestrial environment," in *Proc. Int. Reliability Physics Symp.*, Phoenix, AZ, 2008, pp. 192–194.

[19] G. Gasiot, D. Giot, and P. Roche, "Multiple cell upsets as the key contribution to the total SER of 65 nm CMOS SRAMs and its dependence on well engineering," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2468–2473, Dec. 2007.

[20] O. A. Amusan, A. F. Witulski, L. W. Massengill, B. L. Bhuva, P. R. Fleming, M. L. Alles, A. L. Sternberg, J. D. Black, and R. D. Schrimpf, "Charge collection and charge sharing in a 130 nm CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3253–3258, Dec. 2006.

[21] S. M. Jahinuzzaman, M. Sharifkhani, and M. Sachdev, "An analytical model for soft error critical charge of nanometric SRAMs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, pp. 1187–1195, Sept. 2009.

[22] E. Ibe, H. Taniguchi, Y. Yahagi, K. Shimbo, and T. Toba, "Impact of scaling on neutron-induced soft error in SRAMs from a 250 nm to a 22 nm design rule," *IEEE Trans. Electron Devices*, vol. 57, pp. 1527–1538, Jul. 2010.

[23] R. Garg and S. P. Khatri, "3D simulation and analysis of the radiation tolerance of voltage scaled digital circuit," in *Proc. IEEE Int. Conf. Computer Design*, Las Vegas, NV, 2009, pp. 498–504.

[24] N. Verma and A. Chandrakasan, "A 65 nm 8T sub-vt SRAM employing sense-amplifier redundancy," in *Proc. Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2007, pp. 328–329.

[25] I. J. Chang, J. J. Kim, S. P. Park, and K. Roy, "A 32 kb 10T sub-threshold SRAM array with bit-interleaving and differential read scheme in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 650–658, Feb. 2009.