Signal-Dependent Analog-to-Digital Conversion based on MINIMAX Sampling

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***Abstract*— This paper presents an architecture of signal-dependent analog-to-digital converter (ADC) based on MINIMAX sampling scheme that allows achieving high data compression rate and power reduction. The proposed architecture consists of a conventional synchronous ADC, a timer and a peak detector, and AD conversion is carried out only when input signal peaks are detected. To improve the accuracy of signal reconstruction, MINIMAX sampling is improved so that multiple points are captured for each peak, and its effectiveness is experimentally confirmed. In addition, power reduction, which is the primary advantage of the proposed signal-dependent ADC, is analytically discussed and then validated with circuit simulations.**

I. Introduction

Conventional synchronous analog-to-digital conversion and digital signal processing algorithms have been widely used in various applications and thoroughly studied. Traditionally, converters sample amplitude of analog signals consecutively at constant time intervals. In this approach, the sampling rate is determined by the maximal frequency in the signal spectrum. Therefore, for signals with low activity, the conventional sampling is not power efficient due to continuous sampling rate. For many applications with limited memory recourses and strict power consumption requirements, such as sensing applications, alternative signal-dependent sampling schemes have been explored [1][2][3][4][5]. A well-known signal-dependent sampling is level-crossing scheme [1]. In level crossing ADC, sampling occurs when the signal crosses predefined threshold levels. As a result, non-uniformly spaced samples, whose local sampling density depends on the signal local properties, are obtained. This scheme requires at least two constantly operating comparators and a reference voltage circuit, which contributes to power consumption [2]. Another signal-dependent sampling approach, MINIMAX sampling, which captures a sample every time an analog signal reaches its local maximum or minimum value, is proposed in [6]. The voltage amplitude of the sample is quantized and the time elapsed after the previous sample is measured by a local timer. MINIMAX sampling naturally adjusts sampling frequency depending on input signal frequency. In fact, [6] reported that MINIMAX sampling scheme provides relatively high data compression rate and high reconstruction precision compared to level-crossing scheme. However, no physical implementations have been presented. Use of non-uniform sampling provides various advantages for data acquisition, e.g. reduced number of samples (data compression), absence of aliasing, and etc. However, it often suffers from difficulty of accurate signal reconstruction due to its high computational complexity [7]. In this paper, we propose a power-efficient and signal-reconstruction-friendly implementation of MINIMAX ADC consisting of a peak detector, a timer and an amplitude quantization circuit. In this architecture, the reconstruction accuracy is improved by capturing multiple samples per peak, which reduces necessity for precise peak detection. Power consumption is minimized by sampling an analog signal at discreet time intervals and performing AD conversion only after detection of signal peak. In addition, the power reduction of the proposed implementation is analytically derived, and the derived relation is experimentally validated through 180nm circuit simulation.

The remainder of this paper is organized as follows. Section II presents the proposed architecture of MINIMAX ADC. Section III describes an improved MINIMAX sampling to enhance the accuracy of signal reconstruction and reduction of number of samples. Section IV analytically discusses the SNR (signal-to-noise ratio) and power dissipation. The analytical discussion on dependence of power dissipation on active ratio of analog input signal is experimentally confirmed and power reduction compared with conventional synchronous ADC is shown in Section V. Section VI concludes the discussion.

II. ADC Architecture

Fig.1. shows the architecture of the proposed ADC for MINIMAX sampling composed of a peak detector, a timer and an amplitude quantization circuit. The peak detector finds peaks of a given analog input signal V_{analog}, and gives triggers trig to analog signal quantization circuit and timer. The key circuit of MINIMAX ADC is the peak detector, which enables signal-dependent sampling. Precision of peak detection is one of the important points that characterize the overall performance of the MINIMAX ADC.

A possible implementation of peak detector is shown in the Fig.2. It consists of a comparator, two capacitors and two switches. These pairs work as sample-and-hold circuits and are used for storing previous and current amplitude values of input signal V_{analog} for comparison. In this configuration, when a peak occurs, the comparator generates a transition, which enables peak detection.

On the other hand, conventional synchronous ADC can be used for amplitude quantization. This ADC works only

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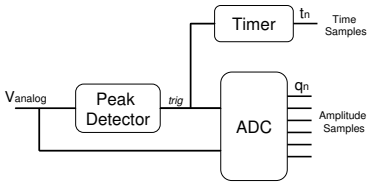

Fig. 1. Structure of MINIMAX ADC.

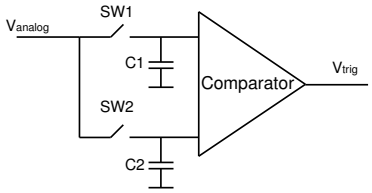

Fig. 2. Switched-capacitor peak detector.

when peaks are detected, and hence an implementation with less static power consumption is desirable. For that purpose Successive Approximation (SA) ADC [9] with clocked comparator [9][10] was selected. Additionally, the same implementation of the clocked comparator is used in the peak detector circuit.

III. MINIMAX SAMPLING

Fig.3. illustrates an example of 1-point MINIMAX sampling in which a sample is captured for each peak. Reference [6] reported that it is theoretically possible to reconstruct an analog signal from MINIMAX samples with relatively high precision if the exact timings of the peaks are known. One of the advantages of MINIMAX sampling is the ability to reconstruct an analog signal with reduced number of samples. Table I lists comparison of conventional and 1-point MINIMAX sampling scheme in processing an audio signal. Here, a short male speech signal was chosen, because it consists of active regions and pauses, which is the property that signal-dependent sampling scheme exploits.

MSE (Mean Squared Error) is defined as:

$$MSE = \frac{1}{n_s}\sum_{i=1}^{n_s}(s_i - \widehat{s_i})^2 \tag{1}$$

where s_i and $\widehat{s_i}$ are original and reconstructed signals at the i-th timing and n_s is number of samples. Note that after signal reconstruction, n_s is the same for all the sampling schemes.

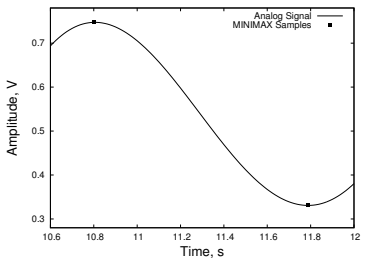

Fig. 3. 1-point MINIMAX sampling.

TABLE I
COMPARISON IN # SAMPLES AND MSE

Sampling	# of samples	MSE
Conventional (44kHz)	1.6M	-
MINIMAX (δ = 0.01)	160k	0.0021
MINIMAX (δ = 0.06)	80k	0.0054
Conventional (4kHz)	160k	0.0051

The sensitivity of peak detection depends on δ parameter, where δ is a parameter that defines how large the difference in voltage amplitude is necessary between successive timer timings for peak detection. It is associated with the comparator performance in the peak detector. At low δ values even small variations of analog signal can be detected, but it will increase the number of acquired samples.

1-point MINIMAX approach with $\delta = 0.01$ produces 160k samples, whereas conventional sampling scheme at 44 kHz sampling frequency produces 1.6M samples. After reconstructing this signal using cubic spline interpolation, the introduced MSE error is 0.0021, although the number of sample is reduced by 90%. The same number of samples could be achieved by down-sampling. However, the reconstruction of down-sampled signal would lead to a 2.4 times higher MSE error (0.0051). On the other hand, it would be possible to achieve similar MSE error (0.0054) by using MINIMAX approach with $\delta = 0.06$. In this case, the number of sample is reduced to 80k indeed. A certain amount of sampling error will be introduced if a discrete timer is used to measure the time between samples. By using timer, however, it becomes possible to use traditional signal processing algorithms because all samples are located on uniform grid.

Fig. 4 exemplifies the error introduced by a discrete timer after 1-point MINIMAX sampling in the case when one sample is captured for each peak. The vertical lines correspond to clock signal at which the timer increments its value and black dots (T1, T2, T3) are the actual peaks of the signal. If any peak occurs between clock edges, its time will be approximated to the current timer value T1*, T2*, T3*. This significantly affects SNR and introduces waveform distortion.

It is obvious that at low timer frequencies it will be difficult to detect the timings of peaks precisely. Use of higher timer frequency, in contrast, leads to more precise peak detection and higher SNR, but may increase the power consumption of the system. We, therefore, propose an alternative approach that samples multiple points around the peak instead of one for improving reconstruction accuracy by mitigating the uncertainty of the peak timings. In the proposed sampling scheme, named 3-point MINIMAX sampling scheme, three points, which are ones before/at/after the peak detection, are sampled using sample-and-hold circuits for each peak (Fig. 5).

Fig. 6 shows how MSE of the reconstructed signal depends on the ratio F, which is defined as:

$$F = \frac{f_t}{f_s} \tag{2}$$

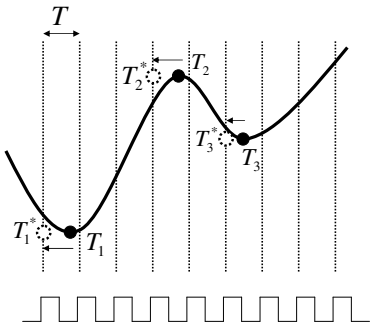

Fig. 4. Error introduced due to 1-point MINIMAX sampling.

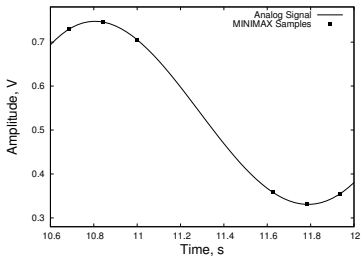

Fig. 5. 3-point MINIMAX sampling.

where f_t is the timer frequency that determines the minimum time interval between samples. f_s is analog signal frequency. Here, sine waveforms were given.

In this evaluation, for signal reconstruction, cubic spline interpolation was used [6]. Quantization error due to sampling is not included.The minimum F value for 3-point sampling scheme starts from 8, because with smaller F values the peak detection is not possible.

It can be seen that, for 1-point sampling, the MSE decreases until a certain point ($F = 10$) as the timer frequency increases. Beyond that point, the peaks can be relatively precisely detected. However, the MSE stays unchanged due to uncertainty in signal trace between samples. More sophisticated signal processing techniques might be able to reduce the MSE, but the reduction is inherently limited. As for 3-point sampling, the error is lower compared to 1-point case and it is relatively stable for all F values, which indicates that high timer frequency is not necessary. This contributes to power efficient implementation, because power dissipation associated with clocking can be suppressed. Furthermore, it mitigates the increase in the number of sampling points due to 3-point sampling.

IV. Performance Analysis

This section analytically investigates two key performance metrics of ADC, SNR and power dissipation.

A. SNR

Performance of ADC is determined by two factors introduced due to conversion quantization and reconstruction errors. Section III discussed the error introduced during signal reconstruction. This section discusses the quantization error.

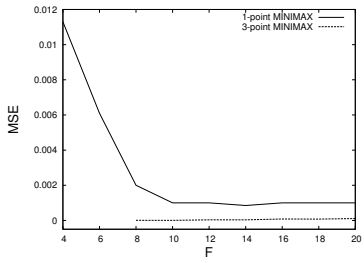

Fig. 6. MSE error dependence on ratio between sampling and signal frequencies.

SNR is often used to evaluate performance of a given ADC and quantify how much a signal has been distorted by quantization noise [8]. SNR is defined as:

$$SNR = 10log_{10}\frac{P_s}{P_{\delta a} + P_{\delta t}} \tag{3}$$

where P_s is the power of the signal, $P_{\delta a}$ is the power of the error due to amplitude quantization and $P_{\delta t}$ is the power of error introduced due quantization in time.

As discussed in Section II, the timings of peak detection are quantized by the timer, which introduces a certain error. For the proposed 3-point MINIMAX sampling a signal is sampled at a certain sampling frequency similar to synchronous sampling scheme, and therefore, $P_{\delta t}$ is the same as in synchronous approach and amplitudes of the peaks will be quantized at clock edge introducing $P_{\delta a}$. Therefore, the quantization noise of the proposed ADC is the same with traditional approach.

B. Power Consumption

In n-bit SA-ADC, comparison is repeated n times for one AD conversion. Then, power consumption of conventional synchronous SA-ADC, P_{conv}, is expressed by

$$P_{conv} = (E_{ADC} + E_{SAR}) \cdot f_t \cdot n \tag{4}$$

where E_{ADC} is the energy per one bit conversion in SA-ADC, E_{SAR} is the energy of Successive Approximation Register (SAR) and f_t is the sampling frequency. In the proposed MINIMAX ADC, the peak detector works at every timer timing. On the other hand, SA-ADC works only when peaks are detected. Therefore, the power dissipation of the proposed MINIMAX ADC, P_{prop}, is expressed by

$$\begin{aligned} P_{prop} &= E_{PD} \cdot 3 \cdot f_t + (E_{ADC} + E_{SAR}) \cdot 3 \cdot f_t \cdot n \cdot \alpha + \\ &+ E_t \cdot 3 \cdot f_t \end{aligned} \tag{5}$$

where E_{PD} is the energy of peak detector per timer cycle, E_t energy of the timer and α is the ratio of peak detection related to timer frequency. Here, $3 \cdot f_t$ comes from a fact that three samples have to be captured for each peak. At $\alpha = 0\%$ analog input signal is constant, while at $\alpha = 100\%$ the AD conversion is done at every timer period. Using these two expressions, we can estimate the power ratio of the proposed

ADC to the conventional ADC:

$$\begin{aligned}\frac{P_{prop}}{P_{conv}} &= \frac{E_{PD}\cdot 3\cdot f_t + (E_{ADC}+E_{SAR})\cdot 3\cdot f_t\cdot n\cdot\alpha}{(E_{ADC}+E_{SAR})\cdot 3\cdot f_t\cdot n} + \\ &+ \frac{E_t\cdot 3\cdot f_t}{(E_{ADC}+E_{SAR})\cdot f_t\cdot n} = \\ &= \frac{3\cdot E_{PD}}{(E_{ADC}+E_{SAR})\cdot n} + 3\cdot\alpha + \\ &+ \frac{3\cdot E_t}{(E_{ADC}+E_{SAR})\cdot n}\end{aligned} \quad (6)$$

From (6) it is possible to derrive the value of α at which the P_{prop} will start to be less that P_{conv}:

$$\begin{aligned}\alpha <= \frac{1}{3} - \frac{E_{PD}}{(E_{ADC}+E_{SAR})\cdot n} - \\ - \frac{E_t}{(E_{ADC}+E_{SAR})\cdot n}\end{aligned} \quad (7)$$

This expression means that as α becomes small and n becomes large, the advantage of the proposed ADC increases.

V. Simulation Results

This section validates the power reduction in Eq. (6) with circuit simulation. We implemented the proposed 3-point MINIMAX ADC in 180nm CMOS technology. The resolution of ADC is 8 bits and supply voltage is 1.8V. Comparator similar to [9] was adopted for the peak detector circuit and SA-ADC. 2 kHz sine signal with 20 kHz timer frequency was used in this evaluation. To emulate intermittent input signals, we changed the ratio of sine signal and DC signal. The power dissipation was estimated by circuit simulation. Since the proposed ADC is targeted for low power applications, it has been assumed that signal reconstruction will not be done by the same chip. Therefore, power overhead of a digital reconstruction filter is not discussed here.

Fig. 7 shows simulation results of MINIMAX ADC with a switched capacitor peak detector, and demonstrates that its power consumption depends on the activity of input signal. The power dissipation of the synchronous SA-ADC is also shown in Fig. 7. The power dissipation of the synchronous SA-ADC is roughly constant, because AD conversion is carried out continuously. When the ratio of active signal is high conventional synchronous ADC is power-efficient. However, when the ratio is lower than $\sim$20%, the proposed ADC attains lower power operation

Let us compare the simulation result with the analytical discussion of Eq. (6). It can be seen that, theoretically, the value of α cannot be more that $\sim$33% for MINIMAX ADC to be more power-efficient than conventional ADC. The energies of peak detector and timer are the key parameters that affect the efficiency. The tie-break point is estimated to be 28% by (6), and close to 20% from the simulation result. It means that the proposed architecture can attain lower power ADC for input signals whose peak ratio is lower than 20$\sim$28% Thus, the discussion in IV.B is validated. The higher values of α can be achieved by reducing energies of peak detector and timer.

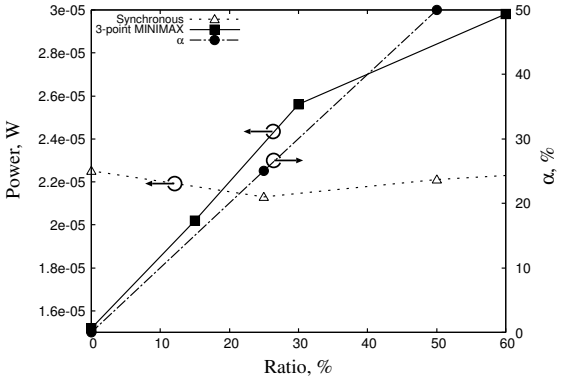

Fig. 7. Simulated power consumption.

VI. Conclusion

This paper demonstrated that 3-point MINIMAX sampling approach can be effective for processing signals with low or changing activity while keeping the reconstruction accuracy. This sampling naturally adjusts to input signal frequency and allows saving power dissipation during inactive periods of input. The structure of 3-point MINIMAX ADC was proposed with switched-capacitor peak detector circuit. The simulation results confirm the validity of theoretical power reduction.

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