Neutron Induced Single Event Multiple Transients With Voltage Scaling and Body Biasing

Ryo Harada†*, Yukio Mitsuyama†*, Masanori Hashimoto†*, and Takao Onoye†*

†Dept. Information Systems Engineering, Osaka University, JAPAN *JST, CREST

{harada.ryo, mituyama, hasimoto, onoye}@ist.osaka-u.ac.jp

Abstract— This paper presents measurement results of neutron induced SEMT (single event multiple transients). We devise an SEMT measurement circuit and evaluate the dependency of SEMT on supply and body voltages using test chips fabricated in a 65nm CMOS process. Measurement results show that transients can arise simultaneously at adjacent six inverters sharing the same well, and SEMT ratio to all the single event transients reaches 40% at 0.7V with reverse body biasing. We also investigate the correlation between the spatial spreading of SEMT and the distance between sensitive nodes in layout. Furthermore, referring to the occurrence rates of single event single transient (SEST) and single event single upset (SESU), we validate the measured results.

I. Introduction

Along with the scaling of semiconductor devices, single event multiple faults, which is a kind of soft error that two or more nodes are affected by one radiation particle, is becoming a serious problem [1], [2], [3], [4], [5]. Single event multiple faults is mainly classified into single event multiple(-bit) upsets (SEMU), which causes bit flips in two or more memory elements, and single event multiple transients (SEMT), which induces pulses in two or more combinational logic nodes.

To understand and avoid SEMU, SEMU characterization[1], [2], [3], SEMU mitigation techniques, such as error checking and correction, memory interleaving [1] and layout design through error-aware transistor positioning (LEAP) [6], has been intensively studied. However, no SEMT measurement results have been reported though a few evaluations based on device and circuit simulation are reported [4], [5].

Soft error mitigation techniques often exploit spatial redundancy such as triple modular redundancy and built-in soft error resilience [7], [8]. On the other hand, for instance, even when a circuit is duplicated, the duplicated cells may simultaneously receive pulses induced by SEMT due to their location proximity. Without the consideration of SEMT, the reliability of the spatially redundant circuits can be overestimated. To avoid unexpected reliability degradation, understanding the characteristic of SEMT and deriving a layout guideline for redundancy are crucially important. Moreover, voltage scaling and body biasing are becoming popular for power reduction, and low voltage yet highly reliable devices are demanded for medical applications, such as implantable devices. Therefore, the dependency of SEMT on supply and body voltages should be investigated.

In this work, we propose a measurement circuit for acquiring the spatial spreading of SEMT. Experimental results of neutron radiation tests using fabricated test chips show that six transients can arise simultaneously at 3x3 inverter matrix and decrease in supply voltage and reverse body biasing increases SEMT ratio to all the single event transients. We also show and investigate the occurrence number and spatially-distributed distance of SEMTs for each spatial SEMT pattern. We furthermore confirm that the measured SEMTs are sufficiently isolated from multiple SESTs (single event single transient) and multiple SESUs (single event single upset) in neutron radiation tests whereas the isolation is not sufficient in alpha-particle radiation tests.

The remainder of this paper is organized as follows. Section II explains requirements for measuring SEMT and introduces the proposed SEMT measurement circuit. Section III presents an implementation of the proposed circuit and shows experimental results of accelerated neutron radiation tests. Section IV discusses difference between neutron- and alpha-induced soft errors and verifies the reliability of the measured SEMT results. Finally, the conclusion is given in Section V.

II. SEMT measurement circuit

We first review the requirements for measuring characteristic of SEMT. We then introduce the proposed measurement circuit.

A. Requirements for SEMT measurement circuit

SEMT causes multiple transients in a combinational circuit. In order to distinguish all the transients, they must be delivered to different memory elements (or different channels of a measurement equipment) respectively. Otherwise, some transients diminish and become invisible. This means that logical and electrical masking must be eliminated in the measurement circuit, and hence parallel cell-chains, each of which is terminated with an individual memory element, are desirable for SEMT measurement.

Furthermore, to finely characterize SEMT spatial distribution, the distance between sensitive nodes included in different cell-chains should be small. From such a perspective, inverter-chains are desirable, since the footprint of inverter cells is small compared to other logic cells. By adjacently placing inverter cells that are included in different cell-chains, the spatial spreading of multiple transients is expected to be captured with high spatial resolution.

Another requirement is the isolation from multiple SESUs and SESTs. When the isolation is not enough, the measured SEMTs are no longer reliable. This isolation must be ensured by circuit organization and/or measurement setup.

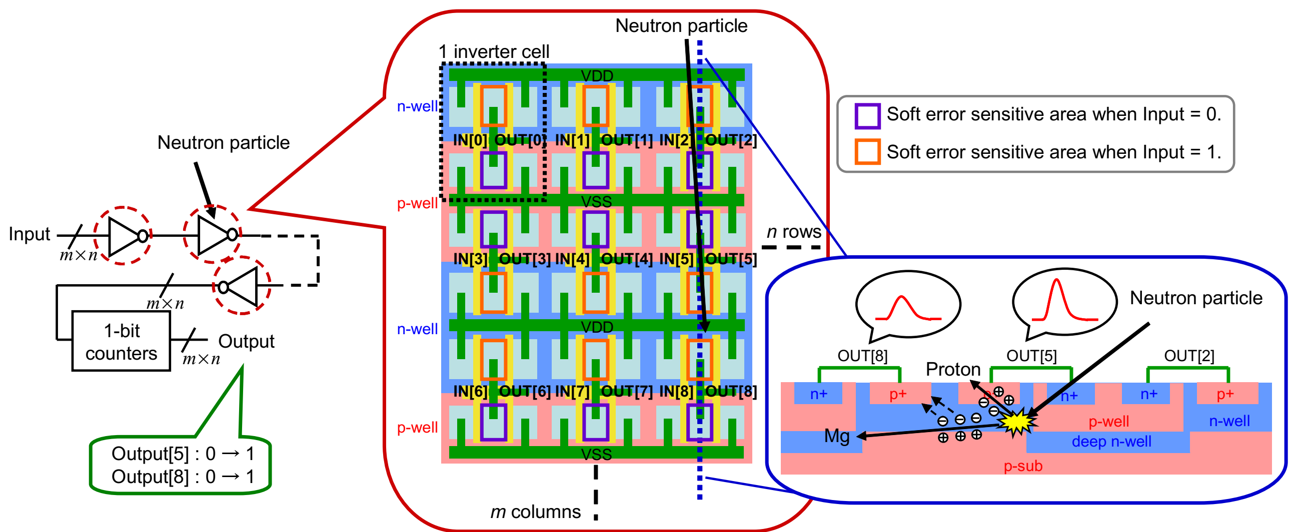

Fig. 1. Structure and operation of SEMT measurement circuit. At each stage, inverters are placed in $m \times n$ array. Each inverter-chain has a 1-bit counter at output, and SEMT across cells can be observed.

B. Proposed measurement circuit

According to the requirements described above, we devised a SEMT measurement circuit. Figure 1 illustrates the proposed measurement circuits composed of $m \times n$ inverter-chains, where each of them has the same stage length and a 1-bit counter at the output. For each stage, inverters are adjacently placed in a $m \times n$ array, and this array is serially connected on the whole.

In this circuit, we can measure SEMTs that spatially spread within $m \times n$ inverters at the maximum. A hit of neutron to silicon substrate could deliver charge to multiple sensitive nodes[1] across cell boundaries due to, for example, diffusion/drift and bipolar action [2]. In the example of Fig. 1, SEMT pulses arise at OUT[5] and OUT[8] and propagate into counters. By reading out the flips of counter values during the short time interval in which multiple SESTs will not happen, we can observe spatial distribution of SEMTs.

III. Experiment

This section first explains the experimental setup and then shows experimental results of accelerated neutron radiation test.

A. Experimental setup

To measure SEMT using the proposed circuit, a test chip was fabricated in a 65 nm CMOS process. The structure of test circuit is depicted in Fig. 2. 3×3 array using 2X-sized inverters in triple-well structure was selected as SEMT target circuit, and 15,896-stage chains were constructed for obtaining a large number of samples. Supply and body voltages of SEMT target circuit can be controlled separately. With double-back layout policy, power/ground lines are shared by inverters at successive columns as depicted in Fig. 1.

Neutron radiation test was performed at RCNP (Research Center for Nuclear Physics, Osaka University) using accelerated wide spectrum neutron beam [9], [10]. Figure 3 shows the test setup. The flux density of neutron beam was $2.41 \times 10^9 \text{cm}^{-2}\text{h}^{-1}$. In the experiment, the beam was irradiated to 30 test chips. The inputs of the inverter-chains were fixed to zero. The counter values were read out in every five seconds. In this implementation, we need to examine how much combinations of SESTs and/or SESUs are mistakenly included in the measured SEMT data. We will discuss it and show that the probability of multiple particle hits is low enough compared to that of SEMTs in Section IV.

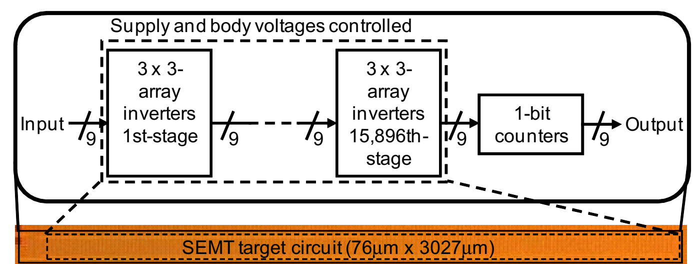

Fig. 2. Test chip fabricated in 65 nm process. SEMT target circuit is 15,896-stage 3×3-array inverter-chains.

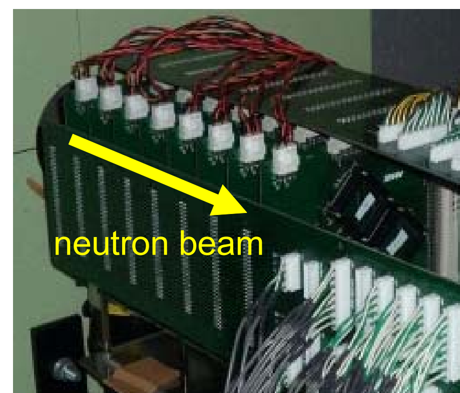

Fig. 3. Photograph of test environment. 30 test chips are installed on 8 DUT boards in total which are placed in series in front of beam aperture.

[1]Soft error sensitive area is NMOS drain area when its inverter input is 0 and PMOS drain area when its inverter input is 1.

TABLE I
NUMBER OF SESTS AND SEMTS OBSERVED IN NEUTRON RADIATION TEST AND SEMT RATIO.

Supply voltage [V]	1.2			0.7		
Body bias	ZBB	FBB	RBB	ZBB	FBB	RBB
Measurement time [h]	1.48	1.96	1.65	1.67	1.01	0.81
# of total transients	122	0	169	127	0	50
# of SESTs [/h]	72.9	0	80.5	50.9	0	37.2
# of SEMTs [/h]	9.46	0	21.8	25.1	0	24.8
SEMT ratio [%]	11.5	-	21.3	33.1	-	40.0

SEST: a flip at one 1-bit counter, SEMT: flips at two or more 1-bit counters.

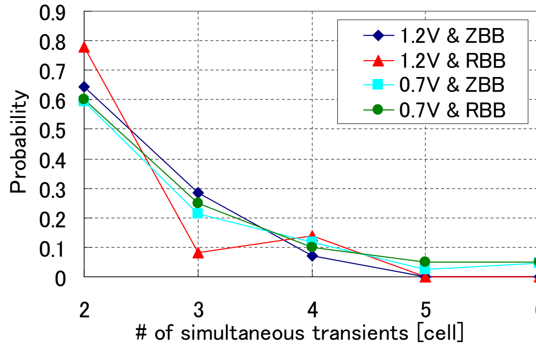

Fig. 4. Probability distribution of number of simultaneous transients, where for each curve the sum of probability is normalized to 1.

B. Results

Table I lists the measured results of experiments at two supply voltages, which are 1.2 V and 0.7 V, with three body-biasing configurations, zero body biasing (ZBB), 0.6 V forward body biasing (FBB), and 1.3 V reverse body biasing (RBB). While in FBB, there was neither SEST nor SEMT in this experiment, in RBB compared to ZBB, the numbers of SESTs and SEMTs increase at 1.2 V and they decrease at 0.7 V. The ratio of SEMTs to the total transients increases as the supply voltage decreases and the body is biased in reverse direction.

Figure 4 shows the probability distribution of the number of simultaneous transients, where for each curve the sum of probability is normalized to 1. We observed six transients at the maximum for a single neutron hit. Five and six transients occurred only in the operation of 0.7 V supply voltage. The occurrence probability decreases as the number of simultaneous transients increases, and this tendency is less dependent on supply and body voltages.

Figure 5 illustrates the layout of sensitive nodes in the 3x3 array and possible horizontal and vertical patterns of two-transient SEMTs. Figure 6 shows the number of occurrence for each SEMT spatial pattern. The horizontal axis is the farthest distance between related sensitive areas in the corresponding SEMT pattern. Here, any symmetric patterns are regarded as a single pattern. We did not observe SEMT across three cells in the vertical direction. This means that SEMTs arise within a single well and no SEMTs across well boundary happen, which is consistent with the SEMU observations [3]. Looking at two-transient cases, the numbers of occurrence are 38 and 35 in horizontal and vertical cases respectively, and they are almost the same, although the distance between sensitive nodes is twice larger in horizontal case (0.6μm) than in vertical case (0.33μm). On the other hand, in 3x3 array, the number of possible physical patterns in horizontal case is six whereas it is three in vertical case when considering SEMTs arise only within the same well. The distance between sensitive nodes is canceled by the number of possible patterns, and then the similar numbers of occurrence were observed. In this experiment, we observed six-transient SEMTs, which are the largest measurable SEMTs in the fabricated test chip, and hence it might be possible that SEMTs were more widely spread. Larger array of inverter-chains would be necessary for further investigation.

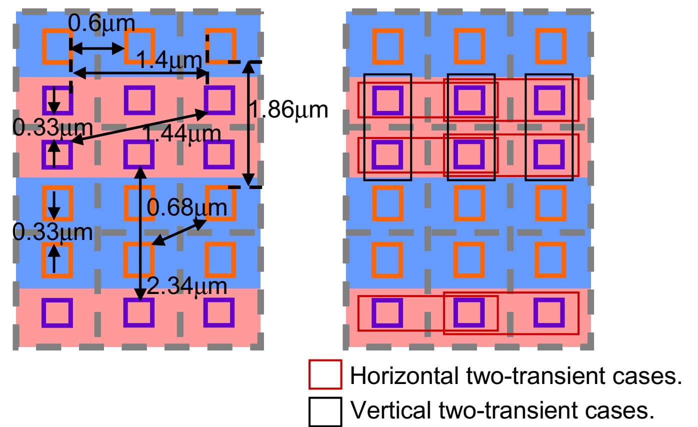

Fig. 5. The distance between sensitive nodes and possible physical patterns of two-transients cases.

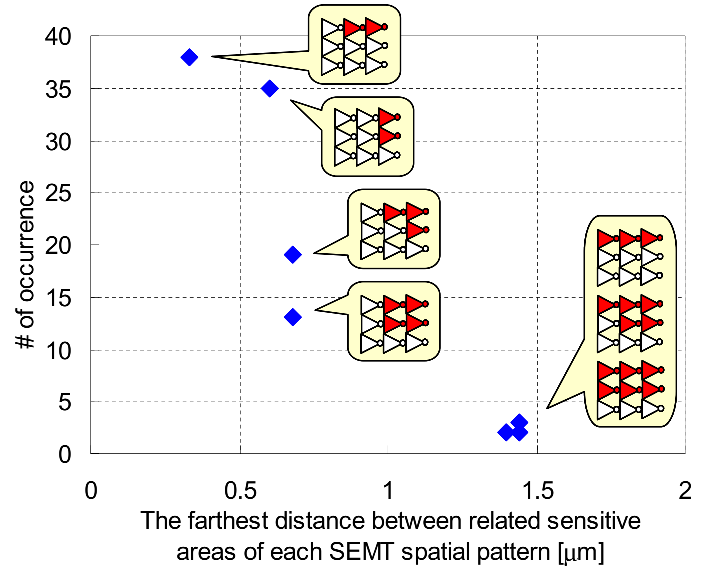

Fig. 6. The farthest distance between two sensitive areas versus the number of occurrence for each SEMT spatial pattern.

IV. DISCUSSION ON SEMT ISOLATION FROM MULTIPLE SESTS AND SESUS

As described in Section III-*A*, by the measurement circuit implemented on the test chip, an true-SEMT cannot be distinguished from pseudo-SEMT, which is multiple SESTs, multiple SESUs and a combination of SEST and SESU. We investigate the misrecognition probability of SEMT.

TABLE IV
RATIO OF ESTIMATED OCCURRENCE PROBABILITIES OF TRUE-SEMT AND PSEUDO-SEMTS TO TOTAL OCCURRENCE PROBABILITY OF ALL SEMTS IN BOTH NEUTRON AND ALPHA-PARTICLE TESTS. EACH OCCURRENCE PROBABILITY IS CALCULATED BY USING THE MAXIMUM λ AMONG SIX SUPPLY AND BODY BIAS CONDITIONS.

	Neutron				Alpha			
	Pseudo-SEMT			True-SEMT	Pseudo-SEMT			True-SEMT
	2 SESTs	2 SESUs	1 SEST & 1 SESU		2 SESTs	2 SESUs	1 SEST & 1 SESU	
Probability ratio[%]	0.72	0.00	0.00	99.28	6.80	22.09	24.57	46.55

TABLE II
CROSS SECTIONS OF SESTS AND SESUS OBSERVED IN NEUTRON AND ALPHA RADIATION TESTS.

	Neutron	Alpha
Measurement time [h]	8.38	5.47
SEST cross section [μm^2/cell]	4.03×10^{-7}	1.28×10^{-6}
SESU cross section [μm^2/bit]	6.63×10^{-6}	1.28×10^{-2}

TABLE III
ESTIMATED NUMBER OF SESTS AND SESUS PER SECOND IN A 1-BIT COUNTER.

	Neutron	Alpha
#SESTs [/(s·counter)]	2.49×10^{-4}	2.66×10^{-5}
#SESUs [/(s·counter)]	6.63×10^{-8}	4.81×10^{-4}

We first examine the cross-sections of SESU and SEST. In the same test chip, a shift register consisting of 100 D-FFs was implemented. We measured SESUs occurred in these D-FFs at the same time as measuring SESTs and SEMTs in the neutron radiation test. We also measured SESTs, SEMTs, and SESUs in alpha radiation test for clarifying the difference between neutron induced soft errors and alpha-particle induced soft errors. The alpha particle tests were performed using an Americium-241 foil whose flux is 9×10^9cm^{-2}h^{-1}. The radiation source was put immediately above on a test chip [10].

Table II shows the experimental results of both the neutron and alpha radiation tests. Compared to the neutron results, alpha-induced SESU has much larger cross section than SEST. We here associate the cross section difference with the energy spectrum difference between neutron and alpha particles as one of possible reasons, though other factors in terms of charge generation and collection are different as well. In the measurement circuit, SESU critical charge for flipping a D-FF is much smaller than SEST critical charge for flipping a 1-bit counter at the end, because the mismatch of rise and fall delay and electrical masking through 15,896 inverters at maximum reduce the SEST pulse width before arriving at the 1-bit counter. Besides, the main peak energy of Americium-241 is 5.49 MeV, while the energy of neutron beam used for the experiments distributes over 100 MeV [9]. If the mean of the charge induced by alpha particles is between the critical charge of SESU and that of SEST, SEST/SESU ratio in alpha radiation test becomes low. On the other hand, the wide spectrum neutron beam includes many particles which can induce the charge that is larger than the SESU and SEST critical charges. This is one of possible reasons that explain lower SEST/SESU ratio in alpha particle tests.

Next, the obtained SEMT results, which might include pseudo-SEMTs, are verified. First, the number of SESTs and SESUs observed in a 1-bit counter of SEMT measurement circuit are estimated from the total number of SESTs observed in the SEMT measurement circuit and the number of SESUs observed in the 100 D-FFs. Table III lists the estimated number of SESTs and SESUs per second in a 1-bit counter. From now, two-transient SEMTs are validated using the estimated number of SESTs and SESUs. The occurrence probabilities of SEST and SESU that N events are observed in a unit time follows the Poisson distribution and is expressed by

$$P(N) = \frac{e^{-\lambda}\lambda^N}{N!}, \quad (1)$$

where λ is the expected number of occurrences in the time interval. Similarly, the occurrence probabilities of all types of SEMTs that flip two of any nine counters during the time interval of counter read, which consist of pseudo-SEMTs and true-SEMTs, are estimated by Table I and (1). Using these occurrence probabilities, we calculate the occurrence probabilities of pseudo-SEMTs and true-SEMT. Table IV lists the ratio of calculated occurrence probabilities of pseudo-SEMTs and true-SEMT to the total occurrence probability of all SEMTs. In the case of two-transient SEMT, the ratio of true-SEMT occurrence probability in alpha particle tests is estimated to be 46.6% because of higher SESU event rate, which means that true-SEMTs are overwhelmed by pseudo-SEMTs. On the other hand, we confirm that the SEMT results in neutron particle tests were sufficiently isolated since the ratio in neutron particle tests is 99.3%.

V. CONCLUSION

In this paper, we proposed an SEMT measurement circuit and presented the measurement result of neutron-induced SEMTs in 65 nm test chips. The measurement result showed that SEMT ratio increases as decreasing the supply voltage and biasing the body in reverse direction. On the other hand, neither SEST nor SEMT occurred in forward body biasing. We observed that SEMT can induce six transients in adjacent inverter cells and the occurrence probability of SEMT decreases according to increase in the number of simultaneous transients. We also showed that the occurrence tendency of spatial patterns of SEMTs and no SEMT observation across three cells in the vertical direction due to well boundary. Furthermore, we validated the SEMT measurement results of the neutron radiation test on the basis of the occurrence probabilities of SEST and SESU. As future works, we will investigate the reason why soft error did not occur in

FBB case and we will characterize SEMTs using larger array structure.

Acknowledgments

The authors would like to acknowledge technical advices from Dr. Eishi Ibe of Hitachi. The authors also would like to thank VDEC, the University of Tokyo in collaboration with STARC, e-Shuttle, Inc., and Fujitsu Ltd. for their support in getting the chip fabricated. The authors appreciate the support of Professor Kichiji Hatanaka and Assistant Professor Keiji Takahisa of Osaka University for the neutron radiation test at RCNP. This work was partly supported by NEDO.

REFERENCES

[1] N. Seifert, P. Slankard, M. Kirsch, B. Narasimham, V. Zia, C. Brookreson, A. Vo, and S. Mitra, "Radiation-induced soft error rates of advanced CMOS bulk devices," in *Proc. IRPS*, pp. 217–225, 2006.

[2] E. Ibe, S. Chung, S. Wen, H. Yamaguchi, Y. Yahagi, H. Kameyama, S. Yamamoto, and T. Akioka, "Spreading diversity in multi-cell neutron-induced upsets with device scaling," in *Proc. CICC*, pp. 437–444, 2007.

[3] Y. Yahagi, H. Yamaguchi, E. Ibe, H. Kameyama, M. Sato, T. Akioka, and S. Yamamoto, "A novel feature of neutron-induced multi-cell upsets in 130 and 180 nm SRAMs," *IEEE Transactions on Nuclear Science*, vol. 54, no. 4, pp. 1030–1036, 2007.

[4] D. Rossi, M. Omana, F. Toma, and C. Metra, "Multiple transient faults in logic: An issue for next generation ICs?" in *Proc. DFT*, pp. 352–360, 2005.

[5] C. Rusu, A. Bougerol, L. Anghel, C. Weulerse, N. Buard, S. Benhammadi, N. Renaud, G. Hubert, F. Wrobel, T. Carriere *et al.*, "Multiple event transient induced by nuclear reactions in CMOS logic cells," in *Proc. IOLTS*, pp. 137–145, 2007.

[6] H. Kelin, L. Klas, B. Mounaim, R. Prasanthi, I. Linscott, U. Inan, and S. Mitra, "LEAP: Layout Design through Error-Aware Transistor Positioning for soft-error resilient sequential cell design," in *Proc. IRPS*, pp. 203–212, 2010.

[7] S. Mitra, M. Zhang, S. Waqas, N. Seifert, B. Gill, and K. Kim, "Combinational logic soft error correction," in *Proc. ITC*, vol. 2, p. 824, 2006.

[8] J. Furuta, C. Hamanaka, K. Kobayashi, and H. Onodera, "A 65nm Bistable Cross-coupled Dual Modular Redundancy Flip-Flop capable of protecting soft errors on the C-element," in *Proc. VLSIC*, pp. 123–124, 2010.

[9] Y. Tosaka, H. Ehara, M. Igeta, T. Uemura, H. Oka, N. Matsuoka, and K. Hatanaka, "Comprehensive study of soft errors in advanced CMOS circuits with 90/130 nm technology," in *Proc. IEDM*, pp. 941–944, 2005.

[10] JEDEC standard JESD89, "Measurement and reporting of alpha rarticles and terrestrial cosmic ray-induced soft errors in semiconductor devices," 2001.