Evaluation of Power Gating Structures Focusing on Power Supply Noise with Measurement and Simulation

Yasumichi Takai, Masanori Hashimoto, Takao Onoye
Dept. Information Systems Engineering, Osaka University, Suita 565-0871, JAPAN
takai.yasumichi@ist.osaka-u.ac.jp, hasimoto@ist.osaka-u.ac.jp

***Abstract*—This paper investigates the impact of power gating structure on power supply noise using 65nm test chip measurement and simulation. We focus on the body connection of power-gated circuits, and examine the contribution of a power-gated circuit as a decoupling capacitance during the sleep mode. Experimental results show that the well junction capacitance of the power-gated circuit with body-tied structure helps reduce power supply noise while a sharp drop cannot be mitigated due to its large RC time constant.**

***Index Terms*—on-chip power supply noise, power gating, well structure**

I. Introduction

As increasing demands for low power LSIs, power gating technique is widely adopted for reducing leakage current of inactive circuits, and is intensively studied for reducing wake-up time and maximizing leakage reduction. On the other hand, shorter wake-up time from sleep (power-gated) mode fundamentally involves larger rush current to recharge gate and PN-junction capacitances in the power-gated circuit, which results in a large voltage droop in the power supply network. To mitigate the droop induced by the rush current, a smart wake-up procedure [1], [2] and a sophisticated power gating structure [3], [4] are studied.

From a viewpoint of supply noise suppression, power gating of inactive circuits means the reduction in intrinsic decoupling capacitance, because the gate and PN-junction capacitances are disconnected from the power distribution network. Besides, PN-junction capacitance depends on the well structure. In [5], power supply noises of circuits with twin-well and triple-well structures are measured and compared. Compared to the twin-well structure, the ground bounce in the triple-well structure is larger due to the absence of the P-substrate resistive network, and the power voltage droop is smaller thanks to the increase in PN-junction capacitance.

This paper focuses on the well structure and the body connection, and presents two measurement results of the power supply noise in power-gated circuits. The first measurement result shows how the power-gated circuit behaves as an intrinsic decoupling capacitance. The other is the power supply noise due to the rush current during the wake-up. We also show the measurement results are correlated with simulation results.

The remaining of this paper is organized as follows. Section II explains power gating structures and their influence on power supply noise. Section III shows test chip structure and explains simulation model. Section IV presents measurement and simulation results of power supply noise focusing on how the power-gated circuit behaves as a decoupling capacitance. Section V shows results of measured and simulated noises due to rush current and Section VI concludes this discussion.

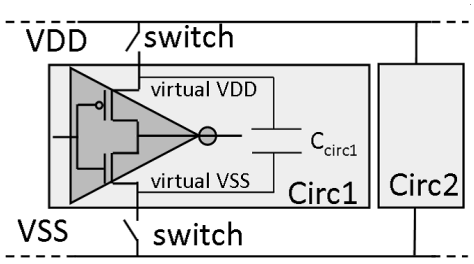

Fig. 1. Basic power gating structure circuit

II. Power Gating Structure

A. Power Gating Structure and Rush Current

Figure 1 shows a schematic of a basic power gating structure. VDD and VSS are power supply and ground lines. Circ1 is the circuit whose power and ground can be gated with switches, whereas Circ2 is always connected to the power and ground lines. By gating Circ1 while it is inactive, its leakage current can be reduced. In the figure, both power and ground are gated, whereas either of the two is often gated in practical implementations.

We next explain rush current that flows when the switch is turned on. C_{circ1} represents gate capacitance of MOS transistors and PN-junction capacitance. During the sleep mode, the voltage of virtual VDD/VSS gradually decreases/increases. This means that C_{circ1} is discharged. On the other hand, when the switches of Circ1 are turned on, C_{circ1} starts to be charged. A large current flows immediately after the switch is turned on because the voltage difference between VDD/VSS and virtual VDD/VSS is large. This temporal large current is called rush current, and causes large IR drop and Ldi/dt noise.

The magnitude of the rush current depends on the amount of C_{circ1}, and the effective resistance of the switch. As the resistance becomes smaller, the wake-up time becomes shorter, but larger rush current flows, that is, larger noise arises. Another important factor is that C_{circ1} depends on the well structure and the body connection. We in this paper focuses on well structures and the body connection, and evaluate them

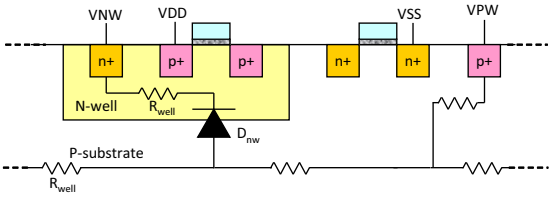

Fig. 2. Cross-section and parasitic elements in twin-well structure.

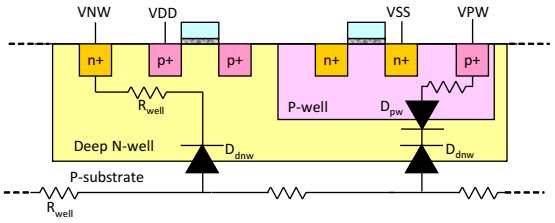

Fig. 3. Cross-section and parasitic elements in triple-well structure.

in terms of an intrinsic decoupling capacitance and the voltage droop due to the rush current.

B. Twin-well and Triple-well Structures and PN-Junction Capacitance

Figure 2 shows a cross-section and parasitic elements in twin-well structure. VDD and VSS are power and ground lines, and VNW and VPW represent backgate voltage lines connected to N-well and P-substrate respectively. PN-junction between N-well and P-substrate is modeled as a diode (D_{nw}). This diode is reversely biased, and hence it behaves as PN-junction capacitance.The substrate is often modeled as a resistive network.

A triple-well structure is depicted in Fig. 3. VNW and VPW are connected to deep N-well and P-well respectively. In the case of the triple-well structure, there are two types of well junction capacitance, which originate from the diode between P-well and deep N-well (D_{pw}), and the diode between deep N-well and P-substrate (D_{dnw}).

When we implement power gating, there are two options; bodies (VNW and VPW[1]) are also gated or not. We hereafter call the option that only VDD and VSS are gated "body-tied", and the option that VNW and VPW as well as VDD and VSS are gated "body-gated". In the body-tied structure, it is expected that the well capacitance contributes to noise suppression as a decoupling capacitance even while the circuit is power-gated. In addition, the well capacitance is not discharged during power gating, which results in less rush current.

III. Test Chip Structure and Simulation Setup

A. Test Chip Structure

1) Overview: A test chip for evaluating the noises in each power gating structure was fabricated in a 65nm CMOS process. Figure 4 shows a micrograph of the test chip. The measurement circuit on the test chip consists of four test elementary groups (TEGs) and shift registers. The shift registers store configurations of the TEGs. The counter used in the waveform sampling macro[6] is also included in the shift resistors. This macro called "gated oscillator" is a ring-oscillator-based circuit but it captures dynamic noise waveforms thanks to intermittent operation at the timing of interest.

[1]In the case of twin-well structure, VPW can not be gated, and only VNW is gated.

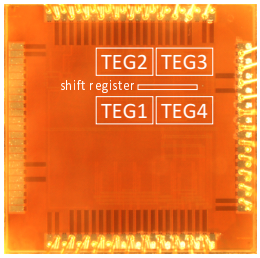

Fig. 4. Chip micrograph (2.1mm × 2.1mm).

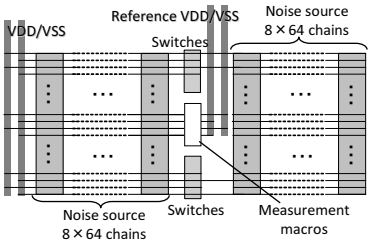

Fig. 5. Basic TEG structure with noise sources and measurement macros.

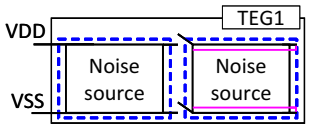

Fig. 6. TEG1:triple-well to triple-well, body-gated.

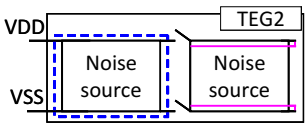

Fig. 7. TEG2:triple-well to twin-well, body-gated.

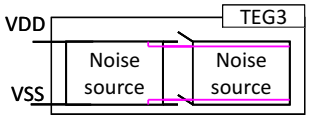

Fig. 8. TEG3:twin-well to twin-well, body-tied.

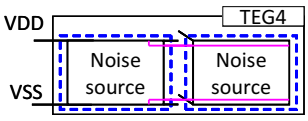

Fig. 9. TEG4:triple-well to triple-well, body-tied.

2) TEG structure: Each TEG consists of noise sources, the measurement macros and control logic. Figure 5 depicts the basic TEG structure including the measurement macros and switches for power gating. A noise source is composed of 512 12-stage NAND chains. Two noise sources are placed in a TEG, and these are connected through transmission gates (switches). A noise source occupies 115μm×150μm area and the area of a TEG is 420μm×180μm. The right noise source, which can be gated, is named "gated_NS", and the other, which is always connected to power and ground lines, is called "powered_NS". To observe VDD, VSS and VDD–VSS separately, three measurement macros are integrated. The first macro is connected to VDD of the DUT and a dedicated stable reference VSS, the second one dedicated stable reference VDD and VSS of DUT, and the last one to VDD and VSS of DUT. In the following measurements, VDD and VSS are set to be 1.2V and 0.0V.

Figures 6–9 illustrate four TEGs (TEG1–TEG4) on the test chip. These TEGs are different in terms of well structure (twin- and triple-well for powered_NS and gated_NS) and power

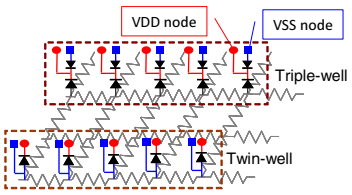

Fig. 10. Well modeling for simulation.

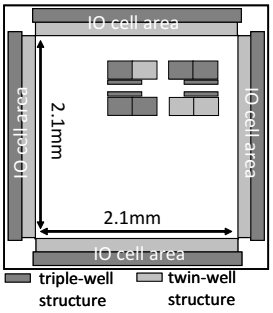

Fig. 11. Well structures assumed in simulation.

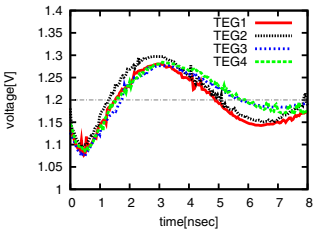

Fig. 12. Measured VDD–VSS noise waveforms when the switch for power gating is OFF.

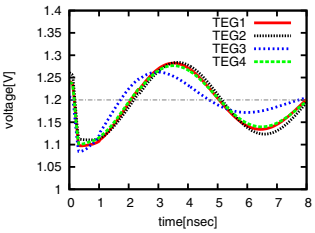

Fig. 13. Simulated VDD–VSS noise waveforms when the switch for power gating is OFF.

gating structure (body-tied and body-gated). With these four TEGs, we carry out two evaluations of power supply noise. The first evaluation aims to examine whether the well capacitance inside the power-gated circuits can be used for noise suppression as a decoupling capacitance. The other evaluates the power supply noise due to rush current that flows when the switch is turned on. In the body-tied structures (TEG 3 and 4), the wells under the gated_NS are always connected to VDD or VSS. This means that the well capacitance under the gated_NS is expected to behave as a decoupling capacitance and help reduce power supply noise. In addition, the well capacitance is not discharged even while the circuit is gated, which results in smaller rush current. Thus, smaller power supply noises are expected in the body-tied structures (TEG 3 and 4) compared to the body-gated structures (TEG 1 and 2).

B. Simulation modeling of substrate and well diode capacitance

We simulate power supply and ground noises with a circuit simulator [7]. The simulated circuit model includes package and bonding wires, on-chip power and ground networks, noise sources, P-substrate resistive mesh and well junction diodes (Figure 10) associated with four TEGs and peripheral IO cells. Figure 11 shows the layout outline of the modeled N-well and deep N-well on the chip. When simulating a TEG, each noise source in the TEG is spatially divided into 8×64 regions, and well diodes in the divided regions are connected with resistive mesh of P-substrate. In the other TEGs and IO cells, sparser mesh modeling is carried out, and then all the meshes are connected with P-substrate resistances for a chip-level substrate and well model. Then, the network of on-chip wire resistance, which is connected to an ideal voltage source through package inductances, is attached to the chip-level substrate and well models. N-well, deep N-well and P-well diode models and substrate resistivity are given from a foundry.

IV. Performance of Power-Gated Circuits as Decoupling Capacitance

A. Evaluation Setup

In this section, we measure power supply noises to evaluate the performance of the power-gated circuit (gated_NS) as a decoupling capacitance. In this measurement, all the chains in powered_NS are active (switching), while all the chains in gated_NS are inactive (stable). A 50MHz clock signal is given to powered_NS, and the power supply noise is measured. The transmission gates for power gating are on or off, and the difference of the power supply noise is evaluated.

B. Well capacitance of body-gated circuits

Figure 12 shows measured VDD–VSS noise waveforms. In these VDD–VSS waveforms, the noises of the body-tied structure (TEGs 3 and 4) are smaller than those of the body-gated structures (TEGs 1 and 2) after 6 nano seconds. This means that the well capacitance under powered_NS contributes to noise suppression.

On the other hand, only little difference in the peak voltage drops (0.5 ns) between body-tied and body-gated structures is observed. This means that the well capacitance under powered_NS cannot respond to a sharp current variation. A larger RC time constant of the well capacitance deteriorates the performance as a decoupling capacitance. These observations suggest that the wells should not be gated from a viewpoint of decoupling capacitance, as we expected.

Figure 13 shows simulation results of the power supply noises under the same conditions of the above measurement. The first peaks of the voltage drop are close to those of the measured waveforms, and less dependent on the body-tied and body-gated structures, which is consistent with the measurement results. Also, the noise difference of TEG 3 after 6 nano seconds was reproduced, which means the well capacitance under gated_NS works as a decoupling capacitance with a larger time constant.

C. Resistance of power gating switch

We next compare VDD–VSS noise waveforms in cases that the power switch is on and off. Figure 14 shows the measured noise waveforms of TEG 1. Figure 15 also plots the simulated waveforms of TEG 1. The waveform labeled “short” in Fig. 15 was obtained supposing that the resistance of the switch is zero.

The supply voltage at the peak drop reaches 1.08V independent of the switch status (on and off) in Fig. 14. This tendency is also observed in the simulation. This is because the resistance of the power switch is not ignorable and it degrades

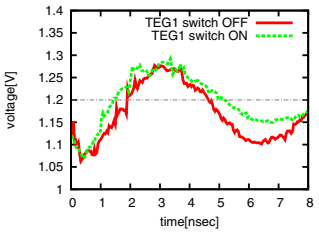

Fig. 14. Measurement VDD–VSS noise results of TEG1

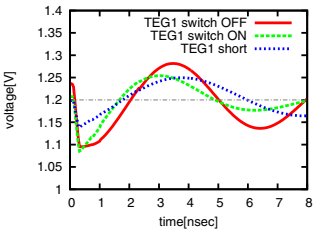

Fig. 15. Simulation VDD–VSS noise results of TEG1

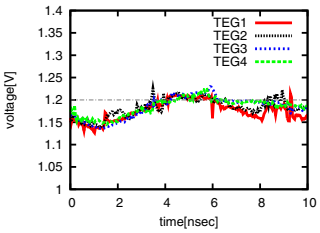

Fig. 16. Measured VDD–VSS noise waveforms when the switch for power gating is repeatedly turned on and off.

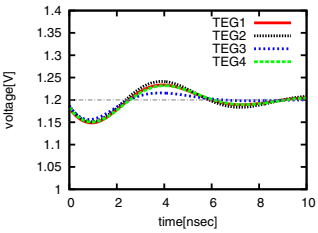

Fig. 17. Simulated VDD–VSS noise waveforms when the switch for power gating is repeatedly turned on and off.

the response of the capacitance in gated_NS to a sharp noise. This explanation is supported by the waveform of "short". When the resistance of the power switch is zero, the peak voltage drop is reduced. Thus, the response of the intrinsic capacitance in the power-gated circuits is worse than that of non-gated circuits.

On the other hand, the capacitance in the gated circuits helps reduce the noise after 6 nano seconds. This behaviour is also found in the simulation. In addition, the power gating affects the LC resonating frequency, and this variation is reproduced in the simulation.

V. Power Supply Noise due to Rush Current

A. Evaluation Setup

This section discusses noise waveforms due to rush current with measurement and simulation. The switch for power gating is repeatedly turned on and off in every 50 nano seconds (10MHz). Due to the limitation of the noise measurement macro[6], a slower operation is difficult. Since the power gating period of 50 nano seconds is not long enough to discharge the capacitance in gated_NS, we gave a pulse to make gated_NS run during the period of power gating and discharged the capacitance. The aim of this operation is to produce a pseudo discharge in longer gating time, and a certain amount of charge stored in gated_NS is consumed. We expect the VDD–VSS noise of body-tied structures (TEGs 3 and 4) is smaller than that of body-gated structures (TEGs 1 and 2) because the well capacitance in gated_NS is not discharged in body-tied structures.

B. Measurement and simulation results

Figures 16 and 17 show measurement and simulation results. These results indicate that there is little difference among TEGs, which is not consistent with the above expectation. This is because the amount of charge discharged in the pseudo operation is roughly independent of TEGs, though it should be different TEG by TEG in actual operations. Therefore, the power supply noise due to the rush current became similar. We need a more sophisticated structure and measurement circuit to capture the noise due to rush current.

VI. Conclusion

We discussed power supply noises in power-gated circuits with body-tied and body-gated structures. We evaluated the noise with measurement results of a 65nm test chip and corresponding simulation results. During the sleep mode, the power-gated circuit with the body-gated structure does not contribute to noise suppression as a decoupling capacitance, whereas the well junction capacitance in the power-gated circuit with the body-tied structure helps reduce power supply noise. A slow voltage fluctuation is well suppressed, though the well junction capacitance cannot mitigate a sharp voltage drop because its RC time constant is relatively large. Besides, voltage fluctuation due to rush current is expected to be smaller in the body-tied structure than in the body-gated structure, because the well junction capacitance is not discharged during the sleep mode. However, this expectation was not well confirmed in the test chip because of the measurement limitation of the test chip. One of future works includes the experimental validation of this expectation.

Acknowledgment

This work was partly supported by NEDO.

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