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Gate Delay Estimation in STA under Dynamic Power Supply Noise*

Takaaki OKUMURA[†a)], ***Member***, **Fumihiro MINAMI**[†], **Kenji SHIMAZAKI**[†], **Kimihiko KUWADA**[†], ***Nonmembers***, ***and*** **Masanori HASHIMOTO**[††], ***Member***

SUMMARY This paper presents a gate delay estimation method that takes into account dynamic power supply noise. We review STA based on static IR-drop analysis and a conventional method for dynamic noise waveform, and reveal their limitations and problems that originate from circuit structures and higher delay sensitivity to voltage in advanced technologies. We then propose a gate delay computation that overcomes the problems with iterative computations and consideration of input voltage drop. Evaluation results with various circuits and noise injection timings show that the proposed method estimates path delay fluctuation well within 1% error on average.

key words: *power supply noise, gate delay, timing analysis*

1. Introduction

Recently, Power/Ground voltage level fluctuation (PG noise) is becoming a primary concern in designing LSI products with the progress of technology scaling [1]. Current density in a chip has been increasing due to increase in operating frequency and power consumption in spite of decrease in supply voltage. This tendency makes circuit timing more susceptible to supply noise, and hence timing verification taking PG noise into account is essential for successful chip design.

Conventionally, the timing degradation due to PG noise is often estimated by annotating voltage drops at each instance. The voltage drops are obtained by static IR-drop analysis, which performs DC analysis using current consumption averaged within a cycle time. There are some reports that timing estimates based on the average voltage are well correlated with measurements [2], [3]. On the other hand, power supply noise is dynamic in nature. It has not been clearly demonstrated what the limitation of timing analysis based on static IR-drop analysis is, and under what conditions it becomes inappropriate.

With technology scaling and voltage lowering, the over-drive voltage (V_{dd}–V_{th}) is decreasing, which means gate delay becomes more sensitive to power supply voltage. Figure 1 depicts delay sensitivities of a 10-stage inverter chain to supply voltage in 180 nm and 45 nm technologies. The horizontal and vertical axes are static voltage drop (ΔV) and ratio of path delay change to the path delay at an ideal supply voltage ($\Delta D_{path}/D_{path}$), respectively. The sensitivity at 45 nm is five times higher than at 180 nm when ΔV=0.2 (V), and it has a strong non-linearity. Unfortunately, PG noise level is not scaling down and is predicted to be nearly constant despite lowering power supply voltage [4]. Thus, first-order approximation using Taylor expansion and static IR drop analysis will be more difficult to accurately capture the effect of noise on timing.

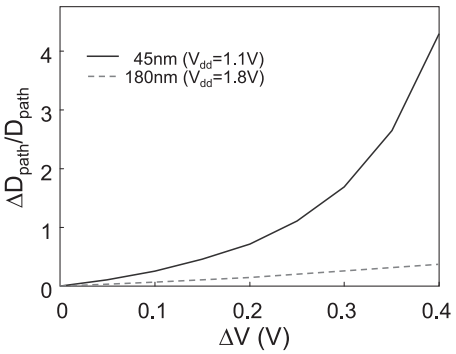

Fig. 1 Comparison of delay sensitivity to voltage between 180 nm and 45 nm.

Decoupling capacitance insertion is a well-known and effective way to suppress power supply noise [5]. Conventionally, it is inserted to satisfy constraints in noise voltage, and it has not been directly associated with timing except a few papers such as [6], since the timing estimation that takes into account dynamic voltage drop has not been well established. To insert necessary and sufficient decoupling capacitance without wasteful gate leakage, the impact of dynamic noise on timing must be accurately estimated.

To capture the impact of dynamic noise behavior on timing, static timing analysis under given noise waveforms has been studied [7], [8]. These methods eliminate dynamic behavior by assigning equivalent DC values to each instance. The DC values are computed by, for example, averaging the noise voltage within a time interval of interest so that time-variant voltage can be considered in each gate delay computation. This treatment necessarily increases gate delay when the voltage drops. However, focusing on each cell delay, this is not true, as [7] pointed out. [7] examines

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[†]The authors are with Semiconductor Technology Academic Research Center, Yokohama-shi, 222-0033 Japan.
[††]The author is with Osaka University, Suita-shi, 565-0871 Japan.

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a) E-mail: okumura.takaaki@starc.or.jp

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delay variation due to power noise separately for rise transition and fall transition, and shows that cell delay decreases in the case of fall transition under V_{dd} noise. [7] then proposed computing an equivalent DC voltage for each instance separately for rise and fall delays. This is also symmetrically applicable to ground noise. The accuracy was evaluated in 180 nm technology and confirmed to be reasonable. However, it is not clear whether [7] is still valid in current technologies, since the relation between voltage and delay has become much different as shown in Fig. 1, that is the higher delay sensitivity to voltage and its stronger non-linearity.

In this paper, we propose a dynamic noise aware timing analysis method that is compatible with conventional gate-level static timing analysis. We first examine the meaning of timing analysis based on static IR-drop analysis, and discuss its limitation. Next, to cope with high sensitivity and non-linearity, we carefully review the previous work proposed in [7], and point out two issues that degrade the estimation accuracy. When supply voltage drops and fall delay is considered, both increase and decrease in delay are observed in our analysis, whereas [7] estimates delay decrease only. To solve this problem, the proposed method computes two equivalent voltages corresponding to the input voltage level and the supply voltage of the gate. For the second issue, we carefully calculate the time interval in which the equivalent voltage level is computed in the proposed method.

The rest of paper is organized as follows. In Sect. 2, we discuss the meaning of timing analysis based on static voltage drop analysis. Sect. 3 reviews the conventional method [7] at the 45 nm technology node and shows that accuracy improvement is necessary. In Sect. 4, we present the proposed procedure for estimating delay fluctuation. Section 5 experimentally evaluates the proposed procedure and Sect. 6 concludes the paper.

2. The Relation between Static and Dynamic Analysis

This section reviews the meaning of timing analysis using static IR-drop analysis, and discusses the relation between static noise based and dynamic noise based analyses.

Let us express path delay fluctuation due to PG noise ΔD_{path} using delay sensitivity to voltage at each instance in a path as follows.

$$\Delta D_{path} = \sum_{i=1}^{n} \frac{\partial D_i}{\partial v} \Delta \overline{v}_i \tag{1}$$

$$\Delta \overline{v}_i = \frac{1}{T_i - T_{i-1}} \int_{T_{i-1}}^{T_i} \Delta v \, dt \tag{2}$$

Here, n is the number of stages and Δv is the difference between given noise waveform and regular supply voltage. T_i and D_i are arrival time at the i_{th}-stage gate output and stage delay of the i_{th}-stage gate, respectively. $\Delta \overline{v}_i$ is the equivalent voltage of Δv averaged between T_{i-1} and T_i, where this time window corresponds to the timing range when the i_{th}-stage gate is switching. ΔD_{path} is expressed as the sum of products of the sensitivity to voltage $\partial D_i/\partial v$ and the equivalent voltage $\Delta \overline{v}_i$.

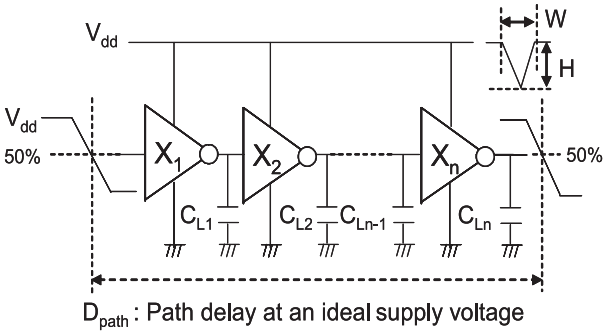

Fig. 2 Experimental circuit setup and parameter definitions.

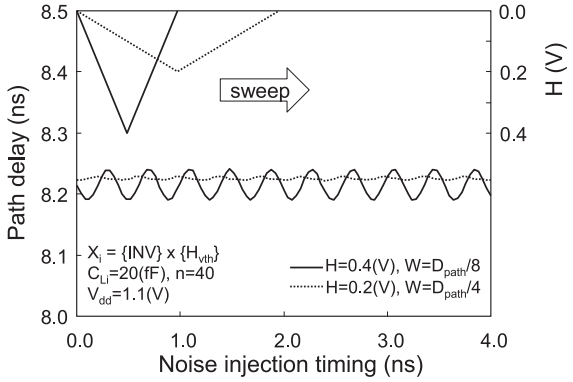

Fig. 3 Delay fluctuation of uniform topology case due to power supply noise at 45 nm technology.

The sensitivity $\partial D_i/\partial v$ is expressed as up to the m_{th}-order polynomial as follows.

$$\frac{\partial D_i}{\partial v} = a_{0i} + \sum_{j=1}^{m} a_{ji} \cdot \Delta \overline{v}_i^j \tag{3}$$

where a_{ji} is the j_{th}-order coefficient of the polynomial for the i_{th}-stage gate.

Here, under an assumption that each instance has the identical sensitivity ($a_j = a_{ji}$), Eq. (1) is simplified as

$$\Delta D_{path} = a_0 \int_{T_0}^{T_n} \Delta v \, dt + O(\Delta v^2). \tag{4}$$

Equation (4) means that delay fluctuation ΔD_{path} is expressed as a function of the integral of noise, and it does not depend on the noise waveform shape.

We experimentally confirmed the above property at a 45 nm technology node. Figure 2 depicts the setup and parameter definitions of the experiment. The regular supply voltage is 1.1 (V). We used triangular waveforms for power supply noise. In the experiments, we chose the width and height of the noise (W and H) so that the integral of noise was unchanged, and altered the noise injection timing.

Figure 3 shows the circuit simulation results as a function of noise injection timing. Solid and dashed lines correspond to different waveform shapes. The figure indicates that the fluctuations are nearly constant as long as the whole

noise waveform is included within the path timing window. That is, the delay fluctuation is mostly dependent on the integral of noise and almost independent of the noise shape.

This is the reason why static IR-drop analysis has been reasonably used in timing analysis for annotating voltage drop to each instance. When analyzing a path whose delay is close to the cycle time which is normally checked for setup constraints, the time interval between T_0 and T_n becomes almost the clock cycle, which means the noise integral in Eq. (4) is equivalent to the static IR-drop. Equation (4) assumes that each instance has an identical sensitivity. As long as the variation of sensitivity is not significant, the estimation of delay fluctuation based on static IR-drop analysis gives a good approximation.

Conversely, Eq. (4) cannot be used for short path delays, which are usually checked for hold constraints, since the time interval for integral differs greatly from cycle time.

More importantly, in cases where the sensitivity is much different instance by instance, the static noise voltage is not appropriate to estimate timing fluctuation. This situation can be often found in industrial designs. For example, large delay buffers are intentionally inserted in a high speed clock line to adjust the phase relative to external signal timing. Normally, the large delay buffers tend to have higher delay sensitivity to voltage. This problem could be aggravated when using multiple-V_{th} cells. If the inserted buffers have significantly different sensitivity from the others, it may result in timing failure due to noise. As shown in Sect. 2, the sensitivity becomes higher with technology scaling. To prevent or predict the timing failures, consideration of dynamic voltage drop in timing analysis is becoming indispensable in recent technologies.

3. Conventional Method and Its Problems

In this section, we introduce a conventional method to estimate delay fluctuation due to dynamic PG noise [7], and point out its problems through experimental evaluation in 45 nm technology.

[7] classified mechanisms to change the propagation delay into two categories; *Charge Change Case* and *Current Change Case*. In the following subsections, these two cases are examined. Since ground noise can be treated similarly, its discussion is omitted throughout this paper.

Figure 4 shows an example of circuits used for evaluation. Low and high V_{th} cells are included. We chose 0.2 and 0.4 (V) for the values of H and altered the noise injection timing similarly to Fig. 3. The delay fluctuations both by [7] and circuit simulation are computed.

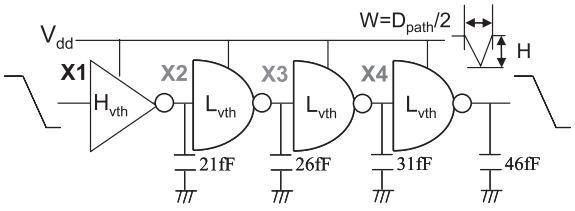

Fig. 4 An example circuit to evaluate [7].

Figures 5(a) and 5(b) show the evaluation results. The stage delays of each instance X1 through X4 are plotted. Solid and dashed lines represent the stage delay estimated by the conventional method and by SPICE simulation, respectively. We can see that the estimated traces are not consistent with the simulation results except X1 in Fig. 5 (a). We will now explain the *Charge Change Case* and *Current Change Case* and examine Fig. 5 considering the two cases.

3.1 Delay Increase in *Charge Change Case*

Figure 6 illustrates an example of *Charge Change Case* with an inverting cell. In the figure, the line labeled "noise" is a given power supply noise. The lines labeled "w/ noise" and "w/o noise" are the input/output signal waveforms of the cell under the power supply noise and an ideal supply voltage, respectively. Suppose that the output is falling under power supply noise. As shown in the figure, the voltage when the signal transition starts has already dropped through a conducting PMOS. In this case, the output swing is small and the amount of charge stored in the output loading changes, which results in a decrease in the propagation delay. Thus, the output voltage V_{t0} when the output transition starts is important, and hence V_{t0} is regarded as equivalent DC voltage in [7].

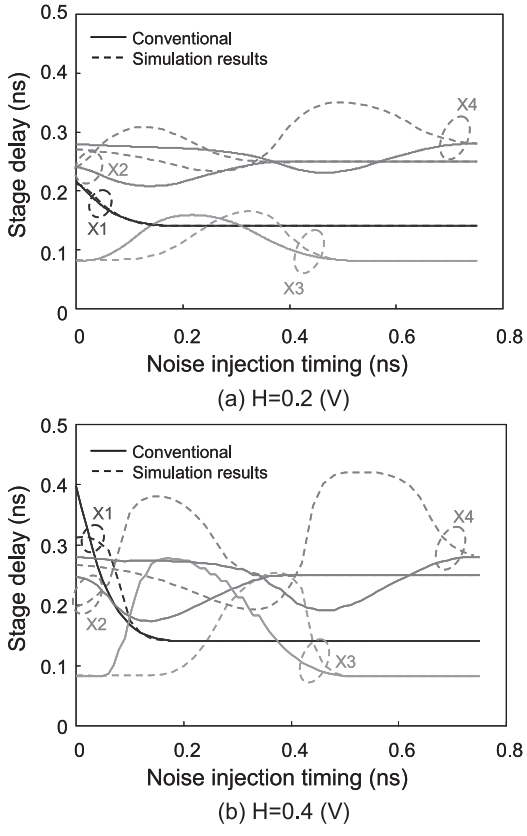

Fig. 5 Evaluation results of conventional method [7] at 45 nm technology.

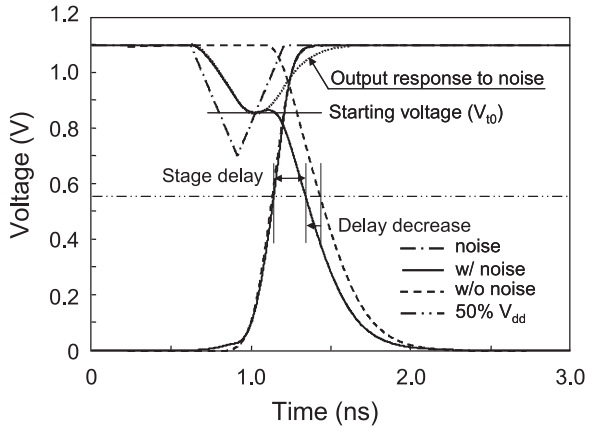

Fig. 6 Stage delay decrease in *Charge Change Case*.

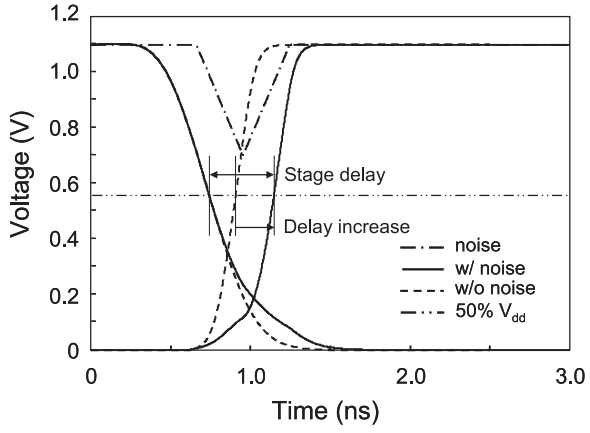

Fig. 7 Stage delay increase in *Current Change Case*.

In Fig. 5, instances X2 and X4 correspond to the *Charge Change Case*. The traces of the instances computed by [7] represent decrease in stage delay from the one at an ideal supply voltage (rightmost value of each trace). However, circuit simulation shows both increases in stage delays as well as decreases in stage delays independent of the values of H, which has not been pointed out before. As a result, the traces of instance X2 show a completely opposite tendency compared with the simulation results. Both increases and decreases in stage delay should be modeled to improve the accuracy otherwise the estimation becomes optimistic.

3.2 Voltage Interval to Average in *Current Change Case*

Let us suppose a rise transition under power supply noise, where this case is called *Current Change Case*. Figure 7 shows an example. The voltage drop reduces the current to charge output loading, and hence it increases propagation delay. The average voltage between $t1$ and $t2$ is empirically used as the equivalent DC voltage V_{dd_eq},

$$V_{dd\_eq} = \frac{1}{t2 - t1} \int_{t1}^{t2} V_{dd\_actual}\, dt, \tag{5}$$

where V_{dd_actual} is the supply voltage with noise, $t1$ is the time when the output starts transition, and $t2$ is the time when the output voltage swing becomes 60% of V_{dd} in [7]. For ease of calculation, [7] computes $t1$ and $t2$ from the transitional waveforms without power supply noise, and uses them in Eq. (5).

In Fig. 5, instances X1 and X3 correspond to this case. Here, let us look at instance X1. X1 is the first stage of the path, and so no earlier computation at upstream instances affects the result. In Fig. 5 (b), the trace of X1 computed by [7] starts with a pessimistic estimation at time 0, and then rapidly decreases to an optimistic estimate while the trace in Fig. 5 (a) shows a reasonable estimation. Our extensive evaluation under various conditions suggests that the interval in Eq. (5) is too narrow in the case of X1 in Fig. 5 (b). The estimations of X3 are more complicated, since it depends on the estimates of the upstream instances. In fact, the rising and falling slopes of the estimations are quite different from the simulation results in both of Figs. 5(a) and 5(b). Revising the time interval to average in Eq. (5) is needed to improve the accuracy and avoid optimistic/pessimistic estimation.

4. Proposed Stage Delay Computation

From the discussion in the previous section, revising averaging interval on the voltage in *Current Change Case* and capturing delay increase in *Charge Change Case* are needed to improve the estimation accuracy. This section describes how to solve these problems.

4.1 Revising Integration Interval to Average in *Current Change Case*

We here define $t1$ and $t2$ in Eq. (5) so that the estimated delay becomes more accurate, and describe how to obtain $t2$ in the stage delay computation. In the proposed method, $t1$ and $t2$ are set to 50% crossing times of the input transition and the output transition, respectively. This definition is reasonable, since the time interval between $t1$ and $t2$ is the propagation delay itself, and the impact of the supply noise on the stage delay is directly considered. The problem here is how to estimate $t2$, since $t1$ is already computed for upstream instances in STA.

The difficulty in estimating $t2$ originates in the dependency of $t2$ on the supply noise. Using the equivalent voltage approach, $t2$ is required to compute V_{dd_eq}, and V_{dd_eq} is necessary for $t2$ computation. We thus adopt an iterative computation. This procedure is illustrated in Fig. 8. In the figure, j and $T_{i,j}$ are the iteration counter and the arrival time of i_{th} stage gate in the j_{th} iteration, respectively. Δt is the time step to increase $T_{i,j}$ during the iterations. f represents the dependence of the stage delay on static voltage drop (ΔV), and it gives the stage delay increase.

The goal of the procedure is to find $t2$ satisfying that $(t2 - t1)$ equals to the stage delay $D_i + \Delta D_i$, where ΔD_i is estimated using Eq. (5) and $t2$. We first set $T_{i,0}(= t2)$ to $T_{i-1}(= t1) + D_i$. We then iteratively increase $T_{i,j}$ by a small step Δt, and estimate $\Delta D_{i,j}$ from the delay dependence

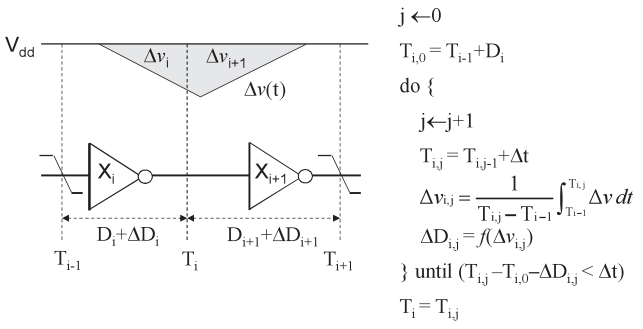

Fig. 8 An iterative procedure to obtain stage delay increase from voltage-delay characteristics.

on ΔV (f) using Eq. (5) and $T_{i,j}$. If the difference between $T_{i,j} - T_{i,0}$ and $\Delta D_{i,j}$ is smaller than Δt, the iteration finishes. Note that this procedure is independent of the noise waveform shape. Although the computational cost of forward time traversing is not significant, other efficient approaches, such as binary search, could be applied to reduce CPU time if necessary.

Note that if the delay dependence on ΔV (function f in Fig. 8) is linear and the fluctuation (ΔD_i) is relatively small to the original (D_i) as the 180 nm case in Fig. 1, the predefined time interval in Eq. (5) gives reasonable approximation. However, since the sensitivity is not linear in the 45 nm case in Fig. 1, detailed computation of the integration interval becomes essential.

4.2 Capturing Stage Delay Increase in *Charge Change Case*

The delay decrease in the *Charge Change Case* arises since the falling transition starts from the lower voltage. That is, this behavior is related to the power supply voltage of the instance of our interest.

On the other hand, the timing region of delay increase appears after the region of delay decrease in Fig. 5. In the delay increase region, the PMOS transistor is already OFF, and hence the behavior of the delay increase originates from NMOS transistor operation.

Figure 9 shows transitional waveforms in the delay increase region. The figure shows that the stage delay increases according to the non-monotonic change of gate input voltage due to the presence of noise. In this region, the discharging current flowing through NMOS is reduced due to lower V_{gs} voltage, which results in stage delay increase. Thus this behavior is related to the input voltage given to the instance. To capture the delay increasing behavior, the dependence of stage delay on input voltage level, which is not considered in [7], should be considered as well as the dependence on the supply voltage.

In *Charge Change Case*, both decrease and increase in stage delay ($\Delta D_i^{'}$,$\Delta D_i^{''}$) have to be considered. $\Delta D_i^{'}$ is estimated similarly to [7]. The voltage drop of the instance output due to noise at a specific time is estimated and used as an equivalent DC voltage drop ΔV_{dd}.

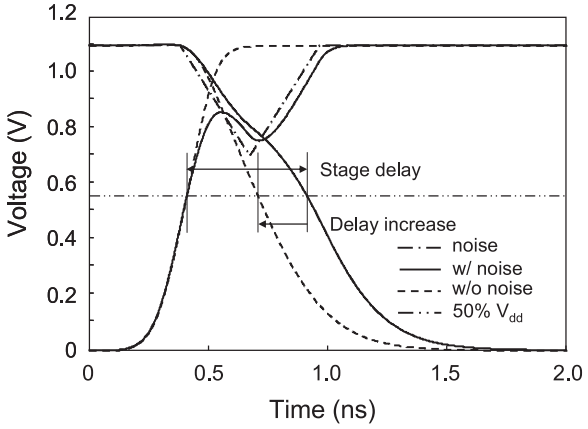

Fig. 9 Stage delay increase in *Charge Change Case*.

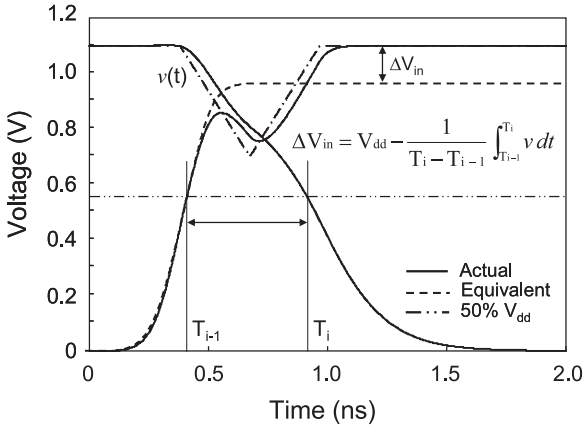

Fig. 10 Equivalent voltage of stage delay increase in *Charge Change Case*.

$\Delta D_i^{''}$ is estimated by regarding the noisy input waveform as the reduction in input voltage swing. The equivalent voltage reduction in input voltage ΔV_{in} is computed using integration, as shown in Fig. 10. When computing this integral, the time interval is important similarly to Eq. (5). To accurately estimate ΔV_{in}, we adopt an iterative computation presented in Sect. 4.1.

To obtain the gate delay using ΔV_{dd} and ΔV_{in}, some pre-characterization of each cell is necessary. Figure 11(a) explains a simulation setup for characterizing the decrease in stage delay. The relation between the power supply voltage drop (ΔV_{dd}) and stage delay decrease (ΔD_i) is characterized keeping the input voltage swing fixed. Figure 11(b) presents a setup to characterize the stage delay increase. The relation between the decrease in input voltage swing (ΔV_{in}) and stage delay increase (ΔD_i) is obtained while keeping power supply voltage (V_{dd}) and input transition-time (T_{in}) unchanged.

A question here is why the delay increase in the *Current Change Case* was missed in [7]. Figure 12 shows the ratio of stage delay fluctuation due to power supply noise depending on the noise injection timing, where a 10-stage inverter chain is evaluated at 180 nm technology node. The

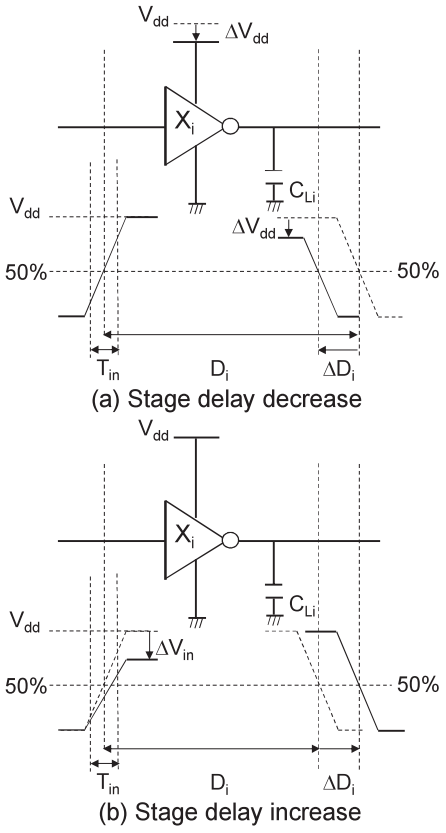

Fig. 11 Characterization for *Charge Change Case*.

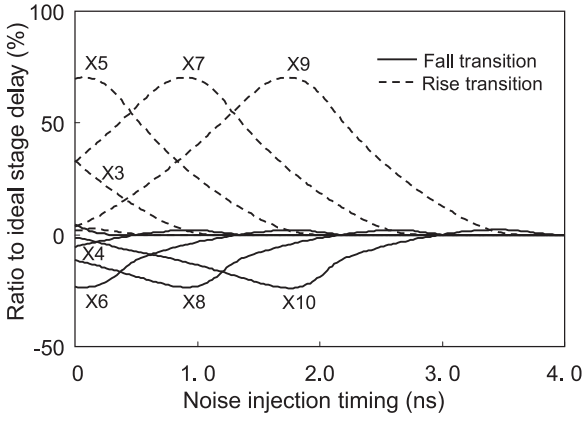

Fig. 12 Stage delay fluctuations due to power supply noise of 10 stages inverters at 180 nm technology.

shape of the noise is set as shown in Fig. 4. The peak voltage of power supply noise (H) is 0.4 (V). From the figure, the increase in falling stage delay (X4, X6, X8, X10) can be observed but its magnitude is negligibly small. This is because the decrease in over-drive voltage (V_{dd}–V_{th}) makes the discharging current sensitive to the input voltage level, which results in relatively large increase in stage delay. Thus, advanced technology necessitates more detailed analysis.

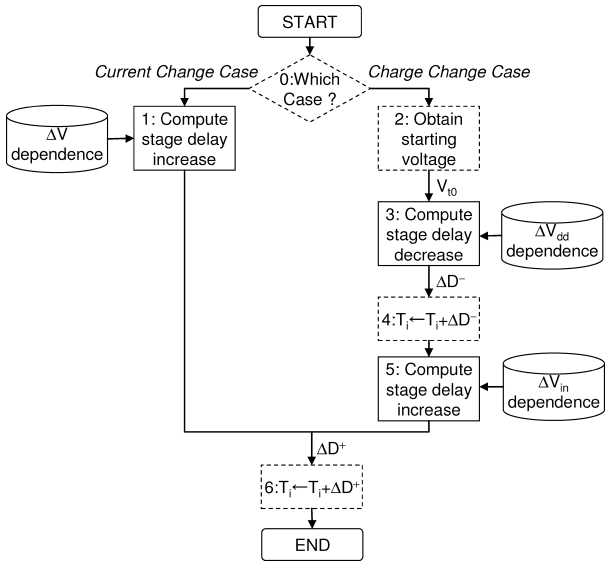

Fig. 13 The procedure of the proposed stage delay computations.

4.3 Proposed Stage Delay Computation Procedure

Figure 13 summarizes the proposed procedure to estimate the stage delay fluctuation due to the dynamic noise. In the figure, the solid squares correspond to the portions where we improved or added to [7].

Initially, in step 0, the signal transition is classified to the *Current Change Case* and the *Charge Change Case* as in [7].

In step 1, the stage delay increase ΔD^+ in the *Current Change Case* is estimated with the iterative computation of Fig. 8 using the dependence of the stage delay on ΔV as the function f. Here, the input voltage and supply voltage to a gate are changed simultaneously, and hence this dependence can be obtained by referring the conventional library [9].

In the *Charge Change Case*, firstly, the stage delay decrease is estimated. In step 2, the output response of the noise is considered to obtain the staring voltage of the transition (V_{t0}) similarly to [7]. The resulting V_{t0} is used in step 3 to obtain the stage delay decrease ΔD^- from the dependence of the stage delay on ΔV_{dd}. Then, the arrival time T_i is temporary decreased by ΔD^- in step 4. Since the input voltage swing and supply voltages are different and the dependence on ΔV_{dd} is not defined in the current library, the characteristics are needed to be additionally extracted as shown in Fig. 11 (a).

Secondly, in step 5, the stage delay increase ΔD^+ in the *Charge Change Case* is estimated with the iterative computation of Fig. 8 using the dependence of the stage delay on ΔV_{in} as the function f. Similarly to ΔV_{dd} dependence, ΔV_{in} dependence is not defined in the current library, an additional characterization shown in Fig. 11 (b) is necessary.

Finally, in step 6, the arrival time T_i is increased by ΔD^+ for the both cases.

5. Experimental Results

We implemented the proposed method and evaluated the accuracy in a 45 nm technology.

Figure 14 shows the results estimated using the proposed method for the same circuit with the same setup as Fig. 5. In the experiments, we characterized each stage with their typical input transition time and given output load to obtain the voltage drop dependences of stage delay. 0.0, 0.1 and 0.3 (V) were used as the voltage drop values in the characterization. The obtained stage delay fluctuations are fitted into quadratic equations and referred in the stage delay computation. The output response of the noise which is required for the stage delay decrease estimation in the *Charge Change Case* is also obtained from SPICE simulation.

From the figure, we can clearly see that the traces of instance X3 are improved thanks to the revision of the integral interval in Eq. (5). The figure also shows that the traces of instance X4 reproduce well both increase and decrease in the stage delay. The estimation of instance X2 in Fig. 14(a) and instances X1, X2 in Fig. 14(b) still include a certain amount of errors, but their tendency became more consistent with the simulation results rather than that of the conventional method.

We next evaluated the accuracy for various topologies. One hundred experimental circuits were randomly generated according to the parameter variations in Table 1 and used for the accuracy evaluation. The gates in each path were chosen from 12 combinations (3 logics × 2 drivability × 2 V_{th}). The output load of each stage was selected randomly in the range of [1, 30] (fF). The resulting path delay ranges from 0.5 ns to 1.85 ns.

The noise waveform was triangular and the height (H) and width (W) were chosen so that the average voltage within the typical path timing window ($\frac{W \times H}{2 \times D_{path}}$) is either 50 or 100 (mV). We set the time step in the iterative computation (Δt) to 5 ps. In the experiments, the voltage of the noise within the stage delay is either monotonic decrease, monotonic increase, or both. In addition, various noise slopes ($\Delta V/\Delta t$) are given, since the path delays are different. We thus expect that this experimental set covers a wide range of noise shape variation for each gate.

For each circuit, we performed timing analysis alternating noise injection timing by 10 ps within the timing window of the path, which results in 11,200 path delay computations. The CPU time consumptions of the SPICE reference and the proposed path delay computation were 8.6 hours and 13.3 seconds on AMD Opteron 2.3 GHz processor with 128 GBytes of memory for the one combination of W and H, respectively.

For the characterization, we used 25 combinations of input transition time and output load. That is, 900 (25 combinations × 12 cells × 3 supply voltages) SPICE simulations were conducted to obtain the conventional ΔV dependence

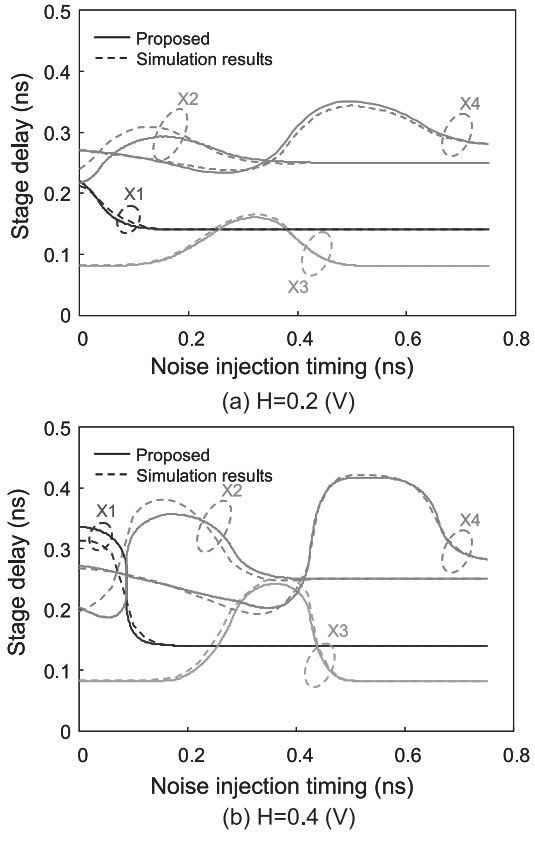

Fig. 14 Evaluation results of proposed method at 45 nm technology.

Table 1 Parameter variation for accuracy evaluations.

Parameter	Values					
X_i	INV, NAND2, NOR2					
Drivability	x1, x8					
Cell V_{th}	H_{vth}, L_{vth}					
CL_i	[1, 30] (fF)					
#stages	10					
W	D_{path}		D_{path}·2/3		D_{path}/2	
H (V)	0.1	0.2	0.15	0.3	0.2	0.4
#circuits	100					

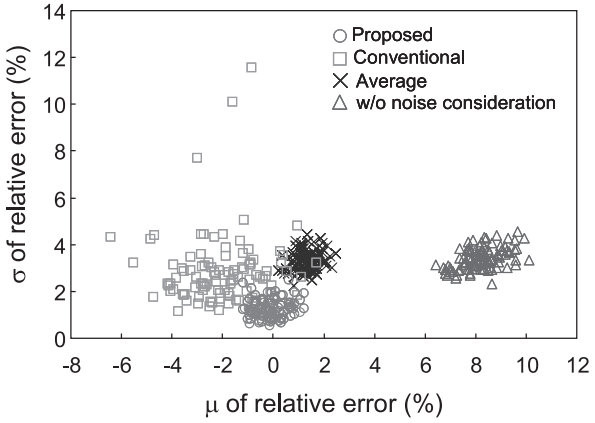

Fig. 15 Accuracy evaluation results of estimation methods for delay fluctuation due to power supply noise at 45 nm technology (H=0.2 (V), W=D_{path}/2).

Table 2 Summary of accuracy evaluation results at 45 nm technology.

Estimation Methods	Estimation Error (%)											
	$W=D_{path}$				$W=D_{path}\cdot 2/3$				$W=D_{path}/2$			
	H=0.1(V)		H=0.2(V)		H=0.15(V)		H=0.3(V)		H=0.2(V)		H=0.4(V)	
	μ	σ	μ	σ	μ	σ	μ	σ	μ	σ	μ	σ
without noise consideration	5.8	3.8	12.7	7.8	7.4	3.7	15.9	7.2	8.2	3.4	17.0	6.2
Average	3.7	3.7	6.4	7.6	2.1	3.6	3.5	6.9	1.4	3.3	2.3	5.9
Conventional	2.8	1.7	4.4	3.2	2.7	2.0	3.5	5.8	2.2	2.9	3.3	9.4
Proposed	0.60	0.80	0.88	1.4	0.53	1.0	0.88	2.1	0.49	1.3	1.0	2.7

of the stage delays, which consumed 6.7 minutes of the CPU time. In addition, the proposed method requires the dependences of the stage delays on ΔV_{in} and ΔV_{dd}. To obtain those, 1,200 (25 combinations × 12 cells × 2 voltage drop values × 2 characteristics) SPICE simulations were carried out. 500 (#stages/2 × #circuits) of SPICE simulations are also conducted to obtain the output responses to the noise. The CPU time consumptions for the new characterization and the output responses were 7.9 minutes and 4.6 minutes, respectively.

We define the estimation error. The error for the l_{th} noise injection timing of the k_{th} circuit is computed as the relative error to the SPICE simulation as follows.

$$E_{k,l} = \frac{D_{path,Est,k,l} - D_{path,Ref,k,l}}{D_{path,Ref,k,l}} \tag{6}$$

where $D_{path,Est,k,l}$ and $D_{path,Ref,k,l}$ are the path delays obtained from the estimation and the SPICE simulation for the l_{th} noise injection timing of the k_{th} circuit, respectively. The average and standard deviation of the relative error for the k_{th} circuit, M_k and S_k, are computed as the average and standard deviation of $E_{k,l}$ with respect to l, respectively. Then, the average and standard deviation of the estimation error for the all circuits are computed as the average of $|M_k|$ and S_k with respect to k, respectively.

Figure 15 shows an example of the evaluation results for the case of H=0.2 (V) and W=$D_{path}/2$. The horizontal and vertical axes are the average and standard deviation of the relative error, respectively.

The delay variation ratios due to the noise itself are shown in the figure labeled "w/o noise consideration," and the average ranges 6.4% to 10.1% and the standard deviation 2.3% to 4.6%. Unless any design strategies to cope with power supply noise are applied, a timing margin which is larger than the fluctuations should be set.

For each of circuit, we experimentally obtained average voltage drop ΔV_{ave},

$$\Delta V_{ave} = \frac{\int_{T_0}^{T_n} \Delta v dt}{T_n - T_0} = \frac{W \times H}{2 \times (D_{path} + \Delta D_{path})} \tag{7}$$

which is equivalent to the static IR-drop in the cases where the path delay is equal to the cycle time. Please recall that T_0 and T_n are defined in Sect. 2. When the timing fluctuation is estimated based on ΔV_{ave} (labeled "Average" in the figure), the relative errors are greatly reduced to within 2.5% average with 4.4% standard deviations. The average and standard deviation of the estimation errors are 1.4% and 3.3%, respectively. Static IR-drop based approach does not take the noise injection timing and waveform into account, and hence the delay variation that is dependent on noise injection timing should be taken into account as a timing margin.

The conventional and proposed methods are expected to eliminate redundant timing margins since they take into account the noise injection timing and dynamic waveform. However, the relative errors of the conventional method are −6.4% to 1.7% on average with 1.1% to 11.6% standard deviation. The average and standard deviation of the estimation errors are 2.2% and 2.9%, respectively. Due to the problems discussed in Sect. 3, the estimation is not accurate.

On the other hand, the estimation accuracy is improved by the proposed method. The relative error ranges from −1.2% to 1.2% on average with 0.5% to 2.5% standard deviation. The average and standard deviation of the estimation errors are 0.49% and 1.3%, respectively.

The evaluation results are summarized in Table 2. As shown in the table, the estimation error of the proposed method ranges within 1% on average and 2.7% of standard deviation among all the experiment conditions. By solving the dominant issues that degrade estimation accuracy in [7], gate delay computation under dynamic power supply noise that is compatible with conventional STA has been established in this work. The improvement in accuracy helps to reduce timing margin for guard-banding, and thus the proposed method contributes to enhancement in performance and/or timing convergence.

6. Conclusions

In this paper, we discussed the estimation of stage delay fluctuation due to power supply noise. Firstly, we pointed out two problems in the conventional method; (1) delay increase in *Charge Change Case* was not considered, (2) predefined time interval for averaging supply voltage was not valid due to high delay sensitivity to voltage and its nonlinearity.

We then proposed a gate delay computation for estimating delay fluctuation that iteratively updates the time interval. Delay increase in the *Charge Change Case* is estimated by computing equivalent DC voltages both of input voltage and supply voltage. The evaluation results show that the proposed procedure estimates delay fluctuation well to within 1% on average with 2.7% standard deviation. The proposed method computes increase/decrease in stage delay

at the 50% crossing point, and hence it has a good compatibility with STA applications.

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Takaaki Okumura received the B.S. and M.S. degrees in information engineering from Shinshu University, Nagano, Japan, in 1986 and 1988, respectively. He is with Fujitsu VLSI Ltd., Kasugai,Japan, from 1988. Since 2008, he is on loan to Semiconductor Technology Academic Research Center (STARC), Yokohama, Japan.

Fumihiro Minami received the B.E. and M.E. degrees in 1982 and 1984, respectively, from Tokyo Institute of Technology, Japan. He joined Toshiba Corporation, Kawasaki, Japan, in 1984. He had been involved in developing physical design methodology, low power design methodology and timing analysis methodology including signal and power integrity. Since 2009, he has been on loan to Semiconductor Technology Academic Research Center (STARC), Yokohama, Japan, where he is researching and developing variation aware design methodology.

Kenji Shimazaki received the B.S. and M.S. degrees in Electrical Engineering from the Keio University in 1988 and 1990, respectively. He joined Panasonic Corporation, Kyoto Japan, in 1990, where he is currently a senior engineer at System LSI Technology Development Center, Semiconductor Company. He received Ph.D. from Kobe university, Japan, in 2007. In 2008, he was temporarily transferred to the Semiconductor Technology Academic Research Center (STARC), Yokohama, Japan, where he has been researching and developing power and supply noise analysis and optimization. He is currently interested in the area of computer-aided design with an emphasis on variation aware analysis and optimization of high-speed SoC.

Kimihiko Kuwada received the B.S. degree in physics from Yamaguchi University, Yamaguchi, Japan, in 1998. Since 1998, he works for NEC Micro Systems Ltd., Kumamoto, Japan. From 1998 to 2008, he had been engaged in developing EDA tools to design LSI, such as Transistor-level simulator, Cell characterization tool. Since 2009, he is on loan to Semiconductor Technology Academic Research Center (STARC), Yokohama, Japan.

Masanori Hashimoto received the B.E., M.E. and Ph.D. degrees in Communications and Computer Engineering from Kyoto University, Kyoto, Japan, in 1997, 1999, and 2001, respectively. Since 2004, he has been an Associate Professor in Department of Information Systems Engineering, Graduate School of Information Science and Technology, Osaka University. His research interest includes computer-aided-design for digital integrated circuits, and high-speed circuit design. He is a member of IEEE and IPSJ.