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Measurement Circuits for Acquiring SET Pulse Width Distribution with Sub-FO1-Inverter-Delay Resolution

Ryo HARADA[†,††a)], ***Student Member***, **Yukio MITSUYAMA**[†,††b)], **Masanori HASHIMOTO**[†,††c)], ***and*** **Takao ONOYE**[†,††d)], ***Members***

SUMMARY This paper presents two circuits to measure pulse width distribution of single event transients (SETs). We first review requirements for SET measurement in accelerated neutron radiation test and point out problems of previous works, in terms of time resolution, time/area efficiency for obtaining large samples and certainty in absolute values of pulse width. We then devise two measurement circuits and a pulse generator circuit that satisfy all the requirements and attain sub-FO1-inverter-delay resolution, and propose a measurement procedure for assuring the absolute width values. Operation of one of the proposed circuits was confirmed by a radiation experiment of alpha particles with a fabricated test chip.

key words: *soft error, single event transient (SET), pulse width, measurement circuit*

1. Introduction

As devices integrated on VLSIs are minitualized, critical charge, which is the minimum charge to cause a bit flip (single event upset: SEU) or a glitch (single event transient: SET), becomes smaller, and functional correctness has been threatened by such soft errors. SEU and SET arise when radiation particles, such as alpha particles and neutrons, collide with Si substrate and electrons/holes whose amount is larger than the critical charge are induced and collected into sensitive nodes. Recently, neutron-induced soft error is becoming a concern even at the sea level [1]–[4].

When an SET pulse, which is generated in a combinational circuit, propagates to a sequential element (e.g. a flip-flop) and is captured at clock edges, the SET pulse causes a error. A wider SET pulse more probably causes an error, because there is a wider range of clock timing at which the SET pulse is mistakenly captured [5]. Generally, suppression and correction of SET-oriented errors are performed using time and/or space redundancy [6]. However, they have to pay a large performance penalty in speed and/or area depending on the reliability requirement and SET pulse width distribution. Therefore, information on the distribution of SET pulse width is eagerly demanded for SET-oriented soft error estimation [7] and suppression [6].

To characterize the distribution of SET pulse width at the sea level, accelerated neutron radiation tests, in which the neutron energy spectrum at the sea-level is reproduced, are performed at some sites, such as Los Alamos. Meanwhile, several circuits have been proposed and successfully used for measuring the SET pulse width [8]–[11]. They directly measure the pulse width of each SET [8], [9], [11], or indirectly estimate the distribution of the SET pulse width from the statistic of SET errors [10]. However, they have remaining issues to resolve on obtaining the distribution with high resolution in time and/or high certainty in absolute values of pulse width.

In this work, existing measurement circuits are reviewed from five requirements, which consist of fine time resolution, wide time range, tolerance to soft errors, ability to obtain a large number of samples, and certainty of measured width, that are essential to achieve precise SET measurement and their problems are discussed. We then propose two circuits; (1) uses electrical masking for filtering SET pulses in terms of the pulse width, and (2) uses Vernier delay line [12] for pulse width evaluation for satisfying four requirements. Here, electrical masking is an effect that vanishes a pulse when propagating through a logic gate whose delay is comparable or larger than the pulse width. To meet the fifth requirement, that is certainty of measured width, we introduce a measurement procedure using an integrated pulse generator that can vary the pulse width continuously and assure the pulse width even though the pulse generatior itself is influenced by manufacturing variability. We experimentally confirm the operation of the proposed circuit based on electrical masking and the procedure using an implementation on a 65nm test chip and an Am-241 foil as an alpha particle source.

The remainder of this paper is organized as follows. Section 2 explains the outline of existing techniques and examines their effectiveness and limitations. Section 3 presents the proposed measurement circuits, and a pulse generator circuit for assuring the measured width is introduced in Sect. 4. Experimental results are shown in Sect. 5, and the conclusion is given in Sect. 6.

2. Requirements for SET Measurement and Conventional Measurement Circuits

This section first describes requirements for measuring distributions of SET pulse width. We then introduce and examine conventional measurement circuits in terms of the re-

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[†]The authors are with the Department of Information Systems Engineering, Osaka University, Suita-shi, 565-0871 Japan.
[††]The authors are with JST, CREST, Tokyo, 102-0075 Japan.
a) E-mail: harada.ryo@ist.osaka-u.ac.jp
b) E-mail: mituyama@eng.osaka-u.ac.jp
c) E-mail: hasimoto@ist.osaka-u.ac.jp
d) E-mail: onoye@ist.osaka-u.ac.jp

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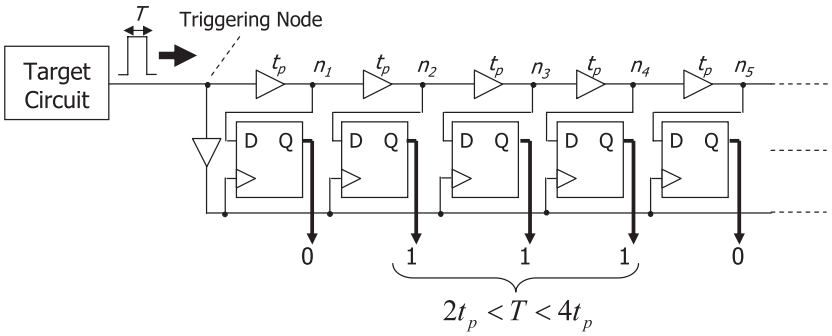

Fig. 1 Schematic of pulse-triggered capturing circuit. The example with $N = 3$ is shown.

quirements.

2.1 Requirements

We below enumerate five requirements for SET measurement in accelerated radiation tests.

R1: fine time resolution
To measure SET pulse width accurately, fine time resolution that is smaller than FO-1 inverter delay is desirable.

R2: wide time range
Measurable minimum pulse width should be FO-1 inverter delay, or minimum pulse width of data and/or clock for FF latch operation. The upper bound must be set to a large value because the pulse width is widely distributed.

R3: tolerance to soft errors
In radiation tests, soft errors necessarily occur even in the measurement circuit. To avoid mis-operation and mis-measurement, the measurement circuits should be soft error tolerant.

R4: ability to obtain a large number of samples
To obtain a confident statistical distribution of SET pulse width, measurement circuits must be area/time-efficient, since radiation time and allowed silicon area are limited.

R5: certainty of measured width
The time resolution and measurable range of pulse width is sensitive to the manufacturing variability. A scheme to verify the performance of the fabricated measurement circuit is necessary.

From now, representative measurement circuits that have been proposed in [8]–[10] are examined from these five points. [11] estimated SET pulse width by measuring supply current of an on-die logic gate with an external real-time oscilloscope and on-die probing. However, the simplicity of measurement and required equipments and skills are much different, and hence [11] is not discussed further in this paper.

2.2 Pulse-Triggered Capturing Circuit

Pulse-triggered capturing circuit has been used in [8], [9]. In this circuit, delayed SET pulse is captured in FFs, where the amount of delay is different for each FF. The SET pulse is also used as a trigger signal and the same trigger signal is given to all the FFs. Therefore, the stored values in FFs correspond to the SET pulse width.

We here introduce [8] as an implementation of this circuit. Figure 1 shows the schematic of the circuit with exemplifying its operation. It consists of a target circuit in which SETs arise, a buffer chain[†], and a D-FF chain. Here, a pulse expander, which was used in [8], is omitted, since it can be also used for other measurement circuits. The triggering node is connected with clock terminals of all the D-FF through a buffer. Suppose an SET has come into this circuit and just reached the clock terminal of the D-FFs. At this timing, each D-FF stores the value at the corresponding node in the buffer chain. In this example, 0, 1, 1, 1, 0 are stored, which means voltages at nodes n_1 and n_5 were low and those at n_2, n_3 and n_4 were high at the timing.

The SET pulse width T satisfies

$$(N-1)t_p < T < (N+1)t_p, \tag{1}$$

where t_p is the propagation delay of a buffer, and N is the number of D-FFs storing 1. By reading out the stored values, we can approximately estimate $T \cong Nt_p$.

Let us check out the five requirements. The minimum resolution of this circuit is equal to the propagation delay of a buffer (inverters), and it can not be reduced further. The measurable range of the pulse width can be extended by increasing the number of stages as long as the area permits. When SET is generated in the buffer chain, it does not arrive at the clock terminals and just vanishes. On the other hand, an SET generated in the clock buffer at the bottom changes the values stored in D-FFs, however they are all zero and easily distinguishable. Therefore, the measurement circuit is immune to SETs. By using SEU-tolerant latch, such as DICE [13], mis-estimation due to SEUs can be eliminated. Basically, there is no restrictions on the target circuit and any target circuits with large sensitive area to SET can be used, whereas we should pay attention to propagation induced pulse broadening (PIPB) effect [14] when designing

[†]An inverter chain can be used for improving time resolution instead of a buffer chain, however here the buffer chain is used for simplifying the explanation of the operation.

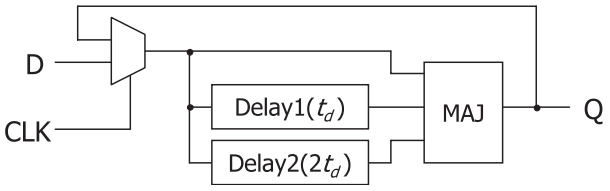

Fig. 2 Temporal latch structure.

a long combinational gate chain as the target circuit. The problem of PIPB effect can be separately discussed from the measurement circuit, and hence we do not discuss it further. A problem is that t_p is different chip by chip and fluctuated even instance by instance due to manufacturing variability.

2.3 Temporal Latch Circuit

Figure 2 shows a temporal latch used in [10]. It consists of a multiplexer, a majority gate, and two current-starved delay circuits that have the propagation delay of t_d and $2t_d$ respectively. By regarding the selection signal of the multiplexer as a clock, this circuit works as a latch, and [10] constructed a shift register using temporal latches. Suppose an SET pulse arises in the majority gate or the multiplexer. When the pulse width is smaller than t_d, the pulse can not go through the lower two paths, and hence the output Q is unchanged. On the other hand, a pulse whose width is larger than t_d causes an output transition. The temporal latch captures this output transition, and then we can perceive that an SET pulse whose width is larger than t_d has arisen.

A problem of this circuit is that the sensitive area to SET occupies a small portion of the temporal latch, and the number of SET pulses per area is small. This means that long radiation experiment and/or large silicon area are necessary to obtain large number of SET samples. In addition, to perform the measurement with different t_d, we need to reconfigure t_d and measure repeatedly. This approach makes the radiation test even longer, and hence is not practical. Another approach is to integrate several circuits with different t_d, which needs large silicon area and considerably degrades area efficiency.

The pulse width resolution is decided by t_d, and the minimum t_d, which is the minimum measurable width, is two inverter delays of FO-1. Large t_d is easily realizable by increasing the number of gate stages. This measurement circuit is soft error tolerant because SETs in delay circuits are masked in majority gate and the remainders are targets for SET measurement. Besides, it is necessary to presume t_d for assuring the pulse width.

3. Proposed Measurement Circuits

This section presents two novel measurement circuits that attain sub-FO1-inverter-delay resolution.

3.1 Measurement Circuit Using Electrical Masking

The measurement circuit using electrical masking, which is proposed in this work, consists of a target circuit, a delay element (filter) chain, and 1-bit counters as illustrated in Fig. 3. Each delay element has different delay values T_{th} and works as a filter that eliminates pulses whose width is smaller than its propagation delay T_{th} thanks to electrical masking. Suppose that an SET comes into the measurement circuit from the target circuit, and the output of the first 1-bit counter is toggled. In this case, we can perceive that an SET whose width is larger than $T_{th,1}$ has arisen. In addition, the pulse that has passed through the first delay element is injected into the second delay element, and the width is further examined successively. To classify SET pulses on the basis of their widths, the delay elements are designed so that T_{th} increases as the delay element becomes distant from the target circuit, i.e. $T_{th,i} < T_{th,i+1}$. If the outputs of the 1-bit counters are 1, 1, 0, 0 as illustrated in Fig. 3, the pulse width T is estimated as $T_{th,2} < T < T_{th,3}$. By checking the outputs of the 1-bit counters periodically, we can know the number of pulses for each range of width.

Difference of T_{th} in consecutive filters is the time resolution of the proposed circuit. T_{th} of each filter can be adjusted by the number of fan-outs (or another factor), the presented circuit attains fine resolution below FO1-inverter-delay. In this measurement circuit, $T_{th,1}$ corresponds to the lower bound of the pulse width that can be measured with the 1-bit counter. By increasing the number of filters and 1-bit counters, the upper bound of measurable pulse width can be extended. The number of SETs measured can be increased by adopting a larger target circuit with large sensitive area. Moreover, SEU occurrences in the 1-bit counters can be eliminated, because when a toggle is observed in a 1-bit counter, the upstream 1-bit counters must toggle either. If not, the toggle is judged as an SEU. In sacrificing the measurement results of the first filter, all SEUs can be removed from the measurement results. Meanwhile, this circuit also needs a presumption system to estimate the threshold values.

Let us exemplify the circuit configuration which can achieve R1 and R2 in a 65 nm process. In the 65 nm process, the minimum pulse widths of data and clock for a standard D-FF operation are estimated to be 32 ps and 33 ps by circuit simulation. Also, the rise and fall propagation delays of a standard FO-1 inverter are 9.1 ps and 10.6 ps. By using 10 filter circuits with adjusted fan-outs, the performance of 5 ps resolution and 34–79 ps measurable range listed in Table 1 was achieved. Here, the performance was evaluated by circuit simulation assuming that wiring capacitances are proportional to the number of fan-outs. Therefore, we confirm that the proposed circuit with the above configuration attains sub-FO1-inverter-delay resolution, and measures the pulses that can be captured in D-FF, though strictly speaking, a small difference of 1–2 ps exists.

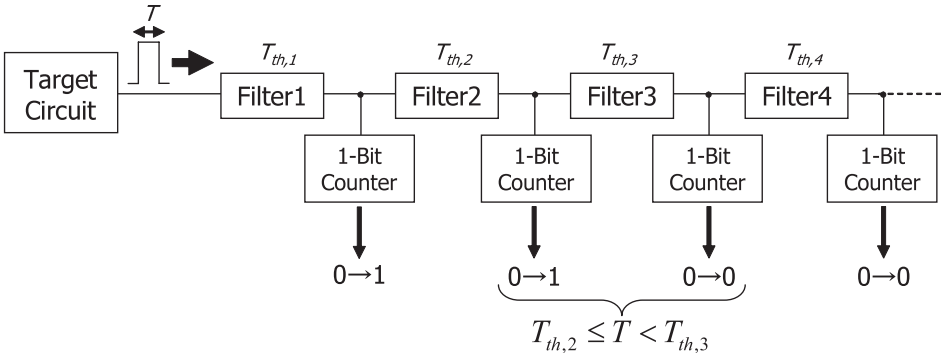

Fig. 3 Proposed measurement circuit using electrical masking. $N = 2$ case is illustrated.

Table 1 An example of #fan-outs and filter threshold.

Filtering circuit	1	2	3	4	5	6	7	8	9	10
#Fan-outs	1	5	6	7.5	11	12.5	15.5	21	25	30
T_{th} [ps]	34	39	44	49	54	59	64	69	74	79

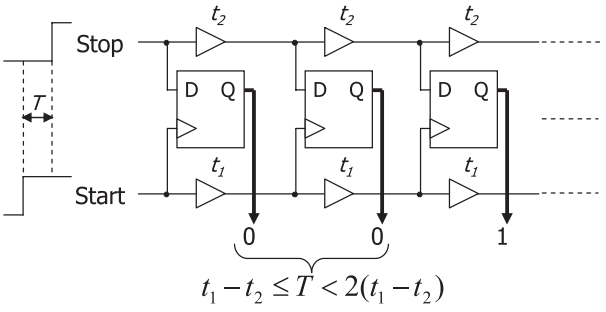

Fig. 4 Circuit configuration of Vernier delay line. The case of $N = 2$ is shown.

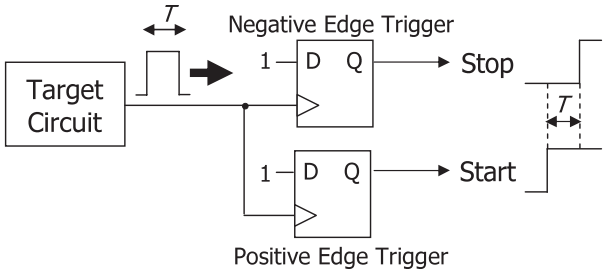

Fig. 5 Two D-FFs of positive edge trigger and negative edge trigger.

3.2 Vernier Delay Line Circuit

Next, Vernier delay line (VDL) is introduced for SET measurement. VDL is composed of two buffer chains and a D-type latch chain, as illustrated in Fig. 4. Two step signals (START and STOP) with T time difference are given to this circuit, and T is to be measured by VDL. The buffer delay of the chain for START signal t_1 is larger than that for STOP t_2. START chain gives clock signals and STOP chain provides data signals to latches. START and STOP signals race and finally STOP signal overtakes START signal. When these signals propagate through a single stage, the time difference between them, which was initially T at the input, is reduced by $t_r = (t_1 - t_2)$. Latches, where the time difference becomes 0 or below, store 1 and the others latch 0. Letting N denote the number of latches storing 1, the time difference T is estimated by

$$(N-1)t_r \le T + t_s < Nt_r, \tag{2}$$

where t_s is the setup time of latch.

To use VDL for SET measurement, we devised a circuit configuration in Fig. 5. Two D-FFs are inserted between the target circuit and VDL. The output of the lower FF changes from low to high at the rising edge of SET pulse, and that of the upper FF transitions at the falling edge. Thus, START and STOP signals with T time interval are generated.

In this measurement, t_r is the time resolution. When propagation delays t_1 and t_2 are finely adjusted by, for example voltage-controlled buffer [12], the pulse width resolution can be improved to be less than FO-1 inverter delay. For example, [15] achieved 4.8 ps resolution in 65 nm process. Similarly to pulse-triggered capturing circuit, the upper range of measurable width can be extended by increasing the number of stages, and assurance of t_r after fabrication is necessary. As for the measureable minimum pulse width, latches store 0 unless STOP signal becomes t_s faster than START signal. For this reason, VDL can measure the time difference T as long as T is larger than t_r. Therefore, the measureable minimum pulse width is determined by the minimum clock pulse in Fig. 5 and this circuit satisfies R2 for the same reason as the measurement circuit using electrical masking. Next, the SEU tolerance of this circuit is examined. The values stored in latches before overtaking should be 0, and after overtaking they should be 1. If an SEU flips a latch, this condition is not satisfied, which means the SEU is distinguishable and can be eliminated. SETs generated in the buffer chains do not cause mis-measurement. SETs in STOP line are not captured since no clock edges are given to latches. When SETs arise in START line, all the values

Table 2 Summary of requirements and satisfaction.

Condition	R1	R2	R3	R4	R5
Pulse-Triggered Capturing Circuit	NG	OK	OK	OK	NG
Temporal Latch Circuit	OK	OK	OK	NG	NG
Circuit using Electrical Masking	OK	OK	OK	OK	NG
Vernier Delay Line Circuit	OK	OK	OK	OK	NG

stored in latches become zero and this case is easily distinguishable. Thus, Vernier delay line circuit is robust to soft errors.

3.3 Summary of Requirements and Satisfaction

Table 2 summarizes the requirements described in Sect. 2.1 and the satisfactions of the circuits discussed in Sects. 3.1 and 3.2. We can see that the proposed two circuits satisfy R1-R4 requirements though pulse-triggered capturing circuit and temporal latch circuit do not satisfy R1 and R4, respectively. However, R5 is not satisfied in all the circuits. In order to satisfy R5, next section will present a pulse generator for assuring the measured pulse width coping with manufacturing variability.

4. Assurance of Pulse Width Using on-Chip Pulse Generator

The proposed measurement circuits use delay elements, and a problem is that their delay is sensitive to manufacturing variability. An approach is to implement and measure replica of delay elements, however this approach can not cope with random manufacturing variability and misestimation of wiring capacitance. We thus implement an on-chip pulse generator to inject a pulse whose width itself can be assured by measurement. This approach is general since it is applicable to any types of SET measurement circuits and the correspondence table between pulse width and observable result can be built. On the other hand, on-chip pulse generators was also implemented in [9] aiming at the assurance of the pulse width. However, it is necessary to assure the performance after fabrication of the implemented pulse generators, which is also fluctuated by manufacturing variability. To assess the width of pulses generated by each pulse generator after fabrication, we incorporate a mechanism for the post-silicon assessment into the pulse generator.

We here show an implementation of on-chip pulse generator. The circuit composition and operation example of the pulse generator are shown in Fig. 6(a). It adopts an exclusive-or gate and a delay element as depicted in Fig. 7 similarly to [9], [10]. In this circuit, an input transition is converted into a pulse whose pulse width is equal to the propagation delay of the delay element. To cancel out the MUX delay, MUX gates are inserted in both paths to the XOR inputs. To continuously change the pulse width, the pulse generator is implemented so that the power supply voltage in the dotted rectangle in Fig. 6, VDD_d, can be varied separately. When the changeable range of t_d is not large

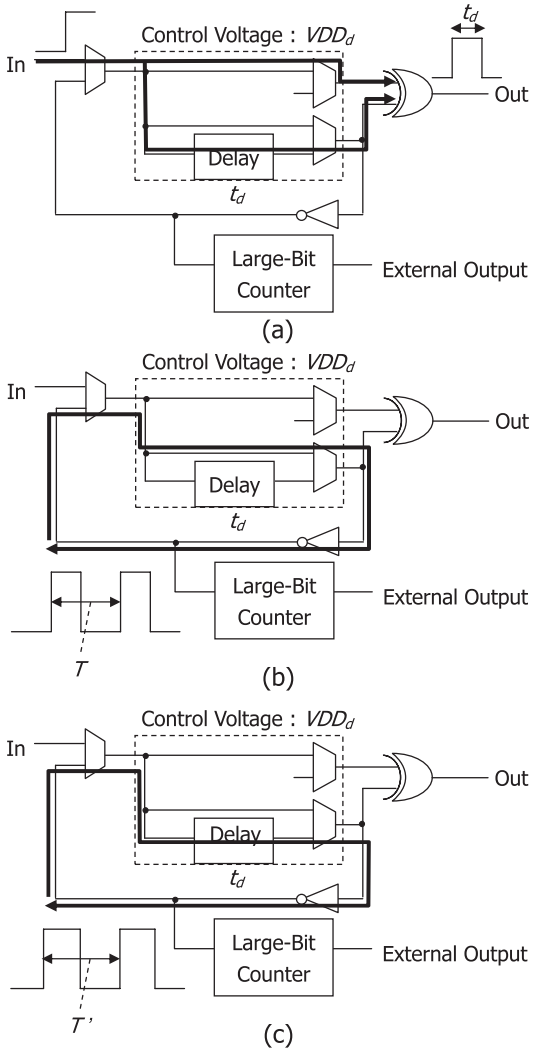

Fig. 6 Schematic and operation examples of on-chip pulse generator: (a) pulse generation with t_d width, (b) oscillation using the path without delay circuit, and (c) oscillation using the path including t_d.

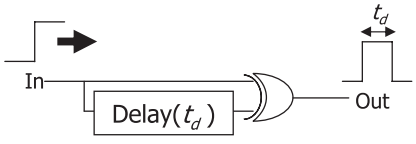

Fig. 7 Schematic of general pulse generator that uses an XOR gate.

enough, increasing the number of MUX inputs and choosing a delay element from several ones extend the changeable range.

Meanwhile, t_d is influenced by manufacturing variability as mentioned above, and then t_d should be measured after fabrication to assess the width of the generated pulse. The assessment process of t_d is explained in the following. The circuit is configured to oscillate by changing the select signal of the left MUX. The oscillating period T of the path without delay circuit (Fig. 6(b)) is calculated from the counts in the large-bit counter. Similarly, the oscillating

period T' of the path including t_d (Fig. 6(c)) is calculated. Based on these two oscillating periods, t_d is obtained by

$$T' - T \cong 2t_d. \quad (3)$$

To minimize the mismatch between t_d and the generated pulse width, the inverter in the figure should be small.

5. Measurement Results

To confirm the operation of the measurement circuit using electrical masking, which is one of the proposed measurement circuits, a test chip was fabricated in the 65 nm process. A micrograph of the test chip is shown in Fig. 8. Figure 9 shows the organization of the test circuit. The circuit is composed of a pulse generator, a target circuit that is 204-stage inverter chain, and the measurement circuit with 9 filters.

The alpha particle tests were performed using an Americium-241 foil whose flux is $9 \times 10^9\,\mathrm{cm}^{-2}\mathrm{h}^{-1}$. The radiation source was put immediately above on the test chip [16] and the outputs of 1-bit counters were observed at room temperature with 0.8 V operating voltage.

Figure 10 shows the measured distribution of SET pulse width in case of 17-hour radiation. The number of SETs measured during this test is 40, after SEUs arisen in the measurement circuit are eliminated. The error cross section in the 204 inverters during the tests is caluculated as $2.6 \times 10^{-2}\mu\mathrm{m}^2$ while the sensitive area is $12.5\,\mu\mathrm{m}^2$, whereas the sensitive area is defined as the total area of sesceptive drain regions. Although a similar inconsistency is also reported in [17], further investigation is necessary. The threshold values T_{th} of 8 filters were estimated before the radiation using the procedure described in Sect. 4. The measurable range of pulse width was 116 ps to 807 ps. We can see the proposed circuit is applicable to SET measurement.

6. Conclusion

We have developed new circuits for measuring SET pulse width in accelerated neutron radiation experiment. To attain sub-FO1-inverter-delay resolution, two circuits are devised; one uses electrical masking and the other adopts Vernier delay line. We also presented a procedure to assure the measured pulse width using on-chip pulse generator that can change pulse width. The experiment of alpha-particle radiation with a fabricated test chip confirmed that the proposed measurement circuit using electrical masking can be used for obtaining SET pulse width distribution. In future work, to more precisely measure SET pulse width, we will investigate the influecne of PIPB effect and inconsistency of the error cross section.

Acknowledgments

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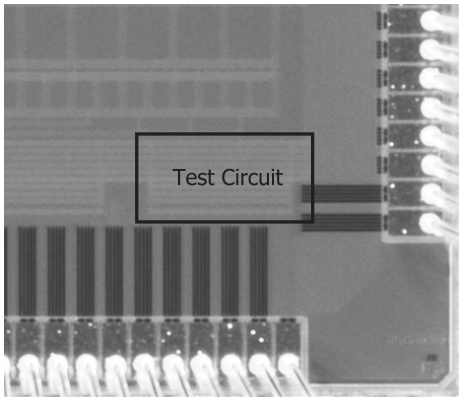

Fig. 8 A micrograph of the test chip in a 65 nm process. The sensitive area of the target circuit is about $12.5\,\mu\mathrm{m}^2$.

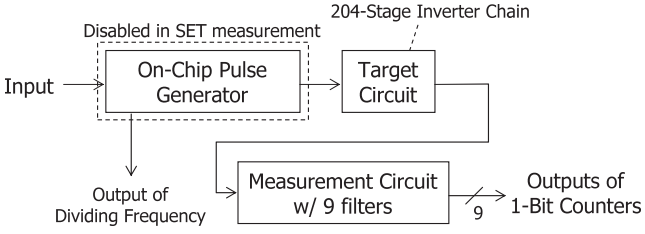

Fig. 9 Composition of the test circuit.

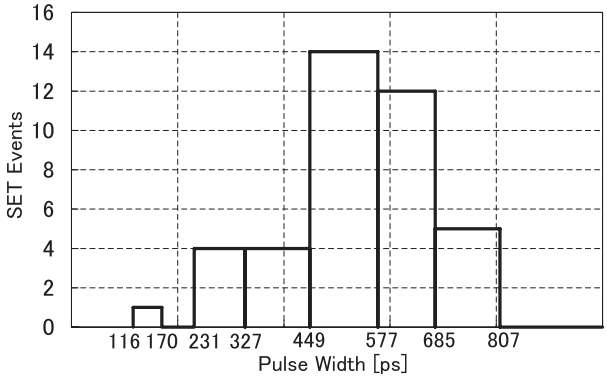

Fig. 10 Distribution of measured SET pulse width.

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Ryo Harada received the B.E. degree in Information Systems Engineering from Osaka University, Osaka, Japan, in 2009. He is currently pursuing the M.E. degree in the Department of Information Systems Engineering at Osaka University. His major interest is soft error mitigation technique. He is a student member of IEEE.

Yukio Mitsuyama received B.E., M.E., and Ph.D. degrees in Information Systems Engineering from Osaka University, Japan, in 1998, 2000, and 2010, respectively. He is currently an assistant professor in Graduate School of Engineering, Osaka University. His research interests include reconfigurable architecture and its VLSI design. He is a member of IEEE, and IPSJ.

Masanori Hashimoto received the B.E., M.E. and Ph.D. degrees in Communications and Computer Engineering from Kyoto University, Kyoto, Japan, in 1997, 1999, and 2001, respectively. Since 2004, he has been an Associate Professor in Department of Information Systems Engineering, Graduate School of Information Science and Technology, Osaka University. His research interest includes computer-aided-design for digital integrated circuits, and high-speed circuit design. Dr. Hashimoto served on the technical program committees for international conferences including DAC, ICCAD, ASP-DAC, ICCD and ISQED. He is a member of IEEE and IPSJ.

Takao Onoye received the B.E. and M.E. degrees in Electronic Engineering, and Dr.Eng. degree in Information Systems Engineering all from Osaka University, Japan, in 1991, 1993, and 1997, respectively. He is currently a professor in the Department of Information Systems Engineering, Osaka University. His research interests include media-centric low-power architecture and its SoC implementation. He is a member of IEEE, IPSJ, and ITE-J.