Setup Time, Hold Time and Clock-to-Q Delay Computation under Dynamic Supply Noise

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***Abstract*- This paper discusses how to cope with dynamic power supply noise in FF timing estimation. We first review the dependence of setup and hold time on supply voltage, and point out that setup time is more sensitive to supply voltage than hold time and hold time at nominal voltage is reasonably pessimistic. We thus propose a procedure to estimate setup time and clock-to-Q delay taking into account given voltage drop waveforms using an equivalent DC voltage approach. Experimental results show that the proposed procedure estimates setup time and clock-to-Q delay fluctuations well with 5% and 3% errors on average.**

I. Intriduction

Recently, Power/Ground voltage level fluctuation (PG noise) is becoming a primary concern in designing LSI products with the progress of technology scaling. Current density in a chip has been increasing due to increase in operating frequency and power consumption. Moreover, lowering supply voltage with technology scaling, over-drive voltage (V_{dd}-V_{th}) is decreasing, which results in higher sensitivity of gate delay to power supply voltage [1]. On the other hand, [2] predicts that PG noise level is nearly constant despite lowering power supply voltage. These tendencies make circuit timing more susceptible to supply noise, and hence timing verification taking PG noise into account is essential for successful chip design.

Several gate delay estimation methods considering a given noise waveform have been proposed to capture the impact of dynamic noise behavior on timing [1][3][4]. These methods assign equivalent DC voltage to each instance by averaging the noise within a time interval of interest to eliminate dynamic behavior. [3] classified the delay variation due to power noise into two categories and carefully calculates the equivalent DC voltage for rise/fall transition to reproduce the stage delay decrease as well as the stage delay increase. Then, [1] improved [3] to overcome inaccuracy originating from higher nonlinearity and sensitivity unique to advanced technology, and shows that the stage delay fluctuations can be estimated well within few percent errors.

On the other hand, under dynamic voltage drop, capturing the delay fluctuations arisen only in combinational circuits is not obviously enough for accurate timing verification, since setup and hold time of Flip-Flop (FF) also play important roles in timing verification. However, the variations of setup and hold times under dynamic voltage drop and their estimation have not been clarified.

Besides, focusing on FF setup and hold times, there are several studies on interdependence between setup and hold time [5][6]. Conventionally, though the setup and hold times are characterized independently, [5][6] pointed out that the setup and hold times of an FF are interchangeable, that is, the hold time can be relaxed when the setup timing is critical, and vice versa. Furthermore, [7] experimentally compares the variations between combinational circuit delay and setup/hold times under constant voltage drop, and pointed out a cancellation behavior. However, to the best of our knowledge, the variation of setup and hold times and clock-to-Q delay under dynamic voltage drop has not been discussed so far.

In this paper, we discuss how to estimate setup and hold times and clock-to-Q delay under given dynamic voltage drop. We first investigate their tendencies under dynamic voltage drop and show that the setup time becomes optimistic while the hold time constraint becomes pessimistic under the noise. We then propose an estimation procedure of the setup time and clock-to-Q delay under the dynamic noise on the basis of [1], and evaluate the estimation accuracy.

The rest of paper is organized as follows. In Sect. II, we review the setup and hold times and examine the necessity/unnecessity to consider the dynamic voltage drop. In Sect. III, we propose an estimation procedure of setup time and clock-to-Q delay under dynamic noise. Sect. IV experimentally evaluates the proposed procedure and Sect. V concludes the paper.

II. Review of Setup and Hold Times

A. Characterization Procedure

Figure 1 shows the circuit diagram of a popular positive edge triggered FF cell [8], and this structure is evaluated throughout this paper. The cell has clock signal input terminal CK, data input terminal D, and output terminal Q. When CK signal is low, the signal path consisting of instances X2 and X3 is enabled to update the value of internal node M1 to the given input signal of D, while the slave latch consisting of instances X5 and X6 outputs the internally stored value to Q. When CK signal is high, clocked inverter X2 is disabled and then the stored value in the master latch consisting of X3 and X4 is outputted to Q through X5 and X7.

Figure 2 illustrates the timing definition of setup and hold skews. The setup skew is defined as the arrival time difference between D and CK, and the hold skew is defined as the arrival time difference between CK and D. The setup time and hold time are defined in textbooks as the amount of time that a given data must be stable before the capturing clock edge and the data must remain stable after the capturing clock edge, respectively. Conventionally, setup and hold times are independently characterized as the setup and hold skews so that the increase in CK-to-Q delay remains within a certain

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amount of percentage (e.g. 10%) [9]. Hereafter, this allowable delay increase is called "CK-to-Q degradation criterion". As shown in Fig.3, the CK-to-Q delay increases drastically as the setup skew becomes small. Without allowing the delay degradation, the setup time would be very large. Note that the CK-to-Q delay needs to be increased simultaneously according to the degradation criterion to keep the consistencies. To explore the boundaries of allowable CK-to-Q delay, heuristic approaches, such as binary search method, are employed, which makes the FF characterization time-consuming.

B. Setup Time and Its Dependence on Supply Voltage

In FF of Fig. 1, the setup time is correlated with D-to-M1 delay and CK-to-XCK delay, since internal node M1 should be stable to capture the data signal safely while CK signal is low. Therefore, the setup time becomes large under the conditions when the stage delays of X2, X3, and/or X1 become large, such as large input transition time of CK or D. This is also valid for supply voltage drop.

Figure 4 plots the setup time dependence on supply voltage with several CK-to-Q degradation criteria given to the characterization. The figure shows that the setup time is sensitive to supply voltage and becomes 2 to 3 times longer when the supply voltage is dropped from 1.0V to 0.8V. The observed tendency is independent of the CK-to-Q degradation criteria. Thus, the setup time at the nominal supply voltage is the loosest setup constraint, and hence the dependence of setup time on supply voltage should be re-examined, and an appropriate setup time must be given to STA.

C. Hold Time and Its Dependence on Supply Voltage

An intuitive understanding of hold time is that D should be stable before XCK is given to X2, X4 and the switch. This means that the hold time is tightly related to CK-to-XCK (X1) delay and is expected to become larger as X1 delay increases.

Figure 5 shows the hold time dependence on supply voltage with several CK-to-Q degradation criteria. Given the strict CK-to-Q degradation criterion of 1%, the hold time is positive and becomes larger as X1 delay increases according to lowering supply voltage, which is consistent with above understanding.

However, with CK-to-Q degradation criterion of 5%, the hold time is insensitive to supply voltage, and above 5% the tendency becomes opposite, which means the hold time is relaxed according to supply voltage drop. Let us explain the reason. In the cases of 7% and 10%, incomplete storing in the master latch at CK capturing edges is acceptable, as long as additional time needed to stabilize the stored value is within CK-to-Q degradation criterion. In this case, lower supply voltage requires longer time to stabilize the stored value.

Suppose the stage delay of X1 is not large enough to dominate CK-to-Q delay with CK-to-Q typical (5-10%) criteria. In other words, the hold time could be interpreted as the time required to make the master latch stable prior to the capturing clock edge and takes negative value in this situation. The important point here is that the amount of allowing delay

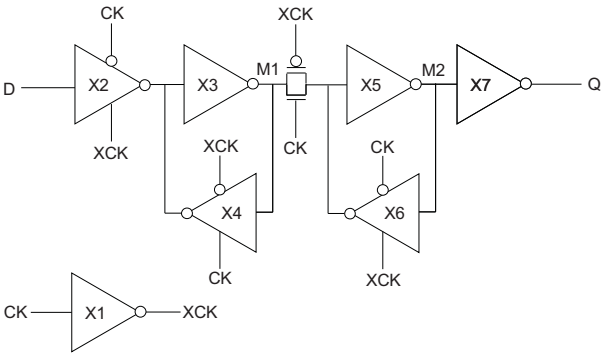

Fig. 1. Circuit diagram of Flip-Flip.

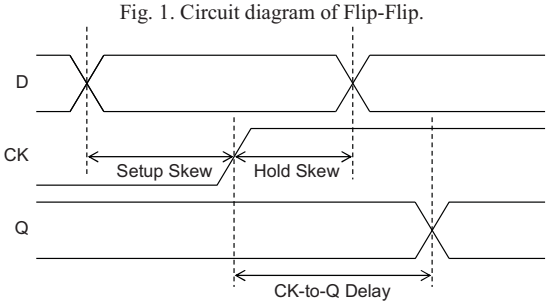

Fig. 2. Timing definitions of setup/hold skews.

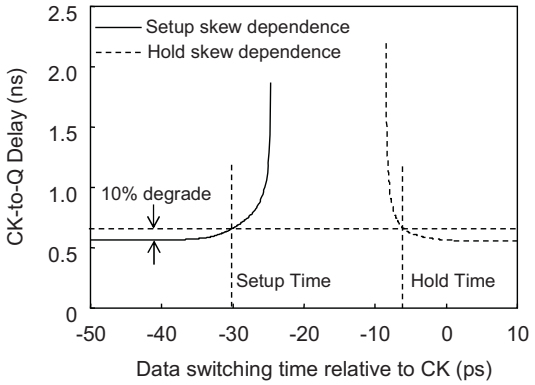

Fig. 3. Relation between CK-to-Q delay and setup/hold skews.

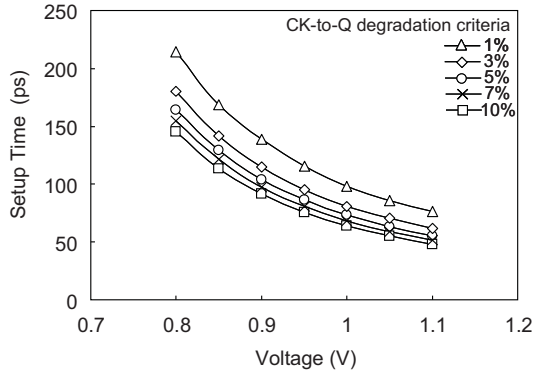

Fig. 4. Setup time dependence on supply voltage.

degradation can be consumed in the required time to make the master latch stable and which results in the relaxation of the hold time constraint. This scenario is also valid for the occurrence of supply voltage drop.

Looking at Fig. 5, revising the hold time under the dynamic voltage drop seems to be dispensable at glance, since the hold time at nominal supply voltage (here, 1.1V) is not

necessarily pessimistic. On the other hand, FF characterization is often carried out with CK-to-Q degradation criteria of 5 to 10% range in industry, as far as the authors know. In this range, the hold time at nominal voltage is the upper bound with reasonable pessimism, since the variation of hold time due to supply voltage is small. We thus conclude that the hold time at nominal voltage is given to STA.

III. Setup Time and CK-to-Q Delay Estimation under Dynamic Voltage Drop

A. Setup Time Dependence on Dynamic Voltage Drop

Figure 6 shows the setup time variation when a dynamic voltage drop waveform is given. The waveform was obtained from analysis results of a commercial tool [10] and we applied it to each cell as a supply voltage. The timing of clock edge injection was alternated and the setup time for each injection timing was characterized with 10% CK-to-Q degradation criterion. In the figure, the variation of CK-to-Q delay, CK-to-M2 delay, D-to-M1 delay, and CK-to-XCK delay are also shown.

The figure shows that, as we discussed in Sect. II, the setup time can be associated with CK-to-XCK delay and D-to-M1 delay and increases in the timing range of 10.4 ns to 10.9 ns. The figure also indicates that the setup time variation is well correlated with that of D-to-M1 delay.

B. Setup Time and CK-to-Q Delay Estimation Considering Dynamic Voltage Drop

Reference [1] presents a gate delay estimation method taking into account given dynamic noise waveforms. The method derives an equivalent DC voltage V_{dd_eq} that makes the gate delay at V_{dd_eq} equal to the actual gate delay under the dynamic noise, and then compute the gate delay using V_{dd_eq}. The method computes V_{dd_eq} by integrating noise w.r.t. time.

$$V_{dd\_eq} = \frac{1}{t2-t1}\int_{t1}^{t2} V_{dd\_actual}\, dt\,, \qquad (1)$$

where V_{dd_actual} is the supply voltage with noise, $t1$ and $t2$ are the time when the input and output voltage swing become 50% of V_{dd}, respectively. The difficulty here is how to estimate t_2, since t_2 is required to compute V_{dd_eq}, and V_{dd_eq} is necessary for t_2 computation. To deal with this problem, [1] adopts an iterative computation as shown in Fig. 7. The goal of the computation is to find t_2 satisfying that (t_2 - t_1) equals to the stage delay D_i+ΔD_i, where ΔD_i is delay variation due to noise and estimated using Eq. (1) and t_2. Initially, $T_{i,0}$ (=t_2) is set to T_{i-1} (=t_1)+D_i. Then, in the j_{th} iteration, $T_{i,j}$ is increased by a small step Δt, and estimate $\Delta D_{i,j}$ from the function f of voltage-delay characteristics using Eq. (1). The iteration will finish if the difference between $T_{i,j}$ - $T_{i,0}$ and $\Delta D_{i,j}$ becomes smaller than Δt.

[1] also discusses the necessities of the separate treatment for rise and fall transitions to estimate the gate delay fluctuations accurately, since V_{dd} drop affects rise and fall delays with different mechanisms. On the other hand, looking at D flip-flop structure of Fig. 1, rise and fall transitions occur in pairs, i.e. X2-X3 and X5-X7. [1] pointed out that path

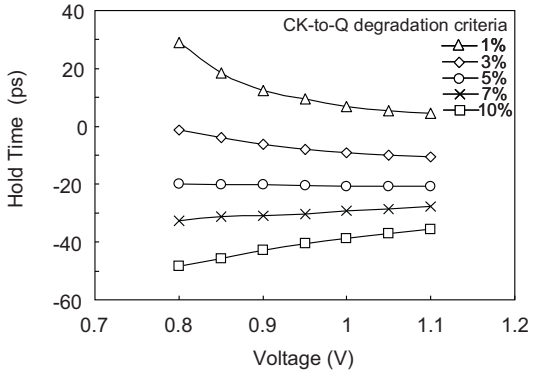

Fig. 5. Hold time dependence on supply voltage.

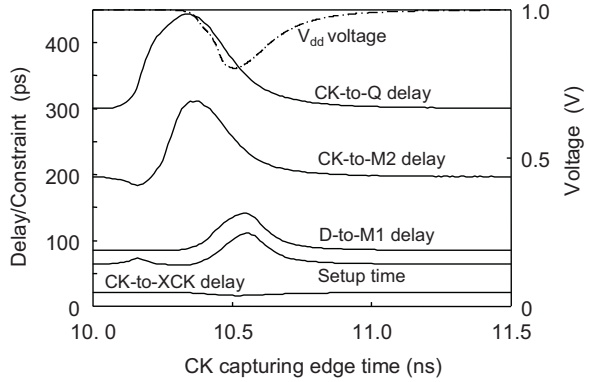

Fig. 6. Setup time dependence on dynamic voltage drop.

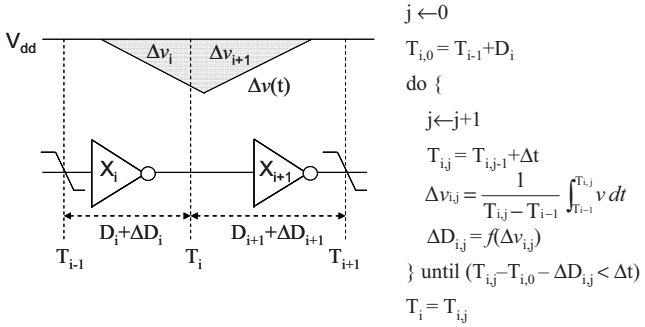

Fig. 7. An iterative procedure to obtain stage delay increase from voltage-delay characteristics.

delays can be estimated well using the average supply voltage during the path operation as long as the voltage-delay sensitivity difference between the stages is insignificant. This was also experimentally validated on silicon [11]. We thus expect that the estimation procedure in Fig. 7 gives a reasonable estimate of CK-to-Q delay.

The setup time corresponds to the stage delays of internal instances as we discussed in Sect. II, and hence the above expectation is also applicable to the setup time estimation. However, the setup time is the time interval between data switching time and capturing clock edge, and then the procedure should be revised slightly as follows.

Initially, $T_{i,0}$ is set to T_{ck} - T_{setup} where T_{ck} and T_{setup} are capturing clock edge time and setup time at nominal supply voltage, respectively. Then, in the j_{th} iteration, $T_{i,j}$ is decreased

by a small step Δt and estimate $\Delta D_{i,j}$ using Eq. (1) from the setup time dependence on voltage as shown in Fig. 4. The iteration will finish if the difference between $T_{i,0}$ - $T_{i,j}$ and $\Delta D_{i,j}$ becomes smaller than Δt.

Figure 8 shows an estimation example of the CK-to-Q delay and setup time under the dynamic voltage drop. The solid and dashed lines are the estimation results and the SPICE reference, respectively. The figure shows that the estimates are consistent with the references. It should be noted that if a strict delay degradation criterion (e.g. 1%) is applied to FF characterization, the hold time also becomes optimistic under the dynamic voltage drop. In that case, the setup time estimation procedure can be applied to the hold time estimation focusing on X1 delay.

IV. Experimental Results

We confirmed the accuracy of the estimation procedure discussed in Sect. III with an experimental circuit. We used a 45nm industrial design which consists of 300K instances. The operating frequency is 100MHz. We picked up two hundreds capture FFs on setup critical paths and extract each output load and input transition times of CK and D. We then applied the dynamic voltage drop waveform as the supply voltage of each FF. The given waveform is the same as Fig. 6. In the experiments, we altered the capturing clock edge time within the first 10% of the cycle time (1ns). The accuracy was evaluated as the relative error between the estimate and SPICE reference. The relative error was computed for each FF at every clock edge timing, and then for each FF the average error was calculated. For comparison, we also estimated setup time using static IR-drop which is an average voltage within a cycle time. This approach is widely used in industrial design flow.

Figure 9 plots the estimation errors of each FF. X-axis is the setup time at nominal supply voltage. As shown in the figure, the proposed method achieves smaller errors compared to "static IR-drop" method. The average errors of the proposed and "static IR-drop" methods are 5.33% and 11.4%, respectively. We also evaluated the CK-to-Q delay. The average errors of the proposed and "static IR-drop" methods are 3.02% and 11.1%, respectively. The proposed method can reduce the estimation error by more than 50%, which contributes to avoid optimism in static timing analysis.

V. Conclusion

In this paper, we discussed variations of setup time, hold time and CK-to-Q delay due to dynamic voltage drop. Through experimental reviews, hold time is less sensitive to supply voltage, and with ordinary 5-10% CK-to-Q degradation criteria hold time at nominal voltage maintains reasonably conservativeness. We thus proposed a method to estimate setup time and CK-to-Q delay under dynamic voltage drop. The experimental results show that the proposed method estimates the setup time fluctuation well with 5% error on average. The proposed method can eliminate the optimism of timing estimate caused by dynamic voltage drop.

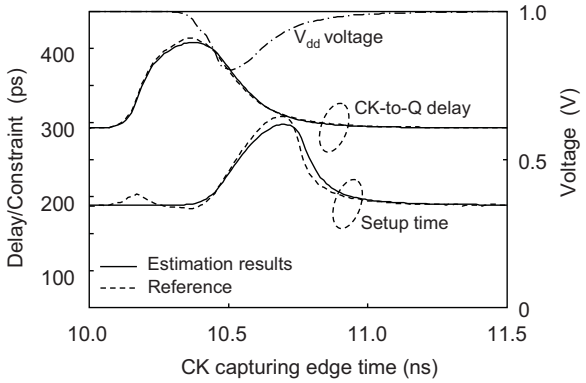

Fig. 8. Comparison between reference and estimation results of CK-to-Q delay and setup time.

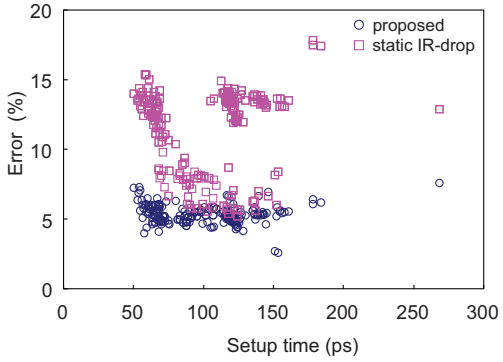

Fig. 9. Accuracy evaluation results of setup time estimation.

Acknowledgments

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