Measurement of On-chip I/O Power Supply Noise and Correlation Verification between Noise Magnitude and Delay Increase due to SSO

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Abstract

This paper presents measurement results of on-chip noise on power and ground rings for I/O (input/output) cells in a simple test structure fabricated in 90nm process. We also show measured timings of an output signal from chip to PCB board, and examine the relation between the magnitude of I/O power supply noise and the output transition timings.

Introduction

As chip-to-chip signaling throughput grows, estimation and mitigation of I/O timing jitter have been studied[1]. For such signals, high-quality chip-to-board transmission lines are provided. On the other hand, for cheaper commodity products, the number of I/O pins is directly related to the production cost, and hence designers are pressured to reduce the number of power/ground pins for both core and I/O cells as much as possible for cost reduction.

This work focuses on the power integrity for I/O cells, and evaluates power/ground noise waveforms using on-chip noise sensors[2]. With the measured noise waveforms and output transition timings, the timing shift of output transitions, i.e. delay due to SSO (simultaneous switching outputs) [3], is explored.

Test Structure and Measurement Setup

We fabricated a simple test structure that can change the number of SSO from one to three (OUT1, OUT2 and OUT3) in 90nm process as shown in Fig. 1. Each of them outputs a clock signal given from PLL through an output buffer. Depending on the SSO numbers, power and ground noises on rings for I/O cells are expected to vary. I/O pins labeled “VDDIO” and “VSSIO” are dedicated to supply power and ground voltages to I/O rings.

To sense VDDIO and VSSIO, noise measurement macros called “gated oscillator” [2], which is a ring-oscillator-based circuit but it captures dynamic noise waveforms thanks to intermittent operation at the timing of interest, are used. In this test chip, three macros, which are responsible to VDDIO, VSSIO and VDDIO–VSSIO respectively, are integrated. After fabrication, the chip was mounted on a QFP package and put on a PCB board through an IC socket. For each pair of VDDIO and VSSIO, 0.1μF chip capacitor is inserted near the socket as a decoupling capacitor. In addition, 47μF tantalum capacitor is placed on board.

In measurements, I/O supply voltage VDDIO is set to 2.1V. A reference clock given to the PLL is 10MHz, and the PLL outputs 100MHz clock. When the noise and the output voltage are measured, one input buffer for the reference clock and the output buffers under consideration are active, and other I/O buffers are quiet. To measure the output waveform of OUT1 us-

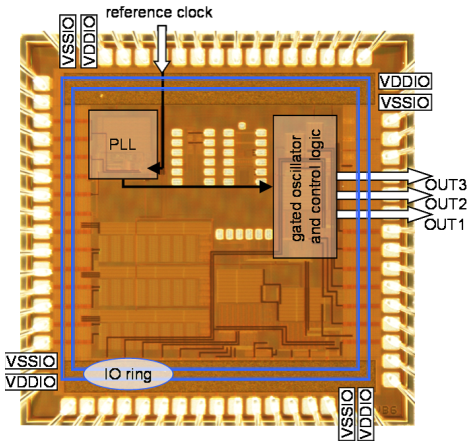

Figure 1: Chip photo and circuit outline. Chip size is 2.5mm x 2.5mm. #pads is 72.

ing a real-time oscilloscope, we attached an active probe to pin OUT1, where the input capacitance of the active probe is 1pF. We also connected a passive probe, as necessary, whose input capacitance is 9pF to OUT1 to see the dependency of the output transition timing on the supply noise. To other outputs OUT2 and OUT3, additional output loads are not connected.

Measured Noise Waveforms

The noise waveforms of VDDIO and VSSIO were measured (Fig. 2-5). Figs. 2 and 4 depict VDDIO and VSSIO noises when an active probe is attached to OUT1. Figs. 3 and 5 are noises when both active and passive probes are attached to OUT1. Note that the externally given VDDIO and VSSIO are 2.1V and 0V. We can see that the noise magnitude becomes larger as the number of switching output buffers increases, which is reasonable since the increases in VDDIO and VSSIO current enlarge VDDIO drop and VSSIO bounce, respectively. Looking at the presence of the passive probe, the average VDDIO, especially after 5,900ps, becomes smaller when both active and passive probes are attached. A similar tendency is found in VSSIO noise.

Correlation between Noise Magnitude and Output Transition Timing

We also measured the output transition waveforms of OUT1 varying the number of switching output buffers and the presence of the passive probe. We then computed the successive ten transition timings regarding the reference clock to PLL as the reference timing (Fig. 6). Here, the reference clock frequency is 10MHz and the clock frequency at the PLL output is 100MHz. During a single cycle of the reference clock, ten transitions ap-

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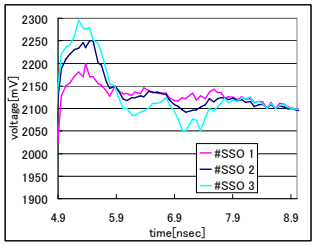

Figure 2: VDDIO noise (active probe is attached to OUT1).

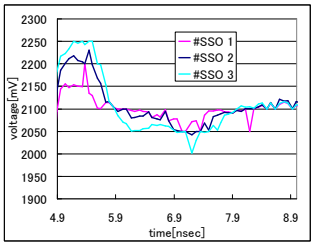

Figure 3: VDDIO noise (active and passive probes are attached to OUT1).

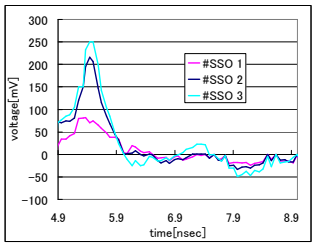

Figure 4: VSSIO noise (active probe is attached to OUT1).

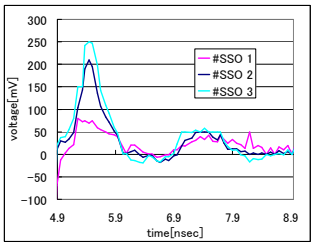

Figure 5: VSSIO noise (active and passive probes are attached to OUT1).

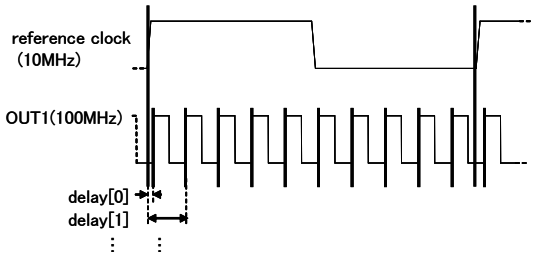

Figure 6: Definition of Measured Delay.

pear at OUT1. We thus obtain ten delay values (delay[0], delay[1], ..., in Fig6) for each reference clock. To evaluate the delay increase due to I/O power supply noise, we here define delay D as the average of these ten delays ($D = \frac{1}{10}\sum_{i=0}^{10}\mathrm{delay}[i]$).

We also define noise magnitude V_{mag} as follows,

$$V_{mag} = \frac{1}{t1 - t0}\int_{t0}^{t1} V_{noise}(t) - V_{ideal}dt,$$

where time interval from $t0$ to $t1$ is the time interval of interest, $V_{noise}(t)$ is the measured noise voltage, and V_{ideal} is the ideal voltage given to the PCB board. V_{mag} means the average difference between $V_{noise}(t)$ and V_{ideal}.

Fig. 8 shows the relation between delay D and noise magnitude V_{mag} in case that both active and passive probes are attached to OUT1. Here, VDDIO-VSSIO is used as V_{noise}, and the time interval $t0$ to $t1$ basically corresponds to one cycle of PLL output, though a small time interval within a cycle, in which the noise measurement macros were not able to sense VDDIO and VSSIO, was excluded. We can see that as the number of active output buffers increases, V_{mag} becomes larger,

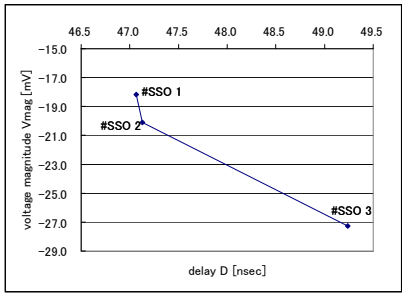

Figure 7: Relation between delay D and noise magnitude V_{mag} (w/ passive probe).

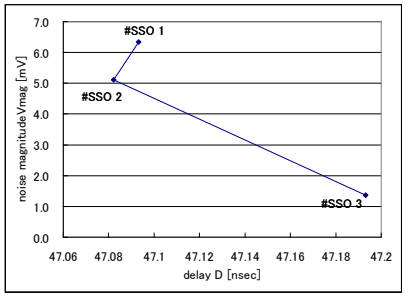

Figure 8: Relation between delay D and noise magnitude V_{mag} (w/o passive probe).

which results in increase of D. Fig. 8 indicates the similar tendency, though the delay variation is quite small. The on-chip I/O power supply noise affects the output transition timing, and hence careful consideration and estimation of I/O power supply noise as well as core power supply noise, especially when the number of pads for IO power supply is reduced, is necessary for sustaining reliable chip-to-chip communication.

Conclusions

This paper presented on-chip I/O power supply noises measured by the noise measurement macros. The measured noises are consistent with intuitive understanding of SSO noise, that is, the noise amplitude becomes larger as the number of SSO increases. We also verified the correlation between noise magnitude and delay and found that the delay increase due to SSO can be reasonably explained with the noise magnitude of I/O power supply noise.

Acknowledgment

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References

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