# A 16-bit RISC Processor with 4.18pJ/cycle at 0.5V Operation

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## I. Introduction

Subthreshold processors, which operate at below MOSFET threshold voltage, are drawing attention for ultra low power applications, such as sensor nodes. Subthreshold circuits have remarkable characteristics of slow yet ultra low power operation, and most of power is consumed by leakage current [1]. To reduce leakage current, smaller area is desirable, but it degrades processor performance. Excessive simplification of processor architecture results in increase in energy required for application execution due to larger execution cycles [2]. Therefore, energy- and application-aware architecture design is indispensable. We evaluated several processor architectures by simulation with three applications for sensor nodes. We then fabricated a 16-bit RISC processor in 65nm process, and measured the power and energy consumption.

## II. Processor Architecture Evaluation

We designed eight RISC processor architectures with a 17-bit instruction set, having different number of pipeline stages (3 or 5) and datapath width (16 or 32bit) and number (8 or 16) of general registers. Twenty basic instructions required for a sensor-node processor are implemented. We used *ASIP Meister* [3] to generate RTL processor designs. Benchmark programs are SHA1 (Secure Hash Algorithm), TEA (Tiny Encryption Algorithm) and CRC16 (Cyclic Redundancy Check) which are typical applications of sensor nodes. Our gate-level performance evaluation assuming 300mV operation and 65nm process revealed an appropriate architecture terms of total energy consumption including processor and SRAMs. Fig. 1 depicts the derived architecuture that has 3-stage pipeline and 16 general registers whose width is 16bit.

## III. Hardware Measurement

We fabricated the processor and SRAMs (DMEM and IMEM) shown in Fig. 1 in 65nm process, and measured the frequency, power, and energy consumption. 10T SRAMs were newly designed for subthreshold operation [4]. Fig. 2 depicts the chip micrograph. Fig. 3 shows circuit frequency at various supply voltages. As the voltage becomes smaller, the frequency

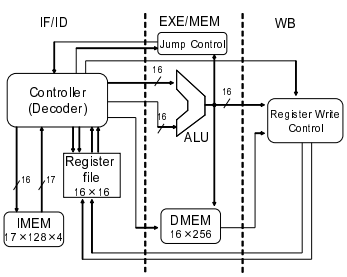


Fig. 1. Result of architecture design.

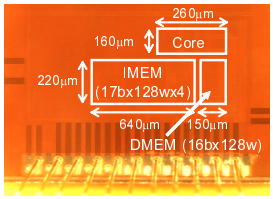


Fig. 2. Chip micrograph.

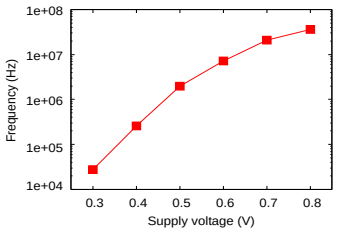


Fig. 3. Frequency vs. voltage.

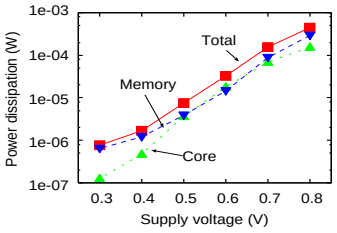


Fig. 4. Power vs. voltage.

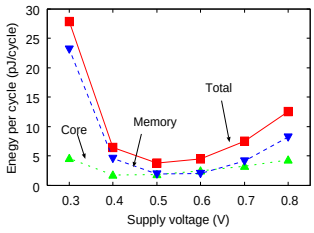


Fig. 5. Energy per cycle vs. voltage.

decreases. When the voltage is 0.8V, the frequency is 35MHz, and it decreases to 27kHz when the voltage is 0.3V. Figs. 4 and 5 show power dissipation and energy consumption per cycle of processor and memory while SHA1 is running. At 0.3V, the total power including processor and SRAMs becomes 0.77 $\mu$W and 1/580 compared that at 0.8V. The power of processor core reaches 1/1200, while that of SRAMs decreases to 1/460. Consequently, the power of SRAMs occupies 83.3 % of the total power at 0.3V. On the other hand, the energy consumption per cycle of the total circuit becomes the minimum at 0.5V, and it is 4.18pJ/cycle at 1.43MHz operation.

## IV. Conclusion

In this paper, we investigated the processor architecture for ultra low voltage operation with gate level evaluation, and selected a 16-bit 3-stage processor with 16 general registers in terms of energy consumption. We fabricated the processor and SRAMs in 65nm process and measured the frequency, power, and energy consumption. The power dissipation at 0.3V is 0.7$\mu$W. The energy consumption for SHA1 execution is minimized at 0.5V. The energy per cycle is 4.18pJ per cycle at 1.43MHz operation.

## References

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