Alpha-Particle-Induced Soft Errors and Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM

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***Abstract*— This paper presents measurement results of alpha-particle-induced soft errors and multiple cell upsets (MCUs) in 65-nm 10T SRAM with a wide range of supply voltage from 1.0 V to 0.3 V. We reveal that the soft error rate (SER) at 0.3 V is eight times higher than SER at 1.0 V, and the ratio of MCUs to the total upsets increases as the supply voltage decreases. The SER and ratio of MCUs with body-biasing are also described. In addition, we investigate an impact of manufacturing variability on the soft error immunity of each memory cell. In our measurement, a distinct influence of manufacturing variability is not observed even in subthreshold region.**

I. Introduction

Subthreshold circuits, which operate at a lower supply voltage than threshold voltage, are expected to be used for ultra-low power applications, such as a sensor-node processor [1], [2]. On the other hand, soft error immunity of subthreshold circuits has become a concern because the ultra-low voltage operation reduces the energy required to cause upsets [3], [4]. Especially, the soft error rate (SER) in SRAM, which often characterize the SER of the entire circuit, must be carefully examined before adopting subthreshold circuits for practical applications.

According to [5], the neutron-induced SER in SRAM increases by 18% for every 10% reduction in the supply voltage. Reference [6] reports a trend that decrease in the supply voltage makes the alpha-particle-induced SER dominant in SRAM. However, these measurements were just performed between the nominal supply voltage and 0.8 V. As for soft errors in subthreshold region, single event transient (SET) was recently analyzed with ring oscillators in [3]. On the other hand, the SRAM SER in subthreshold region has not been measured as far as the authors know.

This paper is the first work to measure the alpha-particle-induced SER in subthreshold region using a newly designed 65-nm 10T SRAM. Measurement results show that 0.3 V operation increases SER eightfold compared to 1.0 V. In addition, information on frequency of multiple cell upsets (MCUs) is important for error prevention using error checking and correction (ECC) technique. In this paper, we also investigate MCUs in subthreshold region. We reveal that although the ratio of MCUs to the total upsets remarkably increases at lower voltage, conventional ECC technique is still effective in our 10T subthreshold SRAM. Additionally, the dependency of SER on body-bias is evaluated, and measurement results indicate that the SER and the ratio of MCUs are less sensitive to the body-bias voltage when the supply voltage is 0.4 V.

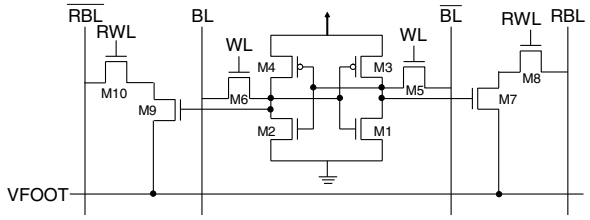


Fig. 1. Structure of the 10T memory cell. WL is only asserted at the write operation and RWL is asserted at the read operation.

Furthermore, we examine the variation in soft error immunity of each memory cell. Reference [7] indicates that the charge required to cause an upset, that is, critical charge varies bit by bit due to manufacturing variability, especially threshold voltage variation, and the variation in critical charge becomes larger as the supply voltage is lowered. In this paper, we investigate the influence of manufacturing variability on the soft error immunity in subthreshold region. Measurement results show that the distribution of the number of SEUs in each memory cell is well explained by the spatial randomness of alpha-particle hits without taking into account critical charge variation due to manufacturing variability.

II. SRAM Structure

In order to measure the SRAM SER over a wide range of supply voltage, SRAM that can operate even in subthreshold region is required. On the other hand, traditional 6T SRAM, which is used in commercial off-the-shelf SRAMs, is scarcely functional in subthreshold region due to weak writability and read instability [8], [9]. Many types of memory cell structure have been proposed to overcome those problems in the low-voltage operation [9]–[13]. One of the potential solutions is to add a few transistors dedicated to a read port [10]. Based on this technique, 10T [9], [11] and 8T [12], [13] SRAMs achieve subthreshold operation.

In this paper, 10T SRAM was newly designed and fabricated. Fig. 1 depicts the structure of designed memory cell. This memory cell is based on the 8T memory cell proposed in [12]. We improved the 8T memory cell such that a differential read operation can be achieved by adding two NMOSs (M9 and M10). VFOOT is used to ensure the correct read operation in subthreshold region [12]. VFOOT of the accessed word is set to low and those of the unaccessed

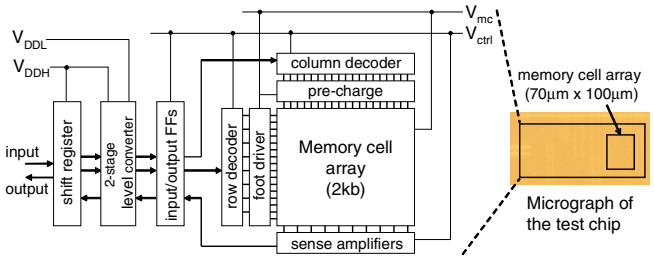


Fig. 2. Block diagram of the SRAM circuit and micrograph of the test chip.

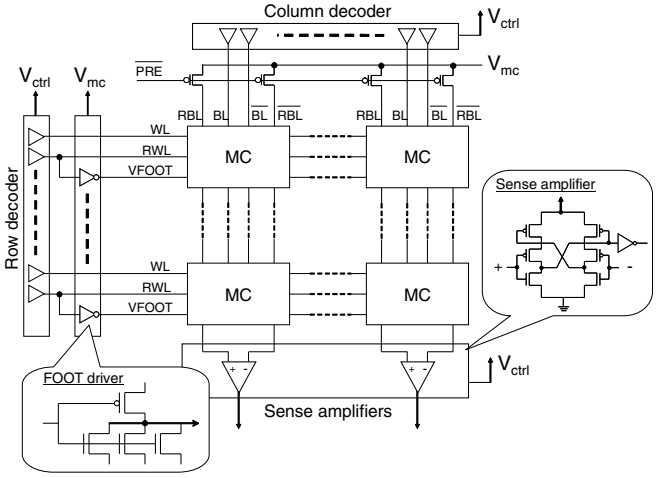


Fig. 3. Details of the memory cell (MC) array and its control logic.

words remain high. The area of 6T (M1–M6) occupies 80% of the total area (10T) because the size of the cross-coupled inverters (M1–M4) was increased to mitigate threshold voltage variability and to retain the correct data in all bits even in subthreshold region.

Fig. 2 shows the block diagram of the SRAM circuit. A test chip was fabricated in a 65-nm CMOS process. 2kb (128 row $\times$ 16 column) cells with triple-well structure are implemented, and are verified to be functional from 1.0 V to 0.3 V. This time, any bit-interleaving technique is not implemented in our design. Fig. 3 illustrates the details of the memory cell array and its control logic. Different supply voltages are applied to the memory cell array and the control circuit which consists of the FFs for input/output data and the row/column decoder. The supply voltage of the control circuit V_{ctrl} is higher than the memory cell voltage V_{mc}. Since the word line (WL) and bit line (BL) drivers operate at V_{ctrl}, strong writability can be achieved, which is similar to so-called "boosted word line" technique [12], [14]. Throughout this paper, V_{ctrl} is set to $V_{mc} + 0.1$ V. Signals at V_{ctrl} are converted to the nominal supply voltage V_{DDH} via V_{DDL} by the 2-stage level shifter. For example, a typical configuration at $V_{ctrl} = 0.4$ V is $V_{DDL} = 0.6$ V and $V_{DDH} = 1.2$ V.

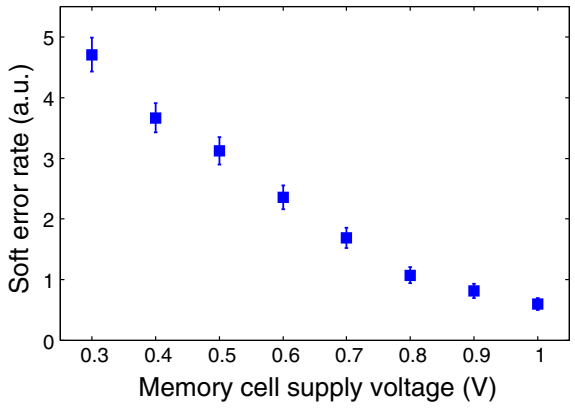


Fig. 4. SERs as a function of the supply voltage of the memory cell array (V_{mc}). Each error bar indicates $\pm 3\sigma$, where σ is defined as the square root of the number of the observed upsets.

III. Experimental Results

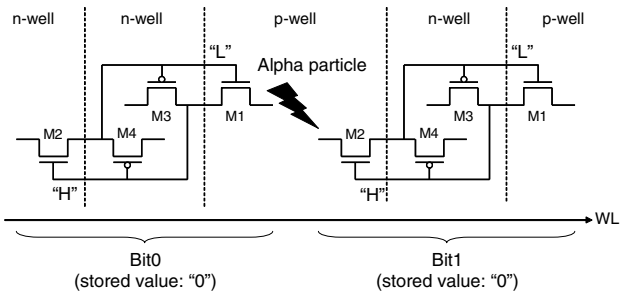
This section describes measurement results. We used an Am-241 foil, whose flux is 9×10^9 cm^{-2}h^{-1}, as an alpha particle source. The main peak energy of the alpha particle is 5.49 MeV. The foil was placed immediately above the die according to [15].

A. Sort Error Rate and Multiple Cell Upset

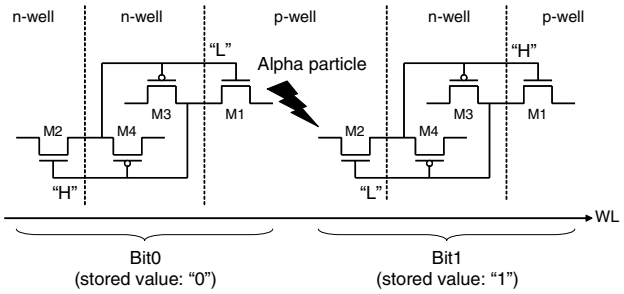
Fig. 4 shows SERs as a function of the supply voltage of the memory cell array (V_{mc}). In this experiment, we first wrote zero to all bits in the SRAM. Then, all stored data was read every 10 seconds, and we checked whether each bit was flipped or not to evaluate the SER. The operation frequency in read operation was 5 kHz. Fig. 4 indicates that the SER increases as the supply voltage is reduced, and the SER at $V_{mc} = 0.3$ V is eight times higher than that at $V_{mc} = 1.0$ V.

Next, we focus on the multiplicity of soft errors. Especially, multiple upsets belonging to the same word are critical, because the conventional SEC-DED (Single Error Correction, Double Error Detection) ECC cannot correct two or more errors in a word. As explained in Fig. 5, the occurrence of multiple upsets in adjacent bits depends on the written data pattern [16]. In our memory cell layout, the intra-word upsets might occur in data pattern "01" and "10". Therefore, we periodically wrote the data pattern "$1010\cdots$" to all words and checked the stored data until around 2000 soft errors were observed. Note that two errors originated from different particles might be misjudged as an MCU in this measurement. We, however, estimated the probability of this misjudgment, and the number of such "pseudo" MCUs was below two in this setup.

Fig. 6 lists the number of single bit upsets (SBUs) and MCUs and plots the ratio of MCUs to the total number of upsets as a function of the memory cell voltage (V_{mc}). All of the observed MCUs were two-bit ones. The ratio of MCUs dramatically increases when V_{mc} becomes less than 0.6 V. Interestingly, on the other hand, multiple upsets belonging to the same word were observed only once in $V_{mc} = 1.0$ V,



(a) intra-word upsets do not occur



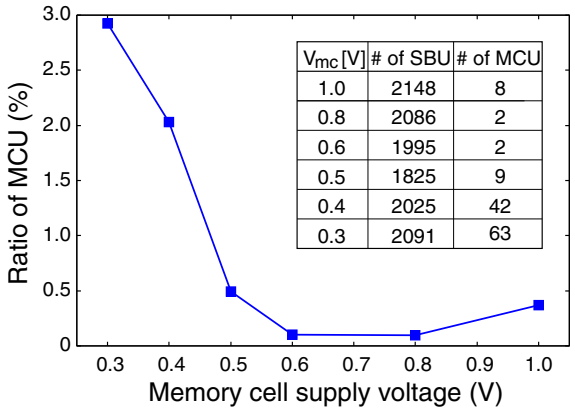
(b) intra-word upsets might occur

Fig. 5. Occurrence of multiple upsets in adjacent bits depends on the written data pattern [16]. Only cross-coupled inverters (M1–4 in Fig. 1) are illustrated in this figure. In our memory cell layout, intra-word upsets might occur in data pattern "01" and "10", and do not occur in "00" and "11".

and all other MCUs occurred in inter-word adjacent bits. This means the conventional ECC technique is still effective for robust operation in subthreshold region.

We here discuss the reason why the MCUs only arose in inter-word adjacent bits in subthreshold operation. Fig. 7 illustrates the layout of the memory cell array. The drains of P/NMOSs in the cross-coupled inverter pair are sensitive to alpha particles. The distance between the sensitive nodes of the adjacent rows is $1/5$ shorter than that of the adjacent columns. In the designed 10T cells, the NMOSs for the read operation (M7–10 in Fig. 1) are located between the adjacent columns, which makes horizontally-adjacent cells distant. Thus, adjacent bits in different words along bit lines are more likely to upset.

Next, we measure the dependence of the SER and MCU on the body-bias voltage of the memory cells at $V_{mc} = 0.4$ V and 1.0 V. Fig. 8 shows the measurement results. When V_{mc} is 1.0 V, the SERs at 1.0 V-RBB (reverse body bias) and at 0.3 V-FBB (forward body bias) increase by more than 30% compared to the SER at ZBB (zero body bias), whereas when V_{mc} is 0.4 V, the SERs at 1.0 V-RBB and 0.3 V-FBB are higher by below 10% than the SER at ZBB. In addition, although FBB raises the ratio of MCUs to the total upsets at $V_{mc} = 1.0$ V, body-bias does not affect the ratio so much at $V_{mc} = 0.4$ V. The SER and the ratio of MCUs are less sensitive to the body-bias at 0.4 V than those at 1.0 V.



V_{mc} [V]	# of SBU	# of MCU
1.0	2148	8
0.8	2086	2
0.6	1995	2
0.5	1825	9
0.4	2025	42
0.3	2091	63

Fig. 6. The number of single bit upsets (SBUs) and multiple cell upsets (MCUs), and the ratio of MCUs to the total upsets (SBU + MCU) as a function of the supply voltage of the memory cell array (V_{mc}).

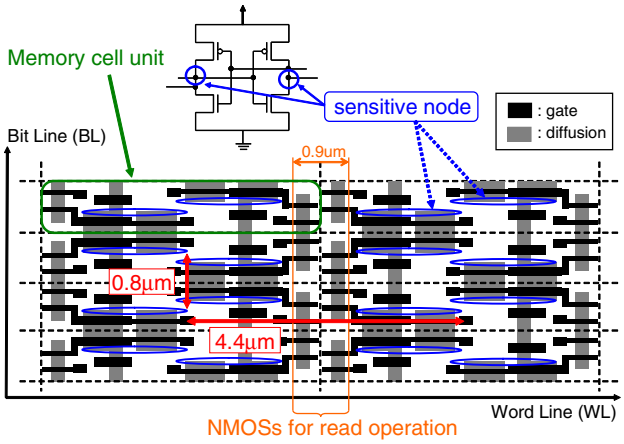


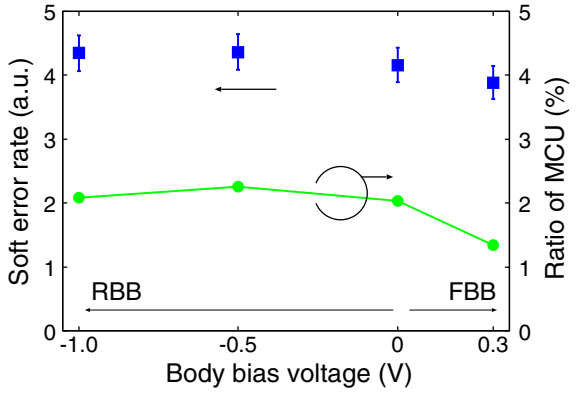
Fig. 7. Layout of the memory cell array. Blue ellipses indicate sensitive nodes for alpha particles. The NMOSs for the read operation (M7–10 in Fig. 1) are located between the adjacent columns.

B. Variation in Soft Error Immunity

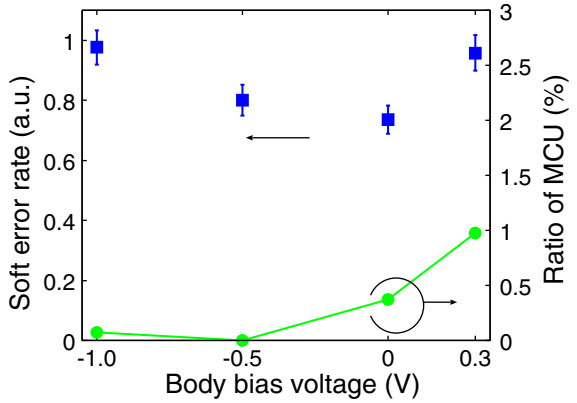
In this section, we investigate the influence of the critical charge variation due to manufacturing variability on the soft error immunity. We measured the number of soft errors in each memory cell for around 16 hours (the total number of errors was 300K) when the memory cell voltage (V_{mc}) is 0.3 V. Fig. 9 shows the distribution of the number of soft errors in each memory cell in a single chip. This figure indicates that the number of errors varies bit by bit.

In order to clarify whether this variation is caused by statistical variation due to the spatial randomness of particle hits or by the critical charge variation, we performed a Monte Carlo simulation with the following procedure:

1) Let P_i be the occurrence probability of errors in the i th memory cell ($0 \leq i \leq 2047$).
2) An integer number n and a real number p are randomly generated. n and p satisfy $0 \leq n \leq 2047$ and $0 \leq p < 1$, respectively.



(a) $V_{mc} = 0.4$ V



(b) $V_{mc} = 1.0$ V

Fig. 8. Dependence of the SER and the ratio of MCUs on the body-bias voltage of the memory cells. "RBB" and "FBB" denote reverse body-bias and forward body-bias, respectively. Each error bar indicates $\pm 3\sigma$.

3) If p is less than P_n ($p < P_n$), we consider that an upset occurs in the n th memory cell.
4) Steps 2) and 3) are repeated until the total number of upsets reaches 300K. Consequently, the number of errors in each memory cell is obtained.

Fig. 10 shows the simulated distribution of the number of errors in each memory cell. Here, we assume that the occurrence probability of errors $P = \{P_0\, P_1 \cdots P_{2047}\}$ is normally distributed with mean μ_P and standard deviation σ_P. In this simulation, μ_P is set to 0.5. Fig. 10-(a) depicts the simulated distribution in the case where σ_P is zero, that is, the occurrence probability of errors in each memory cell is the same. Fig. 10-(b) shows the distribution when σ_P/μ_P is 0.1. The distribution of Fig. 10-(a) is normally distributed, and its standard deviation is equivalent to the square root of the mean ($\sqrt{147.4} = 12.14$). This means that Fig. 10-(a) obeys the Poisson distribution.

If the variation in the number of errors is caused only by the spatial randomness of particle hits, the occurrence probability of errors in each memory cell is the same ($\sigma_P = 0$). In this case, the distribution of the number of errors follows the Poisson distribution as shown in Fig. 10-(a). On the other hand, if the critical charge fluctuation influences the variation

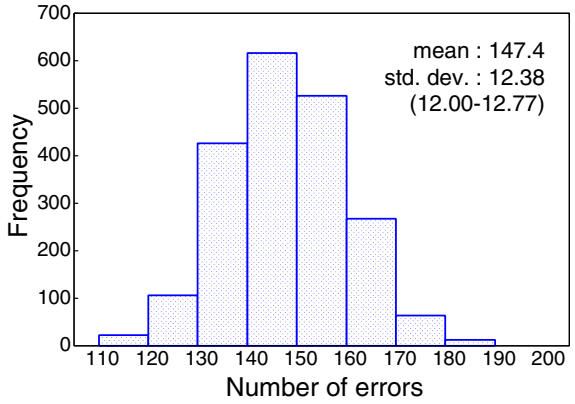


Fig. 9. Measured distribution of the number of soft errors in each memory cell in a single chip ($V_{mc} = 0.3$ V). The total number of errors is 300K. The values in parentheses represent the 95% confidence interval of the standard deviation.

in the number of errors in addition to the spatial randomness of particle hits, the distribution of the number of errors becomes different from the Poisson distribution like Fig. 10-(b).

The distribution of Fig. 9 is normally distributed, and its standard deviation is close to that of Fig. 10-(a). This implies that the both distributions are almost identical and follow the Poisson distribution. This means that the variation shown in Fig. 9 is explained by the spatial randomness of particle hits, and the influence of the critical charge variation was not distinguishably observed even at $V_{mc} = 0.3$ V.

IV. Conclusion

In this paper, we presented alpha-particle-induced SERs and MCUs in subthreshold region of a designed 10T SRAM in a 65-nm CMOS process. The measurement results showed that the SER increases as the supply voltage is lowered and SER at 0.3 V is eight times higher than SER at 1.0 V. We also pointed out that the ratios of MCUs to the total upsets in subthreshold region are much higher than those in super-threshold (nominal supply voltage) region, yet the conventional ECC is still valid because intra-word multiple upsets were not observed in subthreshold region. We additionally revealed that the SER and the ratio of MCU are less sensitive to body-bias at 0.4 V supply voltage. Furthermore, we investigated the influence of the critical charge variation due to manufacturing variability on the soft error immunity in each memory cell. Measurement results indicated that the influence of the critical charge variation was not recognizably observed even in subthreshold region.

Acknowledgments

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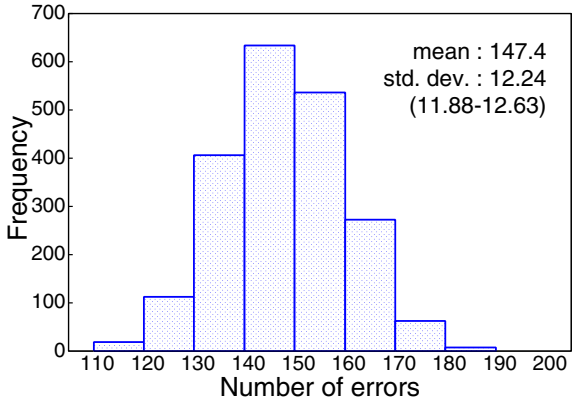
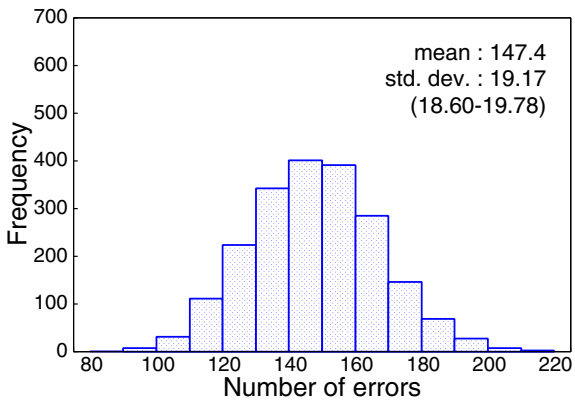


(a) $\sigma_P = 0$ (the occurrence probability of errors in each memory cell is the same)



(b) $\sigma_P \,/\, \mu_P = 0.1$

Fig. 10. Simulated distribution of the number of errors in each memory cell. The total number of errors is 300K. The values in parentheses represent the 95% confidence interval of the standard deviation. The simulation assumes that the occurrence probability of errors is normally distributed with mean μ_P and standard deviation σ_P ($P \sim N(\mu_p, \sigma_P^2)$).

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