PAPER

A Performance Prediction of Clock Generation PLLs: A Ring Oscillator Based PLL and an LC Oscillator Based PLL

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SUMMARY This paper discusses performance prediction of clock generation PLLs using a ring oscillator based VCO (RingVCO) and an LC oscillator based VCO (LCVCO). For clock generation, we generally design PLLs using RingVCOs because of their superiority in tunable frequency range, chip area and power consumption, in spite of their poor noise characteristics. In the future, it is predicted that operating frequency will rapidly increase and supply voltage will dramatically decrease. Besides, rigid noise performances will be required. In this condition, it is not clear neither how performances of both PLLs will change nor the performance differences between both PLLs will change. This paper predicts and compares future performances of PLLs using a RingVCO and an LCVCO with a qualitative evaluation by an analytical approach and with design experiments based on predicted process parameters. Our discussion reveals that the relative performance difference between both PLLs will be unchanged. As technology advances, power dissipation and chip area of both PLLs favorably decrease, while, noise characteristics of both PLLs degrade, which indicates low noise PLL circuit design will be more important.

key words: *clock generation PLL, LC oscillator, ring oscillator, performance prediction, jitter, power consumption, chip area*

1. Introduction

Phase-Locked Loops (PLLs) are widely used for clock generation in high-speed digital systems. Voltage-Controlled Oscillator (VCO) is a key component of PLLs and we have two choices: a voltage-controlled ring oscillator (RingVCO) and a voltage-controlled LC oscillator (LCVCO). A RingVCO has been considered to be a better choice, because of its lower power consumption, smaller chip area and wider tunable frequency range. Recent increase in clock speed and the latest multi-GHz serial link circuits, however, require rigid jitter performance. It is getting harder to satisfy the design requirements using a simple RingVCO. In contrast, an LCVCO is superior to a RingVCO in terms of noise characteristics such as phase noise and jitter [1].

In the future, ITRS roadmap [2] predicts that technology node is aggressively scaled down, and supply voltage V_{DD} will decrease in proportional to the technology node and operational frequency f_0 will increase inversely proportional to the technology node as shown in Table 1. PLLs for clock generation are usually integrated with digital circuits, and hence PLLs must be designed in the same digital CMOS process. Generally, it does not provide an additionally deposited thick metal to achieve a high Q spiral inductor, a high poly resistor, an MIM capacitor and so on. In this condition, it is unclear which type of PLL will be better in the future.

Table 1 Technology scaling.

Year	1999	2002	2005	2008	2011
Tech. Node [nm]	180	130	100	70	50
V_{DD} [V]	1.8	1.2	0.9	0.6	0.5
f_0 [GHz]	1.6	2.1	3.5	6.0	10
Effective T_{ox} [nm]	4.8	1.7	1.25	1.0	0.7

In this work we predict future performances of clock generation PLLs using a RingVCO and an LCVCO. Section 2 predicts major performances of PLLs such as jitter, power consumption and chip area, based on a qualitative evaluation in an analytic way. We project the future technology scaling into the analytic formulas of PLL performances proposed so far, and we reveal and compare the performance trend both of RingVCO and LCVCO. The qualitative discussion in Sect. 2 is ascertained by design experiments in Sect. 3. Finally, Sect. 4 concludes our discussion.

2. Performance Prediction in the Future

In this section, we predict major performances of PLLs; jitter, power consumption and chip area.

2.1 Evaluation Conditions

The PLL architecture under our study is shown in Fig. 1 [3]. It is composed of five major blocks: a phase-frequency detector (PFD), a charge pump (CP), a second order loop filter, a voltage-controlled oscillator (VCO) and a divider. To reduce noise of VCO control voltage, C_2, which is tenth of C_1, is added to the loop filter [3]. All the components including the loop filter and the output buffer are integrated.

The RingVCO and LCVCO under our study are shown in Fig. 2 and Fig. 3 respectively. The RingVCO is five-stage differential inverters. The LCVCO is an NMOS cross-coupled differential oscillator composed of two square-shaped spiral inductors and a differential diode varactor. In actual products, calibration circuits are added to standard PLLs. In this work, however, we study the standard PLLs without calibration circuits in order to evaluate inherent characteristics of fundamental PLL circuits.

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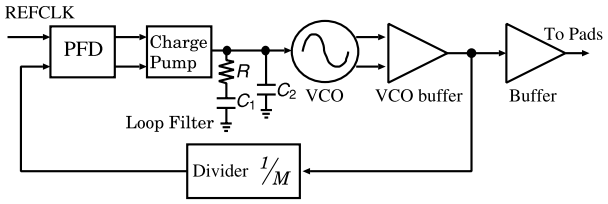

Fig. 1 PLL architecture under our study.

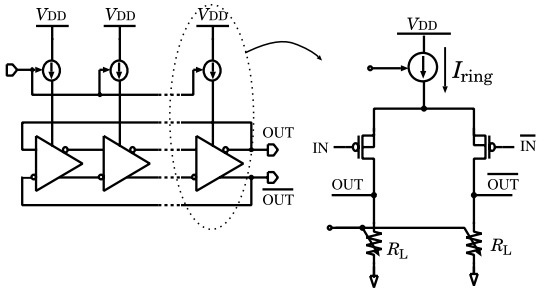

Fig. 2 Ring oscillator (RingVCO) circuit.

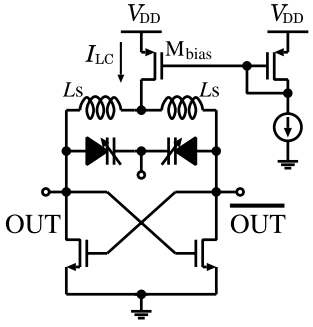

Fig. 3 LC oscillator (LCVCO) circuit.

The highest frequency at each technology node, which ITRS roadmap [2] predicts, is defined as operating frequency f_0 of PLL circuits (Table 1). We use the minimum channel length of the device at every technology node. The number of inverter stage in RingVCO is unchanged. Oscillation voltage amplitude is kept 1/4 of V_{DD}. In the near future it is predicted that we may use copper metals instead of aluminum and the Q value of spiral inductor may increase. In this paper, however, we assume the Q value is constant in every technology node conservatively. When we decide gate width W, we have several choices. For example, W/L ratio is constant or W is kept unchanged. In this paper, we adopt the former choice that W/L is constant, because it is common in digital circuit design.

2.2 Jitter Prediction

The period jitter J of oscillator is the standard deviation of the variation in a cycle time. We evaluate period jitter J, since J is a primary metric of noise characteristics for clock generation PLLs. Period jitter J is hereafter called jitter for short in this paper.

In this work, we focus on inherent and unavoidable jitter sources inside PLL circuits, and the jitter due to environmental factors, such as supply voltage fluctuation, is not discussed. The type of jitter caused in PLL circuits can be classified into two groups; (1) a synchronous jitter generated in PFD, CP and divider, and (2) an accumulating jitter caused by VCO and REFCLK. When a PLL has an optimal closed-loop bandwidth, the former synchronous jitter is eliminated and the jitter that comes from the VCO dominates. The accumulating jitter of a PLL becomes equal to that of its VCO [4]. We hence evaluate the jitter of VCOs in the following sections.

2.2.1 Jitter and Phase Noise

Period jitter J is computed from phase noise $L(\Delta f)$ as follows [4].

$$J = \sqrt{cT_0}, \qquad c = L(\Delta f) \cdot \frac{\Delta f^2}{f_0^2}, \tag{1}$$

where f_0 is the oscillation frequency, $T_0 (= 1/f_0)$ is the oscillation period, and Δf is the offset frequency from the oscillation frequency. Equation (1) is valid when Δf is above the Lorentzian function corner frequency (f_c) [5], in other words, when we choose Δf from the region where white noise dominates and $1/f$ noise is not significant. Reference [4] indicates that Eq. (1) with this selection of Δf is suitable and reasonable to evaluate period jitter J.

Using Eq. (1), the ratio of jitter and oscillation period, J/T_0, can be expressed as

$$\frac{J}{T_0} = \sqrt{f_0 \cdot L(\Delta f) \cdot \frac{\Delta f^2}{f_0^2}}. \tag{2}$$

We discuss the trend of J/T_0 instead of J, because jitter should be reduced as T_0 decreases. Therefore in following sections, we predict J/T_0 of RingVCO and LCVCO.

2.2.2 RingVCO Jitter Prediction

The differential ring oscillator shown in Fig. 2 is evaluated. In RingVCO, thermal noises of MOS transistors and resistors are white noise sources, and are considered in jitter evaluation. Phase noise of RingVCO ($L_{ring}(\Delta f)$) is expressed as [1]

$$L_{ring}(\Delta f) = \frac{8N}{3\eta} \cdot \frac{kT}{P_{ring}} \cdot \left(\frac{V_{DD}}{V_{char}} + \frac{V_{DD}}{R_L I_{ring}} \right) \cdot \frac{f_0^2}{\Delta f^2}, \tag{3}$$

where N is the number of inverter stage, P_{ring} is the power consumption of the ring oscillator, V_{DD} is the supply voltage, I_{ring} is the tail current of each inverter and R_L is the load resistance. η is a constant that represents the proportional relation between rise time and delay time of inverters, k is the Boltzmann constant and T is the temperature. V_{char} is the characteristic voltage of the device, and is defined as $V_{char} = E_c L/\gamma$, where L is the channel length of the device.

E_c is the critical electric field, which is defined as the value of electric field resulting in half the carrier velocity expected from low field mobility. Short-channel devices are considered in these expressions. The parameter γ is the coefficient, which is 2/3 for long-channel devices in the saturation region and typically two to three times larger for short-channel devices [6].

Using Eq. (2) and Eq. (3), J_{ring}/T_0 of RingVCO can be expressed as

$$\frac{J_{ring}}{T_0} = \sqrt{\frac{8N}{3\eta}\cdot\frac{kT}{P_{ring}}\cdot\left(\frac{V_{DD}}{V_{char}}+\frac{V_{DD}}{R_L I_{ring}}\right)\cdot f_0}. \tag{4}$$

In our evaluation, N, η, k, T, E_c and γ are constant in every technology node. L and V_{DD} have a proportional relation roughly, as ITRS predicts. Therefore, V_{DD}/V_{char} is constant. $V_{DD}/R_L I_{ring}$ is also constant, since $R_L I_{ring}$ expresses oscillation amplitude. We can find f_0 and L in ITRS roadmap. The unknown parameter left is P_{ring}. We evaluate the trend of P_{ring}. P_{ring} is expressed as $P_{ring} = N \cdot I_{ring} \cdot V_{DD}$. VCO operating frequency f_0 can be expressed as [1]

$$f_0 = \frac{1}{2Nt_D} \approx \frac{I_{ring}}{2\eta N q_{max}}, \tag{5}$$

where t_D is the delay of an inverter and q_{max} is the charge stored in each node during a cycle. In this case, η and N are fixed, so I_{ring} can be expressed as

$$I_{ring} \propto f_0 \cdot q_{max}. \tag{6}$$

I_{ring} is proportional to the product of f_0 and q_{max}.

Here, let us examine the trend of q_{max}. q_{max} is expected to be proportional to the technology node. The reason is shown below. When W/L is constant, the channel width W decreases in proportion to the technology node. ITRS roadmap forecasts that on-current per unit gate width is unchanged, and then the current is proportional to W. q_{max} is proportional to the current, because the current is proportional to the charge stored in the channel with a first order approximation. Consequently, q_{max} is proportional to the technology node.

f_0 is predicted to be roughly in inverse proportion to the technology node [2]. The decrease of q_{max} cancels out the increase of f_0, and hence I_{ring} is predicted to be almost constant. Therefore, P_{ring} decreases in proportion to V_{DD}, since N is fixed.

Consequently, J_{ring}/T_0 can be expressed as

$$\frac{J_{ring}}{T_0} \propto \sqrt{\frac{f_0}{V_{DD}}}. \tag{7}$$

It is in proportion to the square root of f_0/V_{DD}, which is similarly proportional to the technology node, since the decrease of V_{DD} and the increase of f_0 are predicted to be roughly proportional to the technology node.

2.2.3 LCVCO Jitter Prediction

The differential LC oscillator shown in Fig. 3 is evaluated. In LCVCO, resonator noise, differential pair noise and tail current noise are white noise, and the sum of these noises are considered in the following phase noise expression of LCVCO($L_{LC}(\Delta f)$) [7]

$$L_{LC}(\Delta f) = \frac{FkTr_{eq}}{V_{osc}^2 Q_T^2}\cdot\frac{f_0^2}{\Delta f^2}, \tag{8}$$

where V_{osc} is the oscillation amplitude, Q_T is the quality factor of the LC resonator and r_{eq} is the loss ingredient of the LC resonator. F is the differential oscillator Leeson's noise factor, and is expressed as

$$F = 2 + \frac{8\gamma r_{eq} I_{LC}}{\pi V_{osc}} + \frac{8}{9}\gamma r_{eq} g_{mbias}, \tag{9}$$

where I_{LC} is the tail current of the oscillator and g_{mbias} is the transconductance of transistor M_{bias}.

Using Eq. (2) and Eq. (8), J_{LC}/T_0 of LCVCO can be expressed as

$$\frac{J_{LC}}{T_0} = \sqrt{\frac{FkTr_{eq}}{V_{osc}^2 Q_T^2}\cdot f_0}. \tag{10}$$

When V_{osc} is smaller than V_{DD}, V_{osc} is proportional to I_{LC} [1]. Therefore as far as V_{osc} is not clamped, F is almost constant in every technology node, assuming $r_{eq} g_{mbias}$ is held constant. This condition is satisfied in our analysis. Because we assume V_{osc}/V_{DD} is fixed in every technology node. k and T are also constant. The factors to be examined are r_{eq} and Q_T.

The inductance value of the spiral inductor is L_s and the total capacitance of the LC resonator is C_{total}. The quality factor of the LC resonator Q_T is expressed as $Q_T = r_{eq}/Z_0$, where Z_0 is the characteristics impedance and is expressed as $\sqrt{L_s/C_{total}}$. f_0 is expressed as $1/(2\pi\sqrt{L_s C_{total}})$. Therefore r_{eq} is expressed as $r_{eq} = 2\pi f_0 Q_T L_s$.

Q_T is expressed using the quality factors of the spiral inductor and the capacitor (Q_L and Q_C) as [8]

$$Q_T = \frac{Q_L Q_C}{Q_L + Q_C} = \frac{Q_L}{1 + Q_L/Q_C}. \tag{11}$$

In normal CMOS processes, Q_C of varactor is more than 50, while Q_L of spiral is less than 5. Equation (11) can be approximated as $Q_T \simeq Q_L$. Since Q_L is assumed to be unchanged, Q_T is also constant in every technology node.

Consequently, Eq. (10) can be expressed as $J_{LC}/T_0 \propto \sqrt{f_0^2 L_s/V_{DD}^2}$. When we design LCVCO, we have several ways to decide L_s; keeping $f_0 L_s/V_{DD}$ unchanged or keeping $f_0 L_s$ unchanged, for example. We choose the former way, i.e. we design LCVCO with $f_0 L_s/V_{DD}$ unchanged in our analysis, because the former way provides better jitter characteristic, which will be discussed in Appendix. In this case, J_{LC}/T_0 can be expressed as

$$\frac{J_{LC}}{T_0} \propto \sqrt{\frac{f_0}{V_{DD}}}. \tag{12}$$

Jitter of LCVCO is proportional to the square root of f_0/V_{DD}, which is the same relation with that of RingVCO (Eq. (7)).

2.3 Power Dissipation Prediction

This section evaluates power dissipation of RingVCO (P_{ring}) and LCVCO (P_{LC}) instead of that of RingPLL and LCPLL, because most of power dissipation of PLL comes from that of VCO. As explained in Sect. 2.2.2, P_{ring} is proportional to V_{DD},

$$P_{\mathrm{ring}} \propto V_{\mathrm{DD}}. \tag{13}$$

We here examine P_{LC}. P_{LC} is expressed as $P_{\mathrm{LC}} = I_{\mathrm{LC}} \cdot V_{\mathrm{DD}}$ [1]. Let us evaluate I_{LC}. The oscillation voltage amplitude V_{osc} is expressed using the current at $\omega_0(=2\pi f_0)$, $I_{\omega 0}$, as follows.

$$\begin{aligned} V_{\mathrm{osc}} &= I_{\omega 0} \cdot r_{\mathrm{eq}}, \\ &\simeq I_{\omega 0} \cdot Q_{\mathrm{L}} \omega_0 L_{\mathrm{s}}, \qquad (14) \\ &\propto I_{\mathrm{LC}} \cdot Q_{\mathrm{L}} \omega_0 L_{\mathrm{s}}. \qquad (15) \end{aligned}$$

In a resonator, $I_{\omega 0}$ is proportional to I_{LC}, and this relation is used between Eq. (14) and Eq. (15). Using Eq. (15), I_{LC} can be expressed as

$$I_{\mathrm{LC}} \propto \frac{V_{\mathrm{osc}}}{Q_{\mathrm{L}} f_0 L_{\mathrm{s}}}. \tag{16}$$

We set $V_{\mathrm{DD}}/V_{\mathrm{osc}}$ and Q_{L} constant, as described in Sect. 2.1. We also design LCVCO with $f_0 L_{\mathrm{s}}/V_{\mathrm{DD}}$ unchanged for jitter characteristics as explained in Sect. 2.2.3. Therefore I_{LC} becomes constant at every technology node. Summarizing the above discussion, P_{LC} decreases in proportion to V_{DD},

$$P_{\mathrm{LC}} \propto V_{\mathrm{DD}}, \tag{17}$$

which is the same relation with that of P_{ring}.

2.4 Area Prediction

We next evaluate the PLL circuit area including the loop filter. We first discuss RingPLL. When we separate a RingPLL into a loop filter and other parts, the area of other parts decreases according to the technology node. In digital CMOS processes, where MIM capacitors are not available, a loop filter consists of MOS gate capacitor and poly or diffusion resistor. MOS gate capacitor occupies a large portion of loop filter area and the capacitance of the loop filter C_1 is tenfold of C_2 in Fig. 1, and hence we must discuss C_1. C_1 is expressed as [3]

$$C_1 = \frac{2\pi I_{\mathrm{ch}} K_{\mathrm{v}}}{{\omega_{\mathrm{n}}}^2 M}, \tag{18}$$

where I_{ch} is the current of the charge pump, K_{v}[Hz/V] is the frequency sensitivity of VCO, M is the division ratio of PLL and ω_{n} is the natural angle frequency of second order PLL. ω_{n} is a design parameter determined by the input reference frequency [3]. And hence when the input reference frequency is unchanged while the oscillation frequency increases, ω_{n} is constant. M increases in proportion to PLL operating frequency f_0. K_{v} is a coefficient of (tunable frequency range)/(control voltage range). When the ratio of variable frequency range and operating frequency is almost fixed, variable frequency range increases in proportion to the operating frequency. The control voltage range is proportional to V_{DD}. Therefore K_{v} is proportional to f_0/V_{DD}. When we suppose that I_{ch} decreases according to V_{DD}, C_1 becomes constant as follows.

$$C_1 \propto \frac{I_{\mathrm{ch}} K_{\mathrm{v}}}{M} \propto \frac{V_{\mathrm{DD}} \cdot f_0}{f_0 \cdot V_{\mathrm{DD}}} = \text{constant}. \tag{19}$$

Consequently, the area of loop filter is reduced in proportion to T_{ox}. The area of RingPLL is reduced according to technology advance, since the area of other parts also decreases according to the technology node.

We next discuss LCPLL. LCPLL is composed of the spiral inductor part and the other part. The latter will be reduced according to the technology node, since it depends on the transistor and interconnect area. In general, the area of spiral inductor is considered to be very large. However, with increase of an operational frequency, the required inductance value decreases and the spiral area also becomes small. The technology node and the operational frequency have a proportional relation, so spiral area decreases similarly proportional to the technology node, which will be experimentally shown in Sect. 3. As a result, the area of LCPLL also decreases according to technology advance.

3. Design Experiments

This section shows the results of design experiments. The design experiments aim to confirm the validity of our qualitative predictions. We evaluate the major performances of PLLs; jitter, power consumption and chip area, comparing our prediction results in Sect. 2 and the simulation results of the PLLs designed for predicted future processes.

Ideally, we had better confirm the validity of our predictions by chip fabrications at each technology node, but in practice, fabrications with future processes are impossible. Therefore, we design RingVCOs and LCVCOs at transistor level with the future processes, with scaling down the device parameters of the base PLLs fabricated in a $0.18\,\mu$m CMOS process, and evaluate power consumption and jitter characteristics using the circuit simulator [9]. The area of PLLs is evaluated with scaling down the area of base PLLs, according to the technology node, T_{ox} and spiral inductor. We retarget and scale the layout of the fabricated PLLs in $0.18\,\mu$m technology according in proportion to the technology node, and calculate layout and parasitic parameters, such as diffusion length, transistor size, parasitic capacitance and so on, in order to improve the reliability of the design experiments. These simulation results are the most effective at the present stage to evaluate the PLL performances at each technology node.

This section consists of two themes; chip fabrication results of the base PLL circuit with a current process and simulation results with future processes. The chip fabrica-

tion is performed to confirm that the PLL circuits discussed in this paper work, and evaluate the performance difference in the current technology. These PLL circuits are called the base circuits and future circuits are designed scaling down these base circuits. The simulation with future processes contributes to verify the validity of our qualitative predictions in Sect. 2.

3.1 Chip Fabrication with a Current Process

The base PLL circuits with a current process are evaluated. We designed, fabricated and measured two clock generation PLLs, RingPLL and LCPLL, in Fig. 1 in a 0.18 μm digital CMOS process.

The number of inverter stages in RingVCO is set to 5, and the oscillation amplitude of both VCOs is controlled to be about 400 mV. The VCO buffer consists of a differential to single-ended converter and a low-to-full swing amplifier. The output buffer is a PMOS common source buffer terminated in 50 Ω. Loop filter shown in Fig. 1 is composed of two NMOS gate capacitors and a silicided poly resistor, and we design C_1=80 pF, C_2=8 pF and R=6 kΩ. Supply voltage is set to 1.8 V, the operational frequency is 1.6 GHz and PLL reference frequency is 25 MHz.

Figure 4 shows the output spectrums of two 1.6 GHz PLLs. We can see that LCPLL spectrum is much sharper. Die photographs of two PLLs with the same scale ratio are also shown in Fig. 4. Table 2 lists the measured performances of two fabricated PLLs. In comparison with the LCPLL, the RingPLL has a tenfold tunable frequency range, a 1/4 core chip area and a 1/2 power consumption. In the noise characteristics, however, the LCPLL has better performances. Jitter is reduced to 1/3, and phase noise at 1 MHz offset decreases by 50 dB/Hz compared with the RingPLL.

These fabrication results show that the circuits designed and simulated in the following section work actually with the current process. In the next section, we design future PLL circuits, scaling down these base circuits.

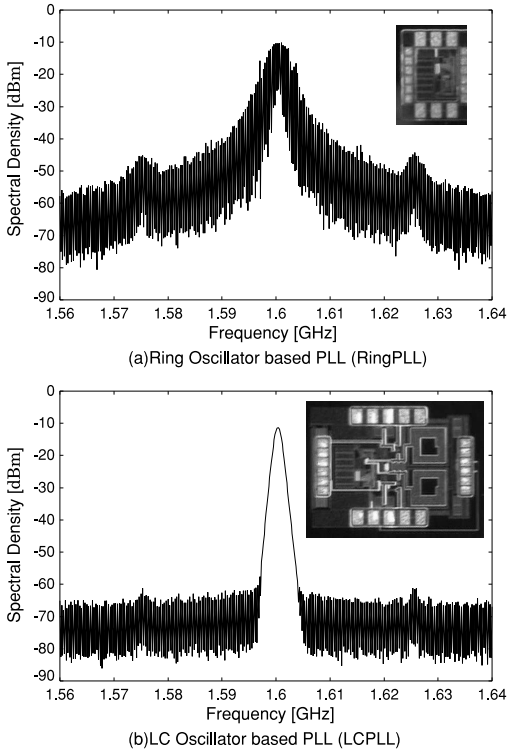

Fig. 4 Output spectrums of two 1.6 GHz PLLs and die photographs of two PLLs with the same scale ratio.

3.2 Simulation with Future Processes

The future PLL circuits are evaluated. We redesign and simulate RingVCO and LCVCO assuming the future processes and evaluate jitter characteristic of VCOs, power consumption of VCOs and chip area of the whole PLLs. These evaluations are performed to verify the validity of our qualitative predictions in Sect. 2 by retargetting the actual circuits for future processes.

We design circuits in the future at transistor level using the transistor model [10] based on the ITRS roadmap [2]. Our experiments use V_{DD}, T_{ox} and f_0 in Table 1. Spiral inductors shown in Table 3 come from our TEG measurement in a 0.18 μm CMOS process. The self-resonant frequency is greater than the operating frequency at each technology node. The series channel resistances of varactor diode are assumed to decrease in proportion to the technology node.

In RingVCO shown in Fig. 2, the PMOS device size is set to $W/L = 70$. In LCVCO shown in Fig. 3, the device size of the cross-coupled NMOS is set to $W/L = 500$ and we add output buffer in the case of analysis. The parameters such as diffusion length, transistor size, parasitic capacitance and so on are settled by scaling of the current device in Sect. 3.1 in proportion to the technology node. To adjust oscillation frequency and voltage amplitude, we tune tail current and load resistance in RingVCO, and tail current and varactor values in LCVCO.

Firstly, we compare the jitter degradation characteristics between our prediction results and simulation results in the future processes. The results are shown in Fig. 5. Figure 5 shows how much jitter characteristics (jitter/period) at each technology node get worse if the jitter characteris-

Table 2 The measured performances of PLLs (out frequency=1.6 GHz).

	RingPLL	LCPLL
Technology	0.18 μm digital CMOS, 5LM, 1.8 V	
Frequency Range	400 MHz–1.8 GHz	1.49–1.64 GHz
Power Dissipation	10.4 mW	22.1 mW
PkPk/RMS jitter	91 ps/15.9 ps	29 ps/3.6 ps
Phase Noise@1 MHz	−65 dBc/Hz	−113 dBc/Hz
Core Chip Area	0.07 mm^2	0.26 mm^2

Table 3 Spiral inductor characteristics from our TEG measurement.

f_0 [GHz]	1.6	2.1	3.5	6	10
Spiral Value [H]	3.2n	1.6n	730p	284p	142p
Spiral Area [mm^2]	0.135	0.072	0.066	0.042	0.018
Q of Spiral	2.7	2.3	2.9	2.6	2.6

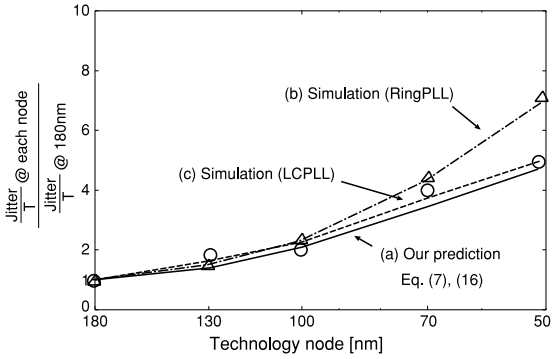

Fig. 5 Jitter characteristic degradation; (a) our prediction results of both PLLs, (b) simulation results of a RingVCO and (c) simulation results of an LCVCO.

tic at technology node 180 nm is set to 1. Our prediction result comes from Eq. (7), Eq. (12) and Table 1. The simulation results are derived in the following way. We simulate phase noise of VCOs, considering only white noise, with circuit simulator [9] and convert it to jitter characteristic by Eq. (2). Since white noise is dominant as a cause of jitter [4], these simulation conditions are effective enough. The simulation results agree with our prediction. Jitter of both PLLs degrades inversely proportional to technology advance, and the relative performance difference between RingPLL and LCPLL are almost constant.

We also discuss the reason why the simulation result of RingPLL in 50 nm technology node is different from the prediction. Table 1 indicates that the reduction ratio of supply voltage from 70 nm to 50 nm is smaller than before. Our prediction assumes that supply voltage is scaled down in proportional to technology node, and hence this assumption is not exact in 50 nm technology. The prediction of RingVCO assumes that $V_{\mathrm{char}}/V_{\mathrm{DD}}$ in Eq. (4), which is proportional to V_{DD}/(gate length), is constant. In the actual simulation, however, when the process moves to 50 nm, $V_{\mathrm{DD}}/V_{\mathrm{char}}$ becomes larger than 1 due to smaller reduction ratio of supply voltage, which results in larger jitter compared with the approximate expression. On the other hand, the jitter prediction of LCVCO does not assume that V_{DD}/(gate length) is constant. Therefore the prediction result is close to the simulation result.

Next, power consumption and chip area are evaluated. Figure 6 shows the relation between technology node and (a) power consumption (b) core chip area. We simulate the VCOs and evaluate power consumption of them. We predict the area of PLLs with scaling down the PLLs fabricated in Sect. 3.1, according to the technology node, T_{ox} and spiral inductor. The simulation results are well in agreement with our prediction discussed in Sect. 2. Power and area of both PLLs decrease proportional to the technology node. The power ratio and the area ratio of both PLLs are roughly unchanged.

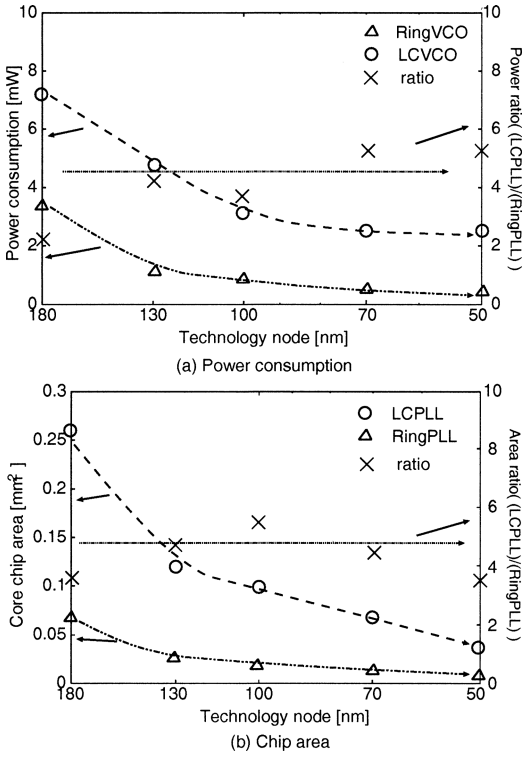

Fig. 6 Simulation results of (a) power consumption of VCOs and (b) chip area of PLLs. Power consumption and area area of both PLLs decrease proportional to the technology node. The power ratio and the area ratio of both PLLs are roughly unchanged.

3.3 Discussion

In the design experiments, all the redesigned circuits work at every technology node, which clarifies that the assumed redesigning policy of the base PLL circuits is feasible and practical. The performances estimated in the design experiments are in good agreement with our qualitative prediction discussed in Sect. 2, and hence we conclude that our qualitative prediction is rightful. Our prediction with the retargeting policy explained in Sect. 2.1 reveals that in the future power dissipation and chip area will decrease, while, jitter characteristics will get worse, as technology advances.

The performance prediction depends on the retargeting policy. One of other scenarios for LCVCO is shown in Appendix. Another scenario is to put more current into VCO so as not to worsen jitter. We finally discuss this scenario briefly.

The jitter improvement of LCVCO gets saturated and starts to degrade as the current increases, because the oscillation voltage amplitude is saturated and the current increase makes thermal noise severe. As long as the voltage amplitude increases with the current increase, the noise characteristics become better from Eq. (10). However, once the amplitude is saturated, the jitter becomes worse since F is proportional to current I_{LC} (Eq. (9)). Therefore, the jitter characteristic of LCVCO gets worse in all cases as long as

quality factor of spiral inductor does not improve and supply voltage is scaled down as ITRS predicts. In other words, to mitigate jitter degradation, improving quality factor and/or using high-voltage transistors prepared for IO cells are necessary.

As for RingVCO, when we increase the current, the amplitude can be controlled by load resistance. The jitter characteristic becomes better as the power dissipation increases (Eq. (4)). On the other hand, the retargeting policy in this paper assumes that W/L is constant, which results in Eq. (6). Consequently, the jitter characteristic gets worse. Similar to LCVCO, moderate voltage scaling is preferable for RingVCO, since we can use smaller transistors and do not have to increase the current so much.

4. Conclusion

This paper describes the performance prediction of two clock generation PLLs, a ring oscillator based PLL and an LC oscillator based PLL with the qualitative evaluations and with the design experiments. The relative performance difference between RingPLL and LCPLL will be almost constant in the future. Power consumption and chip area of both PLLs will fortunately decrease proportional to the technology node. However, if the technology node progresses as it is, noise characteristics of both PLLs will get worse inversely proportional to the technology node. Our discussion indicates that low noise PLL circuit design will be more important in the future.

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Appendix

In this paper, we assume $f_0 L_s / V_{DD}$ is unchanged in LCPLL. The results of our discussion show that the jitter characteristics of both PLLs will degrade inversely proportional to the technology advance and the power dissipation of both PLLs decrease proportional to the technology node shown in Sect. 2 and 3. However, we can think of other scenario.

A scenario is $f_0 L_s$ being constant. In this case, the power dissipation of LCVCO (P_{LC}) decreases proportional to the square of the technology node and the jitter characteristic (J_{LC}/T_0) can be predicted as

$$\frac{J_{LC}}{T_0} \propto \sqrt{\frac{f_0}{(V_{DD})^2}}.$$

The results are compared in Fig. A· 1. Figure A· 1 shows how much jitter characteristics (jitter/period) at each technology node get worse if the jitter characteristic at technology node 180 nm is set to 1. Line (a) is our prediction condition, keeping $f_0 L_s / V_{DD}$ unchanged, and line (b) is this condition, keeping $f_0 L_s$ unchanged. Jitter characteristic under this condition is worse than that of our condition. Therefore, in this paper, we assumed $f_0 L_s / V_{DD}$ is kept unchanged in LCPLL.

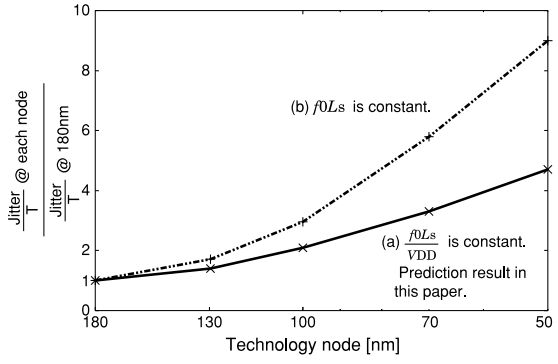

Fig. A· 1 Jitter characteristic degradations of LCVCOs; (a) our prediction condition; keeping $f_0 L_s / V_{DD}$ unchanged (b) keeping $f_0 L_s$ unchanged.

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