Measurement Circuits for Acquiring SET Pulse Width Distribution with Sub-FO1-inverter-delay Resolution

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Abstract—This paper presents two circuits to measure pulse width distribution of single event transients (SETs). We first review requirements for SET measurement in accelerated neutron radiation test and point out problems of previous works, in terms of time resolution, time/area efficiency for obtaining large samples and certainty in absolute values of pulse width. We then devise two measurement circuits and a pulse generator circuit that satisfy all the requirements and attain sub-FO1-inverter-delay resolution, and propose a measurement procedure for assuring the absolute width values. The operation of one of the proposed circuits was confirmed by a preliminary radiation experiment of alpha particles with a fabricated test chip.

I. Introduction

As devices integrated on VLSIs are minitualized, critical charge, which is the minimum charge to cause a bit flip (single event upset: SEU) or a glitch (single event transient: SET), becomes smaller, and functional correctness has been threatened by such soft errors. SEU and SET arise when radiation particles, such as alpha particles and neutrons, collide with Si substrate and electrons/holes whose amount is larger than the critical charge are induced and collected into sensitive nodes. Recently, neutron-induced soft error is becoming a concern even at the sea level [1–4].

When an SET pulse, which is generated in a combinational circuit, propagates to a sequential element (e.g. a flip-flop) and is captured at clock edges, the SET pulse causes an error. A wider SET pulse more probably causes an error, because there is a wider range of clock timing at which the SET pulse is mistakenly captured [5]. Generally, suppression and correction of SET-oriented errors are performed using time and/or space redundancy [6]. However, they have to pay a large performance penalty in speed and/or area depending on the reliability requirement and SET pulse width distribution. Therefore, information on the distribution of SET pulse width is eagerly demanded for SET-oriented soft error estimation [7] and suppression [6].

To characterize the distribution of SET pulse width at the sea level, accelerated neutron radiation tests, in which the neutron energy spectrum at the sea level is reproduced, are performed at some sites, such as Los Alamos. Meanwhile, several circuits have been proposed and successfully used for measuring the SET pulse width [8–11]. They directly measure the pulse width of each SET [8, 9, 11], or indirectly estimate the distribution of the SET pulse width from the statistic of SET errors [10]. However, they have remaining issues to resolve for obtaining the distribution with high resolution in time and/or high certainty in absolute values of pulse width.

II. Requirements for SET Measurement and Conventional Measurement Circuits

This section first describes requirements for measuring distributions of SET pulse width. We then introduce and examine conventional measurement circuits in terms of the requirements.

A. Requirements

We below enumerate five requirements for SET measurement in accelerated radiation tests.

R1: fine time resolution
To measure SET pulse width accurately, fine time resolution that is smaller than FO-1 inverter delay is desirable.

R2: wide time range
Measurable minimum pulse width should be FO-1 inverter delay, or minimum pulse width of data and/or clock for FF latch operation. The upper bound must be set to a large value because the pulse width is widely distributed.

R3: tolerance to soft errors
In radiation tests, soft errors necessarily occur even in the measurement circuit. To avoid mis-operation and mis-measurement, the measurement circuits should be soft
The SET pulse width $T$ satisfies
\[
(N-1)t_p < T < (N+1)t_p, 
\]
(1)

Fig. 1. Schematic of pulse-triggered capturing circuit. The example with $N = 3$ is shown.

Fig. 2. Temporal latch structure.
cups a small portion of the temporal latch, and the number of SET pulses per area is small. This means that long radiation experiment and/or large silicon area are necessary to obtain large number of SET samples. In addition, to perform the measurement with different \( t_d \), we need to reconfigure \( t_d \) and measure repeatedly. This approach makes the radiation test even longer, and hence is not practical. Another approach is to integrate several circuits with different \( t_d \), which needs large silicon area and considerably degrades area efficiency.

The pulse width resolution is decided by \( t_d \), and the minimum \( t_d \), which is the minimum measurable width, is two inverter delays of FO-1. Large \( t_d \) is easily realizable by increasing the number of gate stages. This measurement circuit is soft error tolerant because SETs in delay circuits are masked in majority gate and the remainders are targets for SET measurement. Besides, it is necessary to presume \( t_d \) for assuring the pulse width.

### III. Proposed Measurement Circuits

This section presents two novel measurement circuits that attain sub-FO1-inverter-delay resolution.

#### A. Measurement Circuit using Electrical Masking

The measurement circuit using electrical masking, which is proposed in this work, consists of a target circuit, a delay element (filter) chain, and 1-bit counters as illustrated in Fig. 3.

![Fig. 3. Proposed measurement circuit using electrical masking.](image)

Table I shows the number of fan-outs and filter thresholds where each filter can be adjusted by adjusting fan-outs, the expected performance is attained as listed in Table 1. Here, the performance was evaluated by circuit simulation assuming that wiring capacitances are proportional to the number of fan-outs.

<table>
<thead>
<tr>
<th>Filtering circuit</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
<th>13</th>
<th>14</th>
</tr>
</thead>
<tbody>
<tr>
<td>( T_{th} ) [ps]</td>
<td>42</td>
<td>61</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>140</td>
<td>160</td>
<td>180</td>
<td>200</td>
<td>220</td>
<td>240</td>
<td>260</td>
<td>280</td>
<td>300</td>
</tr>
</tbody>
</table>

#### B. Vernier Delay Line Circuit

Next, Vernier delay line (VDL) is introduced for SET measurement. VDL is composed of two buffer chains and a D-type latch chain, as illustrated in Fig. 4. Two step signals (START and STOP) with \( T \) time difference are given to this circuit, and \( T \) is to be measured by VDL. The buffer delay of the chain
overtaking should be 0, and after overtaking they should be 1. If an SEU flips a latch, this condition is not satisfied, which means the SEU is distinguishable and can be eliminated. SETs generated in the buffer chains do not cause mis-measurement. SETs in STOP line are not captured since no clock edges are given to latches. When SETs arise in START line, all the values stored in latches become zero and this case is easily distinguishable. Thus, Vernier delay line circuit is robust to soft errors.

C. Summary of Requirements and Satisfaction

Table II summarizes the requirements described in Section 2-A and the satisfactions of the circuits discussed in Sections 3-A and 3-B. We can see that the proposed two circuits satisfy R1-R4 requirements though pulse-triggered capturing circuit and temporal latch circuit do not satisfy R1 and R4, respectively. However, R5 is not satisfied in all the circuits. In order to satisfy R5, next section will present a pulse generator for assuring the measured pulse width coping with manufacturing variability.

IV. Assurance of pulse width using on-chip pulse generator

The proposed measurement circuits use delay elements, and a problem is that their delay is sensitive to manufacturing variability. An approach is to implement and measure replica of delay elements, however this approach can not cope with random manufacturing variability and mis-estimation of wiring capacitance. We thus implement an on-chip pulse generator to inject a pulse whose width itself can be assured by measurement. This approach is general since it is applicable to any types of SET measurement circuits and the correspondence table between pulse width and observable result can be built.

We here show an implementation of on-chip pulse generator. The circuit composition and operation example of the pulse generator are shown in Fig. 6 (a). It adopts an exclusive-or gate and a delay element as depicted in Fig. 7 similarly to [9,10]. In this circuit, an input transition is converted into a pulse whose pulse width is equal to the propagation delay of the delay element. To cancel out the MUX delay, MUX cells are inserted in both two paths to the XOR inputs. To continuously change the pulse width, the pulse generator is implemented so that the power supply voltage in the dotted rectangle in Fig. 6, $V_{DD}$, can be varied separately. When the changeable range of $t_d$ is not large enough, increasing the number of MUX inputs and choosing a delay element from several ones extend the changeable range.

To know the width of the generated pulse, $t_d$ should be measured. The estimation process of $t_d$ is explained in the following. The circuit is configured to oscillate by changing the select signal of the left MUX. The oscillating period $T$ of the path without delay circuit (Fig. 6(b)) is calculated from the counts in the large-bit counter. Similarly, the oscillating period $T'$ of the path including $t_d$ (Fig. 6(c)) is calculated. Based on these two oscillating periods, $t_d$ is obtained by

$$T' - T \approx 2t_d.$$  

To minimize the mismatch between $t_d$ and the generated pulse width, the inverter in the figure should be small.
Fig. 6. Schematic and operation examples of on-chip pulse generator: (a) pulse generation with \( t_d \) width, (b) oscillation using the path without delay circuit, and (c) oscillation using the path including \( t_d \).

Fig. 7. Schematic of general pulse generator that uses an XOR gate.

V. Preliminary Measurement Results

To confirm the operation of the presented measurement circuit using electrical masking, a preliminary test chip was fabricated in 65 nm process. A micrograph of the test chip is shown in Fig. 8. Figure 9 shows the organization of the test circuit. The circuit is composed of a pulse generator, a target circuit that is 204-stage inverter chain, and the measurement circuit with 9 filters.

The alpha particle tests were performed using an Americium-241 foil whose flux is \( 9 \times 10^9 \text{cm}^{-2}\text{h}^{-1} \). The radiation source was put immediately above on the test chip [14] and the outputs of 1-bit counters were observed at room temperature with 0.8 V operating voltage.

Figure 10 shows the measured distribution of SET pulse width in case of 17-hour radiation. The number of SETs measured during this test is 40, after SEUs arisen in the measurement circuit are eliminated. The threshold values \( T_{th} \) of 8 filters were estimated using the procedure described in Section 4. The measurable range of pulse width was 116 ps to 807 ps. We can see the purpose circuit is applicable to SET measurement.

VI. Conclusion

We have developed new circuits for measuring SET pulse width in accelerated neutron radiation experiment. To attain sub-FO1-inverter-delay resolution, two circuits are devised; one uses electrical masking and the other adopts Vernier delay line. We also presented a procedure to assure the measured pulse width using on-chip pulse generator that can change pulse width. The preliminary experiment of alpha-particle radiation
with a fabricated test chip confirmed that the proposed measurement circuit using electrical masking can be used for obtaining SET pulse width distribution.

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REFERENCES


