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BRIEF PAPER *Special Section on Circuits and Design Techniques for Advanced Large Scale Integration*

Impact of Self-Heating in Wire Interconnection on Timing*****

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SUMMARY This paper evaluates impact of self-heating in wire interconnection on signal propagation delay in an upcoming 32 nm process technology, using practical physical parameters. This paper examines a 64-bit data transmission model as one of the most heating cases. Experimental results show that the maximum wire temperature increase due to the self-heating appears in the case where the ratio of interconnect delay becomes largest compared to the driver delay. However, even in the most significant case which induces the maximum temperature rise of 11.0°C, the corresponding increase in the wire resistance is 1.99% and the resulting delay increase is only 1.15%, as for the assumed 32 nm process. A part of the impact reduction of wire self-heating on timing comes from the size-effect of nano-scale wires.

key words: *interconnect, delay variation, parasitic resistance, thermal, temperature, self-heat, SoC*

1. Introduction

In general SoC design flows, temperature dependence of signal propagation delay is treated as one of global variations [1], which impact all devices on a die similarly. Recently, self-heating problem of global and local wires has been investigated [2]–[6], and then necessity to treat local temperature variation was discussed [3], [7]. The heated wires deteriorate signal propagation delay due to increase in the wire electric resistance.

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However, realistic impact of the wire self-heating on the signal propagation delay has not been discussed well. This paper reviews factors to induce interconnect self-heating first, and then studies cases which are thought to be significant situations of the wire self-heating. The contribution of this work is to provide possible upper bound of the self-heating and resulting local delay increase of the upcoming 32 nm process. The most significant situation is also revealed through this work.

2. Impact of Self-Heating in Wire Interconnection on Timing

2.1 Factors to Induce Interconnect Self-Heating

Self-heating in wire interconnection is induced by wire resistance which consumes the electric energy, and then results in an increase in temperature. Self-heating problem of global wires has more intensively discussed than one of the local short wires, because relatively large distance from the substrate makes heat difficult to diffuse. On the other hand, local and intermediate wires are also possible to generate large temperature deviation because the electric current energy flows in relatively small volume of the wire segments [6]. From the material point of view, low-k insulator increases self-hearing because of low thermal conductivity.

2.2 Experimental Conditions

Taking into consideration the factors to induce interconnect self-heating, we evaluate a 64-bit data transmission model as one of the most heating cases. Figure 1 shows the entire circuit of the model. It consists of two parts. One is clock distributions shown in Fig. 2, which is a part of Fig. 1. In Fig. 2, R and C stand for interconnect resistance and capacitance, respectively. The clock buffer drives 64 flip-flops placed in line in the horizontal direction. The cluster consisting of 64 flip-flops (XC#1 to XC#64) form heavy loads, and then makes large current flow in the wire. This cluster size is considered to be the maximum of possible size [8], [9]. Length of the wire is determined by layout size of the flip-flop (FF). In order to form an extremely heating case, a single wire in the intermediate 4th layer metal drives all flip-flops. We set the width of the FF as 51 metal pitches, referring to a scan-FF donated by Nangate [10] (Fig. 3).

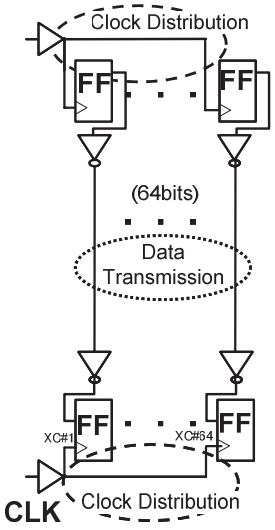

Fig. 1 64-bit data transmission model.

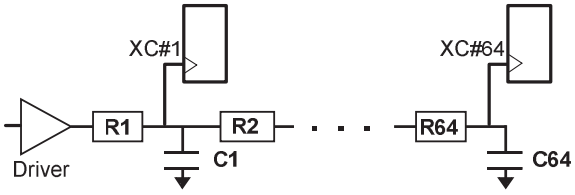

Fig. 2 Clock distribution.

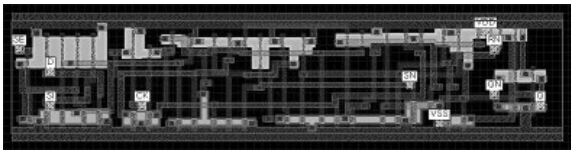

Fig. 3 Layout pattern of the scan flip-flop.

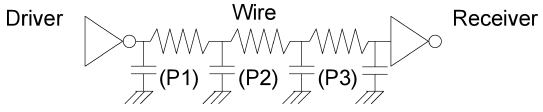

Fig. 4 Data transmission.

The other part is a data transmission part shown in Fig. 4, which is a part of Fig. 1. We control the driver size and the wire length so that signal propagation delay from the driver input to the receiver input is equal to $1/7$ of cycle time determined by the specified frequency. Receiver size is set to be same as the driver size. By means of Elmore delay, we varied the ratio of driver delay and wire delay as $\{1/8, 1/4, 1/2, 1, 2, 4, 8\}$. Appropriate driver size cannot be allocated outside of the range. For electrical and thermal analysis, the wire models are distributed into the three resistors and four capacitors shown in Fig. 4.

The reason why we adopted this model consists of the following two factors.

Table 1 Interconnect cross-sectional parameters.

Category	Year of Production	2013
General	Metal1 half pitch (nm)	32
	Insulator dielectric constant	2.8
	Cu temp. coeff. of resistance	0.00439
	Local clock frequency (MHz)	7344
Inter-connects (Metal 1)	Wiring pitch (nm)	64
	Aspect ratio (Cu wire)	1.9
	Wiring width (nm)	32
	Wiring thickness (nm)	60.8
	Dielectric thickness (nm)	60.8
Inter-connects (Inter-mediate)	Wiring pitch (nm)	64
	Aspect ratio (Cu wire)	1.9
	Aspect ratio (Cu via)	1.7
	Wiring width (nm)	32
	Wiring thickness (nm)	60.8
	Barriar thickness (nm)	2.4
	Dielectric thickness (nm)	54.4
	Effective resistivity ($\mu\Omega$cm)	4.83

Table 2 Thermal conductivity.

Material		SiO2	Air	(ITRS)2013
ϵ_r		3.9	1	2.8
Thermal conductivity	W/ meter k	1.38	0.0241	0.1601

1. Large temperature gain due to the wire self-heating can happen when wires have relatively large distance from the substrate which makes heat difficult to diffuse, or when the electric current energy flows in relatively small volume of the wire segments. Clock distribution is thought to be one of the most significant cases because large electric currents flow in intermediate metal wires.

2. Impact of wire self-heating on timing depends on the contribution of wire delay as well as the amount of heating. The data transmission bus can induce large temperature rises especially around the center bits because there are many heat sources surrounding the bits. Ratio of the wire delay can be controlled by varying driver/receiver size and wire length.

Referring related articles [11]–[13], we construct the 64 bit data transmission model for realistic evaluation.

In this work, we suppose the upcoming 32 nm process using corresponding ITRS interconnect parameters [14] and PTM SPICE model parameters [15]. Table 1 shows the interconnect parameters. From the predicted dielectric constant of low-k material, we deduce the corresponding thermal conductivity, assuming that the material consists of SiO_2 and air. Table 2 shows the retrieved thermal conductivity.

We use PTM parameters shown in Table 3 for the Elmore delay estimation, as well as for the circuit simulation. ϵ_0 and *epsrox* are the dielectric constant of vacuum, and the ratio of the oxide permittivity to that of vacuum, respectively. *cgso*, *cgdo*, *cgbo* are gate overlap capacitances of source, drain, and the end side edges. *toxm* stands for the gate oxide thickness. *L*, *W* are length and width of the gate.

Table 3 Capacitance parameters of unit MOS transistors.

Parameter		Unit PMOS	Unit NMOS
ϵ_0	F/m	8.85E-12	
epsrox		3.9	
cgso	F/m	8.50E-11	8.50E-11
cgdo	F/m	8.50E-11	8.50E-11
cgbo	F/m	2.56E-11	2.56E-11
toxm	m	1.75E-09	1.65E-09
L	m	3.20E-08	3.20E-08
W	m	9.00E-07	4.00E-07
Cgate	F	7.22E-16	3.37E-16

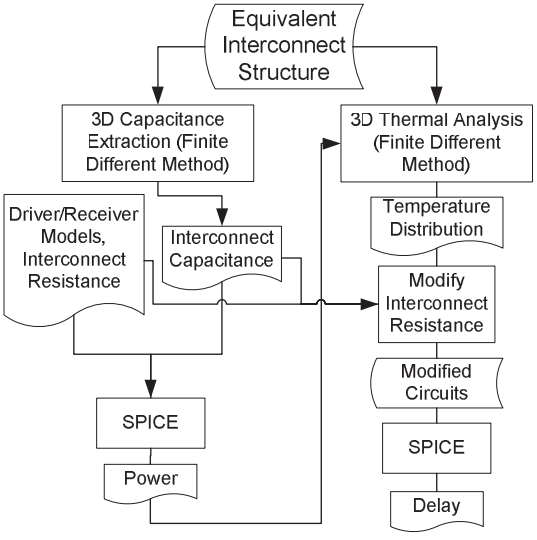

Fig. 5 Evaluation flow of the impact of wire self-heating on timing.

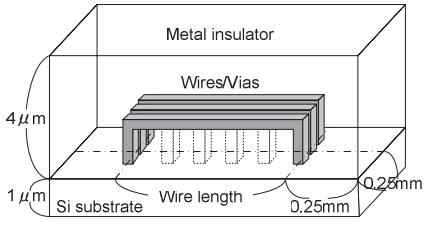

Fig. 6 Wire model for capacitance extraction and thermal analysis.

Total gate capacitance C_{gate} is calculated from *L*, *W*, *toxm*, and *epsrox* as a fixed value, and then applied to the Elmore delay estimation.

The entire flow of this work is shown in Fig. 5. Both of the electric field and the thermal analysis are achieved using the Finite Different Method (FDM) [16]. The extracted interconnect capacitances are used for deriving the power, as well as the delay estimation. Interconnect resistances in delay estimation are deviated considering the temperature rise simulated by the thermal analysis. Wire structures for capacitance extraction and thermal analysis are modeled as shown in Fig. 6 [6]. Thermal analysis is achieved setting the surface of the Si substrate uniformly to the reference temperature, because the wire self-heating is of interest. The rest of the boundaries is treated as periodic.

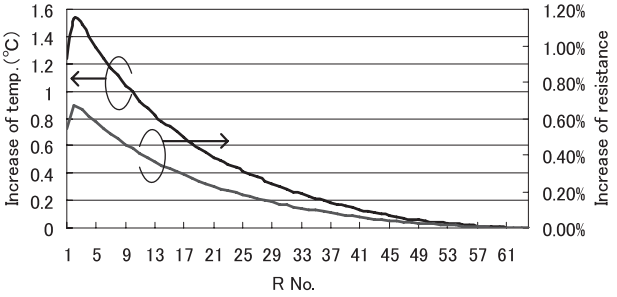

Fig. 7 Thermal effects on the clock distribution.

2.3 Simulation Results and Discussion

2.3.1 Clock Distribution

Driver size suitable for the specified physical parameters and local clock frequency of 7344 MHz becomes 64 times larger than the unit inverter used for input of the FFs, where the unit inverter consists of the unit PMOS and the unit NMOS specified in Table 3. In order to unify peak current of PMOS and NMOS, gate width of the unit PMOS is modified to 2.0 μm, here. As for the wire, 5 times larger width than the minimum width is required to fully drive the farthest FF. The reason is that wire resistance reduction by the width gain dominates the capacitance increase due to existence of the total gate capacitance. Actually, the total gate capacitance of FF becomes 124 fF and it is larger than the wire capacitance of 10–50 fF. In the equivalent interconnect structure, we assume power and ground lines to extend in parallel at 32 nm of the minimum spacing in both of the capacitance extraction and the thermal simulation. The experimental results of the clock distribution part are shown in Fig. 7. The numbers in x-axis are corresponding to the indexes of R in Fig. 2. It turns out that temperature increase becomes small along with the distance from the driver. In this case, even the maximum increase of temperature is 1.56°C, and then the resulting resistance increase is below 1%. We derive the resistance increase using the temperature coefficient in Table 7. The major reason why no significant temperature deviation appears is that the required larger width of wire makes the heat density low. In addition, a size-effect which is discussed below may ease the resistance rise, even though the effect is not taken into consideration in this case because the wire is wider compared to the minimum width.

2.3.2 Data Transmission

As to the data transmission part, driver sizes and wire lengths corresponding to the ratio of driver delay and wire delay are shown in Table 4. The maximum impact of wire self-heating on timing is derived by two steps shown in the following sub-sections.

Table 4 Driver size and wire length.

Driver delay to wire delay ratio	Driver size (per unit inverter size)	Wire length (μm)
1/8	22.4	26.8
1/4	7.2	52.5
1/2	3.6	59.7
1	2	57.1
2	1.2	48.9
4	0.8	38.8
8	0.5	29.3

Table 5 Thermal effects on an isolated single data transmission line.

Driver delay to wire delay ratio	Power(W)		
	P1	P2	P3
1/8	8.99E-06	8.34E-06	7.77E-06
1/4	2.76E-06	1.93E-06	1.37E-06
1/2	1.96E-06	1.16E-06	6.39E-07
1	1.45E-06	7.92E-07	3.65E-07
2	9.70E-07	5.13E-07	2.11E-07
4	6.00E-07	3.14E-07	1.23E-07
8	3.05E-07	1.57E-07	5.87E-08
Driver delay to wire delay ratio	ΔT(°C)		
	P1	P2	P3
1/8	1.62E-01	1.49E-03	1.37E-03
1/4	2.60E-02	1.77E-04	1.25E-04
1/2	1.60E-02	9.37E-05	5.19E-05
1	1.30E-02	6.74E-05	3.11E-05
2	1.00E-02	5.04E-05	2.08E-05
4	8.00E-03	3.85E-05	1.50E-05
8	6.00E-03	2.53E-05	9.80E-06

2.3.3 Screening the Case Which Offers the Maximum Impact of Wire Self-Heating on Timing

First, in order to screen the case where the most significant impact of wire self-heating occurs, we simplified the data transmission to a stand-alone single bit structure. Power and ground lines are assumed to extend in parallel at 32 nm of the minimum spacing. Thermal analysis results are shown in Table 5. P1/P2/P3 in Table 5 and the following Table 6 correspond to the wire resistance portions P1/P2/P3 shown in Fig. 4. The values of power stand for the power consumed by each resistance portion. Simulation results show that the maximum temperature deviation appears when the driver delay to wire delay ratio is 1/8. In general, impact of wire self-heating on signal propagation delay is thought to be determined by the contribution of wire delay, as well as the temperature rise. Here, the case showing the maximum temperature deviation is expected to have the maximum impact of wire self-heating on timing, since it also shows the largest ratio of the wire delay.

2.3.4 Estimation of the Maximum Impact of Wire Self-Heating on Timing

As for the most significant case, we arrange adjacent bit wires with the minimum spacing of 32 nm to estimate the effect of superposed heating on temperature rise. The experimental results are shown in Table 6. Values correspond to the center 33rd and 34th bits. Here, P2 shows the maximum temperature deviation because the heat can hardly diffuse due to heated adjacent wires.

Table 6 Maximum thermal effect to the data transmission in the 64-bit bus.

Driver delay to wire delay ratio		1/8
Power(W)	P1	8.99E-06
	P2	8.34E-06
	P3	7.77E-06
	Total	2.51E-05
ΔT(°C)	P1	5.49E+00
	P2	1.10E+01
	P3	5.49E+00
$\Delta R(\Omega)$	P1	0.996%
	P2	1.99%
	P3	0.996%

Table 7 Material resistance constants.

Material	$\rho_0(\Omega\text{cm})$	TCR_0
Copper	1.67E-06	4.33E-03
Barrier(Ta)	1.23E-05	3.30E-03

In order to derive increase in delay, we also take a size-effect [17] into consideration. In nano-scale wires, the size-effect to the wire resistivity does not depend on temperature. In other words, the total wire resistivity can be separated into a temperature-dependent part (the phonon contribution) and a temperature-independent part (the defect part) (Eq. (1)).

$$\rho_{total}(T) = \rho_{defect} + \rho_{phonon}(T). \tag{1}$$

Assuming that the size-effect affects only the defect part in Eq. (1), the derivative of the wire resistivity can be expressed in Eq. (2).

$$\frac{d\rho}{dT} = \rho_0(T) \times TCR_0(T), \tag{2}$$

where ρ_0 is the resistivity of the bulk material and TCR_0 is the corresponding linear temperature coefficient of resistance. The bulk material resistance constants applied to this work are shown in Table 7. We assume that the difference in resistivity between the ITRS specified value and a value derived from the bulk material constants stands for the defect part of the wire resistivity. The process to derive the resistance increase consists of the following three steps.

1. Referring Table 1, calculate the areas of copper and barrier for 32 nm wire width.
2. Assuming Ta for barrier, calculate the resistivity of the copper area, using the areas from Step 1, the effective resistivity of Table1, and the ρ_0 of Ta in Table 7. Subtracting the $\rho 0$ of Cu from the calculated resistivity of the copper area, derive ρ_{defect} in Eq. (1).
3. For each temperature before and after the rise, calculate the corresponding resistance, referring Table 7 and ρ_{defect}, which has no temperature dependence.

In this case, the resulting increase in the wire resistance is 1.99%. Circuit simulation results show that the resistance

increase induces 1.15% of rise in the signal propagation delay.

3. Conclusion

This paper evaluated impact of self-heating in wire interconnection on signal propagation delay estimation in an upcoming 32 nm process technology, using practical physical parameters. This paper examined a 64-bit data transmission model as one of the most heating cases. Simulation results show that large self-heating happens in short wires which drive heavy loads. The most significant case induces the maximum temperature rise from the ambient temperature becomes 11.0°C. However, the corresponding increase in the wire resistance is 1.99%, and delay increase is 1.15% as for the assumed 32 nm process. A part of the impact reduction of wire self-heating on timing comes from the size-effect of nano-scale wires. Concerning the future 22 nm node and beyond, the size-effect will have to be taken into consideration more, as well as use of low-k dielectric materials and small metal pitches.

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