Adaptive Performance Control with Embedded Timing Error Predictive Sensors for Subthreshold Circuits

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Abstract— This paper presents an adaptive technique for compensating manufacturing and environmental variability in subthreshold circuits using "canary flip-flop" that can predict timing errors. A 32-bit Kogge-Stone adder whose performance was controlled by body-biasing was fabricated in a 65 nm CMOS process. Measurement results show that the adaptive control can reduce the power dissipation by 46% in comparison with the worst-case design with guardbanding.

I. Introduction

Subthreshold circuits are attracting attention of designers implementing ultra-low power applications, such as a sensor-node processor [1]. However, there is a critical problem that prevents subthreshold circuits from being widely used; the performances are extremely sensitive to manufacturing and environmental variability due to an exponential dependence of subthreshold current on threshold voltage (V_{th}). Therefore, a traditional "worst-case" design with guardbanding is totally inefficient, and an adaptive performance control is indispensable for subthreshold circuits.

In this paper, a self-adaptive speed control for subthreshold circuits using "canary flip-flop" which can predict timing errors [2] is proposed. We will demonstrate that the adaptive control compensates manufacturing and environmental variability and reduces power dissipation by 46% compared to traditional worst-case design and operation with guardbanding.

II. Self-adaptive speed control with canary FF

A. Overview

Figure 1 shows an overview of the self-adaptive speed control with canary FF [3]. Canary FF, which consists of a normal FF (we call it "shadow FF"), a delay buffer and a comparator, generates a warning signal to predict the occurrence of timing errors. The warning signal is monitored during a specified period. Once the warning signal is detected, the circuit is controlled to speed up. If no warning signals are generated during the monitoring period, the circuit is controlled to slow down. The circuit speed is controlled digitally and we use a term "speed level" to describe how fast or slow the circuit is controlled to be. Higher speed level means the circuit is controlled for faster operation.

B. Circuit structure of test chip

We designed and fabricated a test circuit to demonstrate the adaptive speed control with canary FF in a 65 nm CMOS process. The structure of the test circuit is depicted in Fig. 2. A 32-bit Kogge-Stone adder (KSA) was adopted as a circuit whose performance was controlled. We implemented the "configurable" canary FF such that the inserted location and the buffer delay can be configured. The configurable canary FF is composed of 16 canary FFs with variable delay buffer.

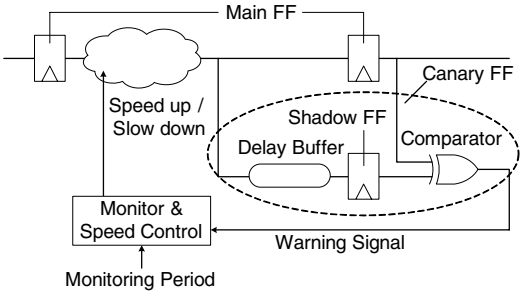

Fig. 1. Self-adaptive speed control with canary FF.

The speed control unit alters by body-biasing the speed of the KSA, main FFs and canary FFs at inputs and outputs of the KSA. Figure 3 shows the schematic of the speed control unit. VPW/VNW denotes p-/n-well body-bias voltage of the KSA, main FFs, and canary FFs. Four speed levels can be provided by applying four pairs of body-bias voltage (VPW0–3 and VNW0–3), where each body-bias voltage is supplied by external DC voltage sources. VPW and VNW are selected from VPW0–3 and VNW0–3 according to the speed level stored in a two-bit register.

The circuit operation starts at the maximum speed level. When the monitoring period of the warning signal elapses, a timer signal is asserted. At that time, the speed control unit decrements the speed level by one and the circuit is controlled to slow down. In contrast, when the warning signal is asserted, the speed control unit immediately increments the speed level by one and the circuit is controlled to speed up.

III. Measurement Results

Figure 4 shows the power dissipation at the various temperature conditions (25–70˚C) when the operation frequency and V_{DD} were 3 MHz and 350 mV in the following cases;

CT1: the circuit was controlled adaptively with a canary FF,

CT2: 200 mV-FBB (forward body-bias), which was the minimum body-bias for 3 MHz operation at 25˚C, was fixedly applied,

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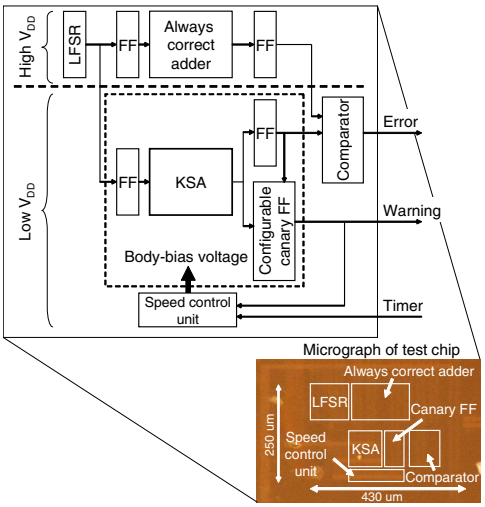

Fig. 2. Block diagram and the micrograph of the test circuit. 32-bit Kogge-Stone adder (KSA) is controlled adaptively.

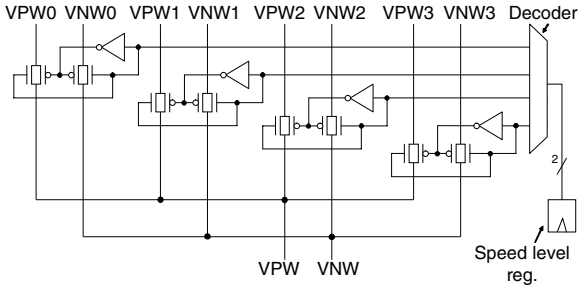

Fig. 3. Schematic of the speed control unit. VPW and VNW denote body-bias voltages of the KSA, main FFs, and canary FFs.

CT3: the minimum FBB voltage required for 3 MHz operation at each temperature was applied.

The power dissipation includes those of the KSA, the main FFs, the speed control unit, and canary FF. The power overhead of a canary FF was estimated to be around 2% by circuit simulation. We can see that the power dissipation of CT1 is very close to that of CT3, which means optimal body-bias voltages were selected adaptively at each temperature. Consequently, the power dissipation of CT1 at 75˚C was 39% smaller than that of CT2. This indicates that the fixed performance compensation (CT2) is significantly inefficient for subthreshold circuits because their performances are sensitive to temperature.

We next discuss the worst-case design in terms of manufacturing variability. Figure 5 shows the power dissipation of five chips when the operation frequency was 2 MHz in the following cases;

CM1: all chips operated at $V_{DD} = 0.5$ V, which was the minimum V_{DD} for a chip at SS device corner to operate correctly at 2 MHz,

CM2: all chips operated with adaptive control using a canary FF at $V_{DD} = 0.35$ V.

In the case of the adaptive control (CM2), an adequate body-bias voltage was applied to compensate the manufacturing

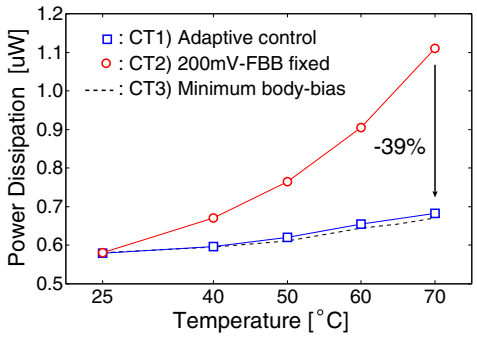

Fig. 4. The power dissipation at the various temperature conditions (3 MHz @ $V_{DD} = 0.35$ V). The circuit operates CT1) adaptively, CT2) with 200 mV-FBB fixedly, and CT3) with a minimum body-bias required for 3 MHz operation at each temperature.

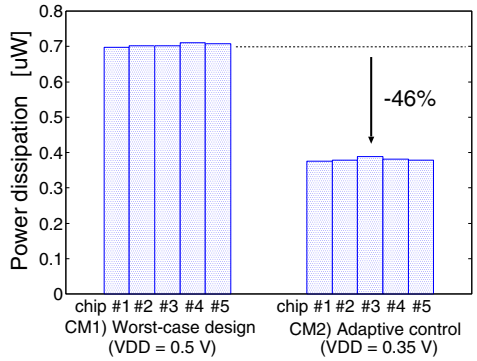

Fig. 5. The power dissipation when the operation frequency is 2 MHz in the following cases; CM1) all chips operate at $V_{DD} = 0.5$ V, CM2) all chips operate with the adaptive control at $V_{DD} = 0.35$ V.

variability of the each chip at $V_{DD} = 0.35$ V, whereas the conventional worst-case design (CM1) requires a large margin (here, higher V_{DD} was applied) to guarantee the correct operation even for a chip at the worst process corner. Consequently, the power dissipation of CM2 was smaller than that of CM1 by 46%. This means that the operation with guardbanding spoils the good energy-efficiency of subthreshold circuits.

IV. Conclusion

This paper demonstrated the self-adaptive control with canary FF compensated manufacturing and environmental variability on silicon using 65nm subthreshold circuit. Compared with guardbanding approach, power dissipation was reduced by 46%.

Acknowledgements

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