

## Gate Delay Estimation in STA under Dynamic Power Supply Noise

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**Abstract** –This paper presents a gate delay estimation method that takes into account dynamic power supply noise. We review STA based on static IR-drop analysis and a conventional method for dynamic noise waveform, and reveal their limitations and problems that originate from circuit structures and higher delay sensitivity to voltage in advanced technologies. We then propose a gate delay computation that overcomes the problems with iterative computations and consideration of input voltage drop. Evaluation results with various circuits and noise injection timings show that the proposed method estimates path delay fluctuation well within 2% error on average.

### I. Introduction

Recently, Power/Ground voltage level fluctuation (PG noise) is becoming a primary concern in designing LSI products with the progress of technology scaling. Current density in a chip has been increasing due to increase in operating frequency and power consumption in spite of decrease in supply voltage. This tendency makes circuit timing more susceptible to supply noise, and hence timing verification taking PG noise into account is essential for successful chip design.

Conventionally, the timing degradation due to PG noise is often estimated by annotating voltage drops at each instance. The voltage drops are obtained by static IR-drop analysis, which performs DC analysis using current consumption averaged within a cycle time. There are some reports that timing estimates based on the average voltage are well correlated with measurements [2][3]. On the other hand, power supply noise is dynamic in nature. It has not been clearly demonstrated what the limitation of timing analysis based on static IR-drop analysis is, and under what conditions it becomes inappropriate.

With technology scaling and voltage lowering, the over-drive voltage ( $V_{dd} - V_{th}$ ) is decreasing, which means gate delay becomes more sensitive to power supply voltage. Figure 1 depicts delay sensitivities of a 10-stage inverter chain to supply voltage in 180nm and 45nm technologies. The horizontal and vertical axes are static voltage drop ( $\Delta V$ ) and ratio of path delay change to the path delay at an ideal supply voltage ( $\Delta D_{path}/D_{path}$ ), respectively. The sensitivity at 45nm is five times higher than at 180nm when  $\Delta V = 0.2V$ , and it has a strong non-linearity. Unfortunately, PG noise level is not scaling down and is nearly constant despite lowering power supply voltage [4]. Thus, first-order approximation using Taylor expansion and static IR drop analysis will be more difficult to accurately capture the effect of noise on timing.

Decoupling capacitance insertion is a well-known and

effective way to suppress power supply noise [5]. Conventionally, it is inserted to satisfy constraints in noise voltage, and it has not been directly associated with timing except a few papers such as [6], since the timing estimation that takes into account dynamic voltage drop has not been well established. To insert necessary and sufficient decoupling capacitance without wasteful gate leakage, the impact of dynamic noise on timing must be accurately estimated.

To capture the impact of dynamic noise behavior on timing, static timing analysis under given noise waveforms has been studied [7][8]. These methods eliminate dynamic behavior by assigning equivalent DC values to each instance. The DC values are computed by, for example, averaging the noise voltage within a time interval of interest so that time-variant voltage can be considered in each gate delay computation. This treatment necessarily increases gate delay when the voltage drops. However, focusing on each cell delay, this is not true, as [7] pointed out. [7] examines delay variation due to power noise separately for rise transition and fall transition, and shows that cell delay decreases in the case of fall transition under  $V_{dd}$  noise. [7] then proposed computing an equivalent DC voltage for each instance separately for rise and fall delays. This is also symmetrically applicable to ground noise. The accuracy was evaluated in 180nm technology and confirmed to be reasonable. However, it is not clear whether [7] is still valid in current technologies, since the relation between voltage and delay has become much different as shown in Fig. 1.

In this paper, we propose a dynamic noise aware timing analysis method that is compatible with conventional gate-level static timing analysis. We first examine the meaning of timing analysis based on static IR-drop analysis, and discuss its limitation. Next, to cope with high sensitivity and non-linearity, we carefully review the previous work proposed in [7], and point out two issues that degrade the estimation accuracy. When supply voltage drops and fall delay is considered, both increase and decrease in delay are observed in our analysis, whereas [7] estimates delay decrease only. To solve this problem, the proposed method computes two equivalent voltages corresponding to the input voltage level and the supply voltage of the gate. For the second issue, we carefully calculate the time interval in which the equivalent voltage level is computed in the proposed method.

The rest of paper is organized as follows. In Sect. II, we discuss the meaning of timing analysis based on static voltage drop analysis. Sect. III reviews the conventional method [7] at the 45 nm technology node and shows that accuracy improvement is necessary. In Sect. IV, we present

the proposed procedure for estimating delay fluctuation. Sect. V experimentally evaluates the proposed procedure and Sect. VI concludes the paper.

## II. The Relation between Static and Dynamic Analysis

This section reviews the meaning of timing analysis using static IR-drop analysis, and discusses the relation between static noise based and dynamic noise based analyses.

Let us express path delay fluctuation due to PG noise  $\Delta D_{path}$  using delay sensitivity to voltage at each instance in a path as follows.

$$\Delta D_{path} = \sum_{i=1}^n \frac{\partial D_i}{\partial v} \Delta v_i \quad (1)$$

$$\Delta v_i = \frac{1}{T_i - T_{i-1}} \int_{T_{i-1}}^{T_i} \Delta v dt \quad (2)$$

Here,  $n$  is the number of stages and  $\Delta v$  is given noise voltage.  $T_i$  and  $D_i$  are arrival time at the  $i_{th}$ -stage gate output and stage delay of the  $i_{th}$ -stage gate, respectively.  $\Delta v_i$  is the equivalent voltage of  $\Delta v$  averaged between  $T_{i-1}$  and  $T_i$ , where this time window corresponds to the timing range when the  $i_{th}$ -stage gate is switching.  $\Delta D_{path}$  is expressed as the sum of products of the sensitivity to voltage  $\partial D_i / \partial v$  and the equivalent voltage  $\Delta v_i$ . The sensitivity  $\partial D_i / \partial v$  is expressed as up to the  $m_{th}$ -order polynomial as follows.

$$\frac{\partial D_i}{\partial v} = a_0 + \sum_{j=1}^m a_{ji} \cdot \Delta v_i^j \quad (3)$$

Here, under an assumption that each instance has the identical sensitivity, Eq. (1) is simplified as

$$\Delta D_{path} = a_0 \int_{T_0}^{T_n} \Delta v dt + O(\Delta v^2). \quad (4)$$

Equation (4) means that delay fluctuation  $\Delta D_{path}$  is expressed as a function of the integral of noise, and it does not depend on the noise waveform shape.

We experimentally confirmed the above property at a 45nm technology node. Figure 2 depicts the setup and parameter definitions of the experiment. We used triangular waveforms for power supply noise. In the experiments, we chose the width and height of the noise so that the integral of noise was unchanged, and altered the noise injection timing.

Figure 3 shows the circuit simulation results as a function of noise injection timing. Solid and dashed lines correspond to different waveform shapes. The figure indicates that the fluctuations are nearly constant as long as the whole noise waveform is included within the path timing window. That is, the delay fluctuation is mostly dependent on the integral of noise and almost independent of the noise shape.

This is the reason why static IR-drop analysis has been reasonably used in timing analysis for annotating voltage drop to each instance. When analyzing a path whose delay is close to the cycle time, the time interval between  $T_0$  and  $T_n$  becomes almost the clock cycle, which means the noise integral in Eq. (4) is equivalent to the static IR-drop. Equation (4) assumes that each instance has an identical sensitivity. As long as the variation of sensitivity is not

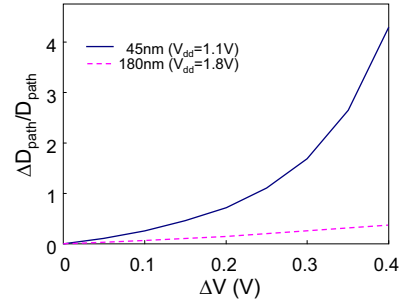


Fig. 1 Comparison of delay sensitivity to voltage between 180nm and 45nm.

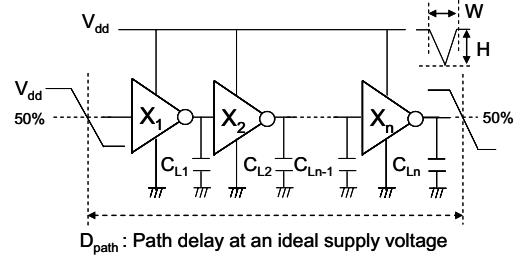


Fig. 2 Experimental circuit setup and parameter definitions.

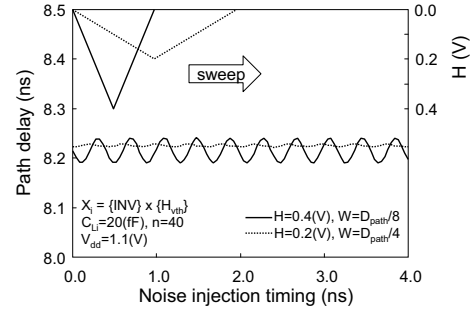


Fig. 3 Delay fluctuation of uniform topology case due to power supply noise.

significant, the estimation of delay fluctuation based on static IR-drop analysis gives a good approximation.

Conversely, Eq. (4) cannot be used for short path delays, which are usually checked for hold constraints, since the time interval for integral differs greatly with cycle time.

More importantly, in cases where the sensitivity is very different instance by instance, the static noise voltage is not appropriate to estimate timing fluctuation. This situation can be often found in industrial designs. For example, large delay buffers are intentionally inserted in a high speed clock line to adjust the phase relative to external signal timing. Normally, the large delay buffers tend to have higher delay sensitivity to voltage. This problem could be aggravated when using multiple- $V_{th}$  cells. If the inserted buffers have significantly different sensitivity from the others, it may result in timing failure due to noise. As shown in Sect. I, the sensitivity becomes higher with technology scaling. To prevent or predict the timing failures, consideration of dynamic voltage drop in timing analysis is becoming indispensable in recent technologies.

## III. Conventional Method and Its Problems

In this section, we introduce a conventional method to

estimate delay fluctuation due to dynamic PG noise [7], and point out its problems through experimental evaluation in 45nm technology.

[7] classified mechanisms to change the propagation delay into two categories; *charge change case* and *current change case*. In the following subsections, these two cases are examined. Since ground noise can be treated similarly, its discussion is omitted throughout this paper.

Figure 4 shows an example of circuits used for evaluation. Low and high  $V_{th}$  cells are included. We altered the noise injection timing similarly to Fig. 3, and computed the delay fluctuation both by [7] and circuit simulation. Figure 5 shows the evaluation results. The stage delays of each instance X1 through X4 are plotted. Solid and dashed lines represent the stage delay estimated by the conventional method and by SPICE simulation, respectively. We can see that the estimated delay is not consistent with the simulation result. We will now explain the *charge change case* and *current change case* and examine Fig. 5 considering the two cases.

#### A. Delay increase in Charge Change Case

Figure 6 illustrates an example of *charge change case* with an inverting cell. Suppose that the output is falling under power supply noise. As shown in the figure, the voltage when the signal transition starts has already dropped through a conducted PMOS. In this case, the output swing is small and the amount of charge stored in the output loading changes, which results in a decrease in the propagation delay. Thus, the output voltage  $V_{i0}$  when the output transition starts is important, and hence  $V_{i0}$  is regarded as equivalent DC voltage in [7].

In Fig. 5, instances X2 and X4 correspond to the *charge change case*. The traces of the instances computed by [7] represent decrease in stage delay from the one at an ideal supply voltage (rightmost value of each trace). However, circuit simulation shows both increases in stage delays as well as decreases in stage delays, which has not been pointed out before. As a result, instance X2 shows a completely opposite tendency compared with the reference. Both increases and decreases in stage delay should be modeled to improve the accuracy otherwise the estimation becomes optimistic.

#### B. Voltage interval to average in Current Change Case

Let us suppose a rise transition under power supply noise, where this case is called *current change case*. Figure 7 shows an example. The voltage drop reduces the current to charge output loading, and hence it increases propagation delay. The average voltage between  $t1$  and  $t2$  is empirically used as the equivalent DC voltage  $V_{dd\_eq}$ ,

$$V_{dd\_eq} = \frac{1}{t2 - t1} \int_{t1}^{t2} V_{dd\_actual} dt, \quad (5)$$

where  $V_{dd\_actual}$  is the supply voltage with noise,  $t1$  is the time when the output starts transition, and  $t2$  is the time

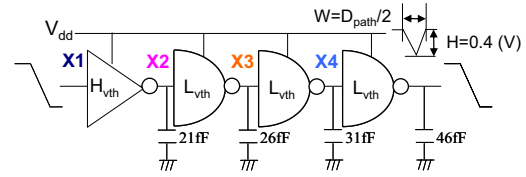


Fig. 4 An example circuit to evaluate [7].

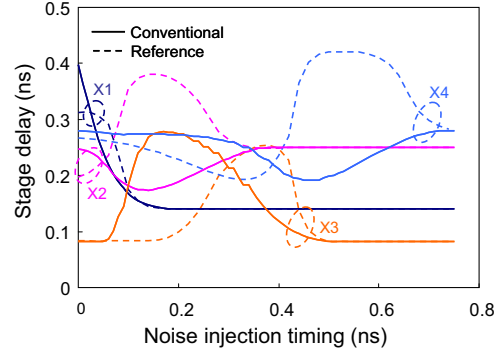


Fig. 5 Evaluation results of conventional method [7].

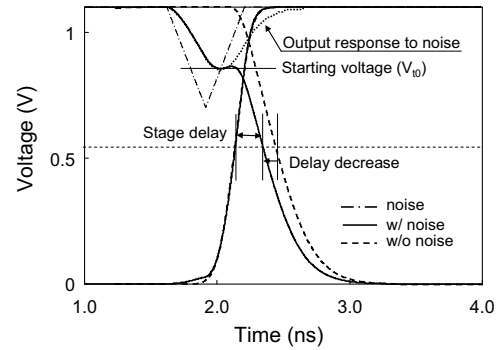


Fig. 6 Stage delay decrease in Charge Change Case.

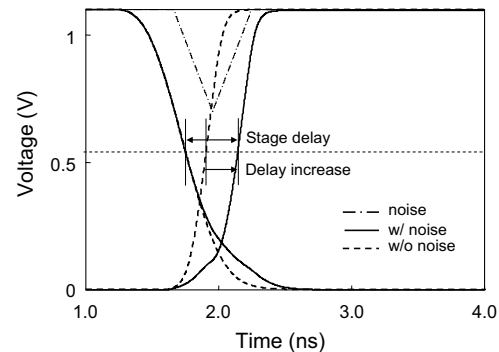


Fig. 7 Stage delay increase in Current Change Case.

when the output voltage swing becomes 60% of  $V_{dd}$  in [7]. For ease of calculation, [7] computes  $t1$  and  $t2$  from the transitional waveforms without power supply noise, and uses them in Eq. (5).

In Fig. 5, instances X1 and X3 correspond to this case. Here, let us look at instance X1. X1 is the first stage of the path, and so no earlier computation at upstream instances affects the results. The trace of X1 computed by [7] starts with a pessimistic estimation at time 0, and then rapidly decreases to an optimistic estimate. Our extensive evaluation under various conditions suggests that the interval in Eq. (5)

is too narrow in the case of X1 in Fig. 5. The estimation of X3 is more complicated, since it depends on the estimates of the upstream instances. In fact, the rising and falling slopes of the estimation are quite different from the reference. Revising the time interval to average in Eq. (5) is needed to improve the accuracy and avoid optimistic / pessimistic estimation.

#### IV. Proposed Stage Delay Computation

From the discussion in the previous section, revising averaging interval on the voltage in *Current Change Case* and capturing delay increase in *Charge Change Case* are needed to improve the estimation accuracy. This section describes how to solve these problems.

##### A. Revising integration interval to average in Current Change Case

We here define  $t_1$  and  $t_2$  in Eq. (5) so that the estimated delay becomes more accurate, and describe how to obtain  $t_2$  in the stage delay computation. In the proposed method,  $t_1$  and  $t_2$  are set to 50% crossing times of the input transition and the output transition, respectively. This definition is reasonable, since the time interval between  $t_1$  and  $t_2$  is the propagation delay itself, and the impact of the supply noise on the stage delay is directly considered. The problem here is how to estimate  $t_2$ , since  $t_1$  is already computed for upstream instances in STA.

The difficulty in estimating  $t_2$  is that the dependency of  $t_2$  on the supply noise. Using the equivalent voltage approach,  $t_2$  is required to compute  $V_{dd\_eq}$ , and  $V_{dd\_eq}$  is necessary for  $t_2$  computation. We thus adopt an iterative computation. This procedure is illustrated in Fig. 8. The goal is to find  $t_2$  satisfying that  $(t_2 - t_1)$  equals to the stage delay  $D_i + \Delta D_i$ , where  $\Delta D_i$  is estimated using Eq. (5) and  $t_2$ . We first set  $T_{i,0}$  ( $=t_2$ ) to  $T_{i-1} (=t_1) + D_i$ . We then iteratively increase  $T_{i,j}$  by a small step  $\Delta t$ , and estimate  $\Delta D_{i,j}$  from delay sensitivity ( $f$ ) using Eq. (5) and  $T_{i,j}$ . If the difference between  $T_{i,j} - T_{i-1}$  and  $\Delta D_{i,j}$  is smaller than  $\Delta t$ , the iteration finishes. Although the computational cost of forward time traversing is not significant, other efficient approaches, such as binary search, could be applied to reduce CPU time if necessary.

Note that if delay sensitivity to voltage (function  $f$  in Fig. 8) is linear and the fluctuation ( $\Delta D_i$ ) is relatively small to the original ( $D_i$ ) as the 180nm case in Fig. 1, the pre-defined time interval in Eq. (5) gives reasonable approximation. However, since the sensitivity is not linear in the 45nm case in Fig. 1, detailed computation of the integration interval becomes essential.

##### B. Capturing stage delay increase in Charge Change Case

The delay decrease in the *Charge Change Case* arises since the falling transition starts from the lower voltage. That is, this behavior is related to the power supply voltage of the instance of our interest.

On the other hand, the timing region of delay increase

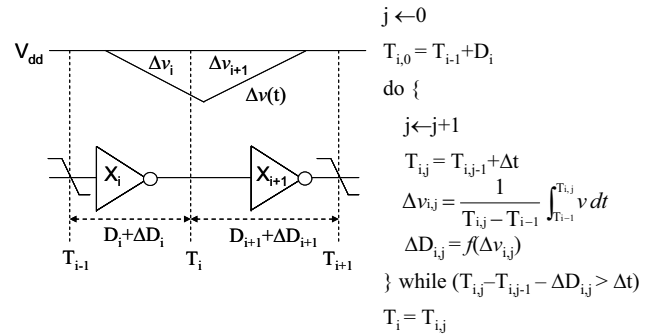


Fig. 8 An iterative procedure to obtain stage delay increase from voltage-delay characteristics.

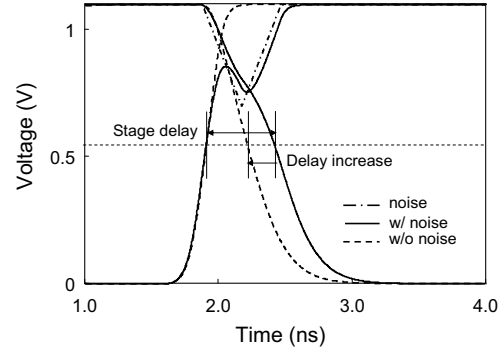


Fig. 9 Stage delay increase in *Charge Change Case*.

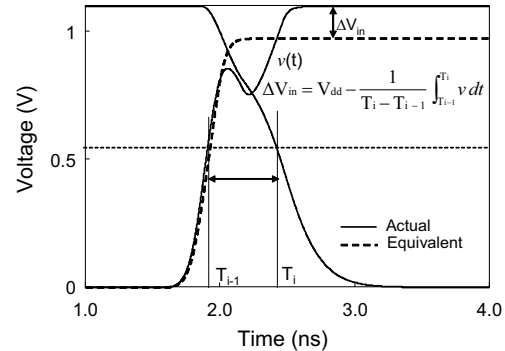


Fig. 10 Equivalent voltage of stage delay increase in *Charge Change Case*.

appears after the region of delay decrease. In the delay increase region, the PMOS transistor is already OFF, and hence the behavior of the delay increase originates from NMOS transistor operation. Figure 9 shows transitional waveforms in this region. In this case, the input voltage of the gate changes non-monotonically, and then the discharging current flowing through NMOS is reduced due to lower  $V_{gs}$  voltage. This behavior is related to the input voltage given to the instance. To capture the delay increasing behavior, the dependence of stage delay on input voltage level, which is not considered in [7], should be considered as well as the dependence on the supply voltage.

In *Charge Change Case*, both decrease and increase in stage delay ( $\Delta D_i'$ ,  $\Delta D_i''$ ) have to be considered.  $\Delta D_i'$  is estimated similarly to [7]. The voltage drop of the instance output due to noise at a specific time is estimated and used as an equivalent DC voltage drop  $\Delta V_{dd}$ .  $\Delta D_i''$  is estimated

by regarding the noisy input waveform as the reduction in input voltage swing. The equivalent voltage reduction in input voltage  $\Delta V_{in}$  is computed using integration, as shown in Fig. 10. When computing this integral, the time interval is important similarly to Eq. (5). To accurately estimate  $\Delta V_{in}$ , we adopt an iterative computation presented in Sect. IV. A.

To obtain the gate delay using  $\Delta V_{dd}$  and  $\Delta V_{in}$ , some pre-characterization of each cell is necessary. Figure 11 (a) explains a simulation setup for characterizing the decrease in stage delay. The relation between the power supply voltage drop ( $\Delta V_{dd}$ ) and stage delay decrease ( $\Delta D_i$ ) is characterized keeping the input voltage swing fixed. Figure 11 (b) presents a setup to characterize the stage delay increase. The relation between the decrease in input voltage swing ( $\Delta V_{in}$ ) and stage delay increase ( $\Delta D_i$ ) is obtained while keeping power supply voltage ( $V_{dd}$ ) and input transition-time ( $T_{in}$ ) unchanged.

A question here is why the delay increase in the *current change case* was missed in [7]. Figure 12 shows the ratio of stage delay fluctuation due to power supply noise depending on the noise injection timing, where a 10-stage inverter chain is evaluated at 180nm technology node. Peak voltage of power supply noise is set as shown in Fig. 4. From the figure, the increase in falling stage delay (X4, X6, X8, X10) can be observed but its magnitude is negligibly small. This is because the decrease in  $(V_{dd} - V_{th})$  makes the discharging current sensitive to the input voltage level. Thus, advanced technology necessitates more detailed analysis.

## V. Experimental Results

We implemented the proposed method and evaluated the accuracy in a 45nm technology.

Figure 13 shows the results estimated using the proposed method for the same circuit with the same setup as Fig. 5. We can clearly see that the traces of instances X1 and X3 are improved thanks to the revision of the integral interval in Eq. (5). The figure also shows that the traces of instances X2 and X4 reproduce well both increase and decrease in the stage delay.

We next evaluated the accuracy for various topologies. One hundred experimental circuits were randomly generated according to the parameter variations in Table 1 and used for the accuracy evaluation. The gates in each path were chosen from 12 combinations (3 logics  $\times$  2 drivability  $\times$  2  $V_{th}$ ). The output load of each stage was selected randomly in the range of [1, 30] (fF). The noise waveform was triangular and the height and width were chosen so that the noise was equivalent to 4.5% static IR-drop which corresponds to 9.6% path delay margin on average. We set the time step in the iterative computation to 10 ps in the experiments.

For each circuit, we performed timing analysis alternating noise injection timing within the timing window of the path. The relative error to SPICE simulation is calculated at each noise injection timing, and the average and standard deviation of the estimation error are computed for each circuit. Figure 14 shows the evaluation results. The horizontal and vertical axes are the average and standard deviation of the relative error, respectively. The evaluation

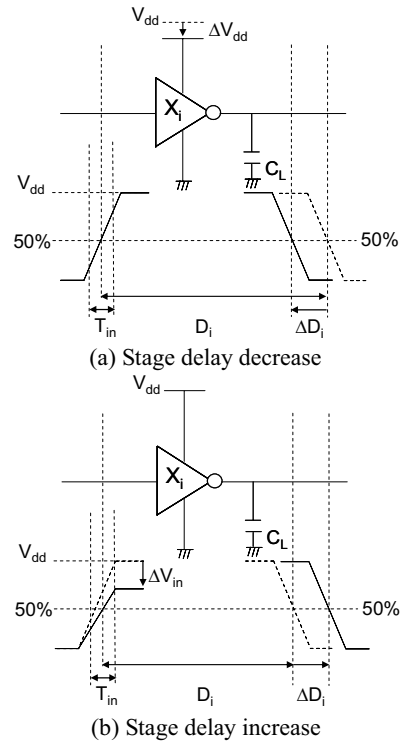


Fig. 11 Characterization for *Charge Change Case*.

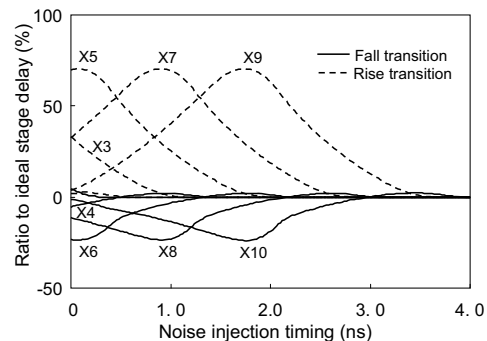


Fig. 12 Stage delay fluctuations due to power supply noise of 10 stages inverters at 180nm technology.

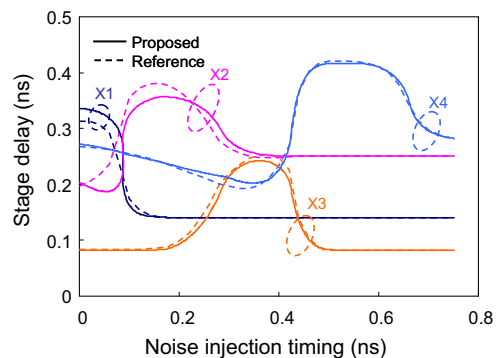


Fig. 13 Evaluation results of proposed method.

results are summarized in Table 2.

The delay variation ratios due to the noise itself are shown in the figure labeled “w/o noise consideration”, and the average ranges 6% to 11% and the standard deviation 2% to 5%. Unless any design strategies to cope with power supply noise are applied, a timing margin which is larger than the



Table 1 Parameter variation for accuracy evaluations.

Parameter	Values
$X_i$	INV, NAND2, NOR2
Drivability	x1, x8
Cell $V_{th}$	$H_{vth}, L_{vth}$
$C_{Li}$	[1, 30] (fF)
#stage (n)	10
W	$D_{path}/2$
H	0.2 (V)
#circuits	100

fluctuations should be set.

When the timing fluctuation is estimated based on static IR-drop analysis (labeled “Average” in the figure), the estimation errors are greatly reduced to within 3% average with 4% standard deviations. The average and standard deviation of the relative errors are 1.4% and 3.3%, respectively. Static IR-drop based approach does not take the noise injection timing and waveform into account, and hence the delay variation that is dependent on noise injection timing should be taken into account as a timing margin.

The conventional and proposed methods are expected to estimate the delay fluctuation accurately since they take into account the noise injection timing and dynamic waveform. However, the estimation errors of the conventional method are -7% to 8% on average with 2% to 11% standard deviation. The average and standard deviation of the errors are 2.0% and 5.0%, respectively. Due to the problems discussed in Sect. III, the estimation is not accurate.

On the other hand, the estimation accuracy is improved by the proposed method. The estimation error ranges from -2% to 2% on average with 1% to 3% standard deviation. The average and standard deviation of the relative errors are 0.61% and 1.8%, respectively. By solving the dominant issues that degrade estimation accuracy in [7], gate delay computation under dynamic power supply noise that is compatible with conventional STA has been established in this work. The improvement in accuracy helps to reduce timing margin for guard-banding, and thus the proposed method contributes to enhancement in performance and/or timing convergence.

## VI. Conclusions

In this paper, we discussed the estimation of stage delay fluctuation due to power supply noise. Firstly, we pointed out two problems in the conventional method; (1) delay increase in *Charge Change Case* was not considered, (2) pre-defined time interval for averaging supply voltage was not valid due to high delay sensitivity to voltage and its non-linearity. We then proposed a gate delay computation for estimating delay fluctuation that iteratively updates the time interval. Delay increase in the *charge change case* is estimated by computing equivalent DC voltages both of input voltage and supply voltage. The evaluation results show that the procedure estimates delay fluctuation well to within -2% to 2% on average with 1% to 3% standard deviation. The proposed method computes increase/

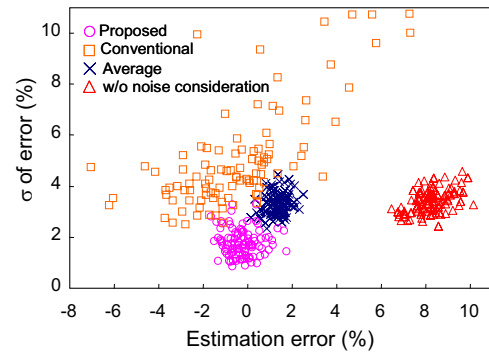


Fig. 14 Accuracy evaluation results of estimation method for delay fluctuation due to power supply noise.

Table 2 Summary of accuracy evaluation results.

Estimation methods	Est. error	
	$\mu$ (%)	$\sigma$ (%)
without noise consideration	8.2	3.4
Average	1.4	3.3
Conventional	2.0	5.0
Proposed	0.61	1.8

decrease in stage delay at the 50% crossing point, and hence it has a good compatibility with STA applications.

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